Breve introduzione all'elettronica e alla microelettronica

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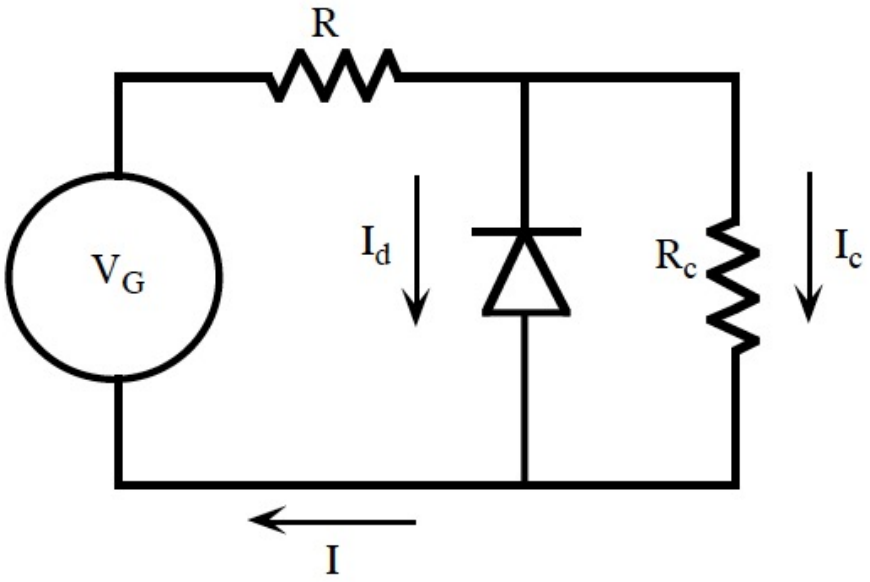
Corso di Fondamenti Fisici di Tecnologia Moderna

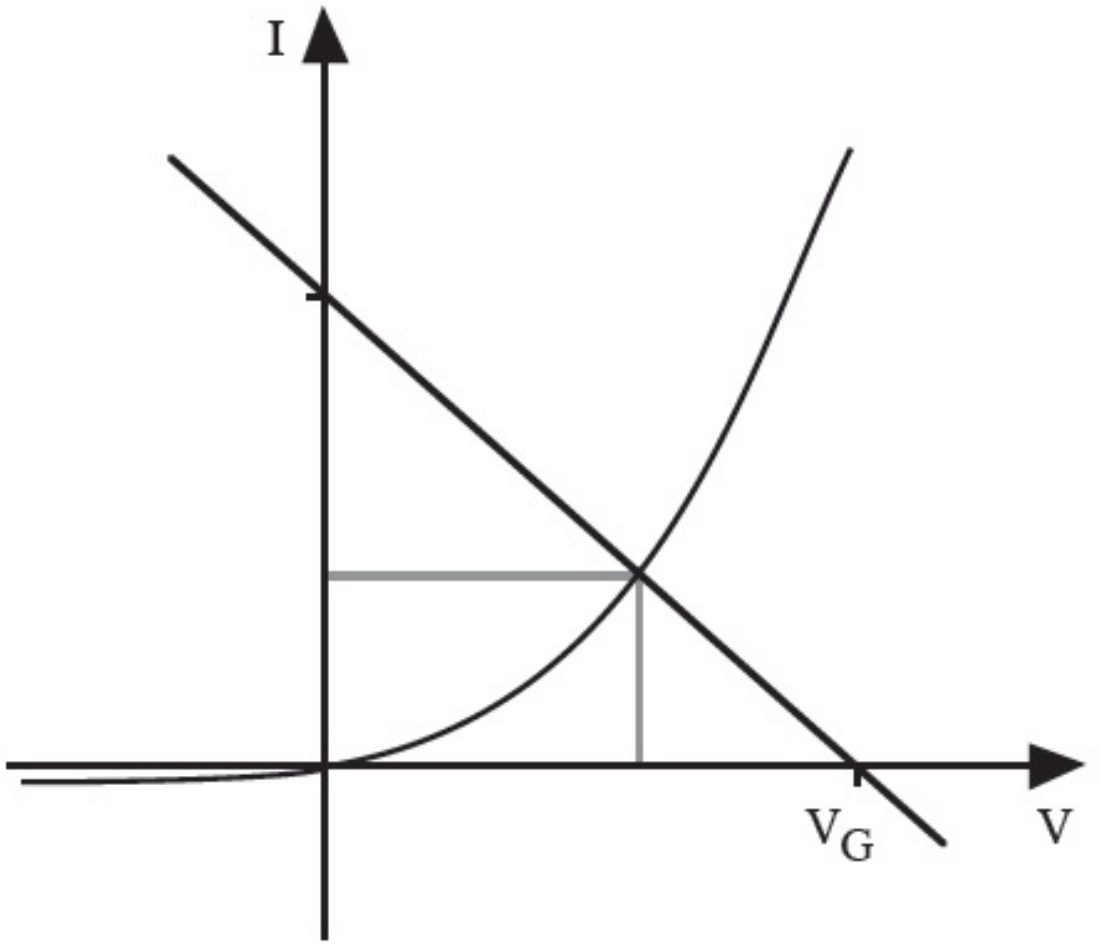
A. A. 2021-22

Soluzione di problemi non lineari in elettronica: il metodo della retta di carico



$$\begin{cases} V_G = IR + V_d \\ V_d = I_c R_c \\ I = I_d + I_c \\ V_d = V_d(I_d) \end{cases}$$

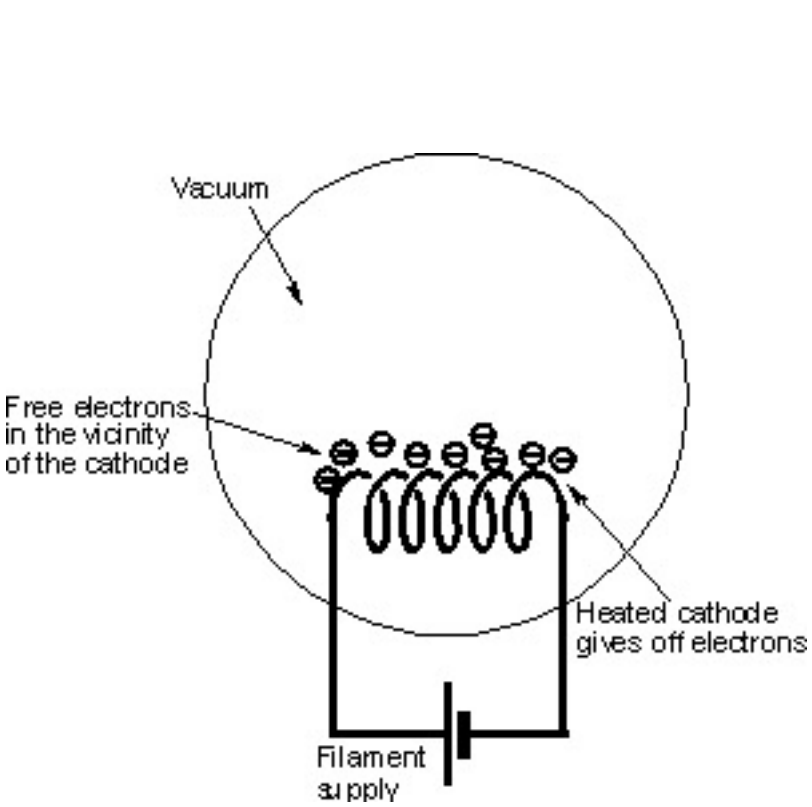
$$\begin{cases} V_G = I_d R + V_d\left(1+\dfrac{R}{R_c}\right) \\ V_d = V_d(I_d) \end{cases}$$

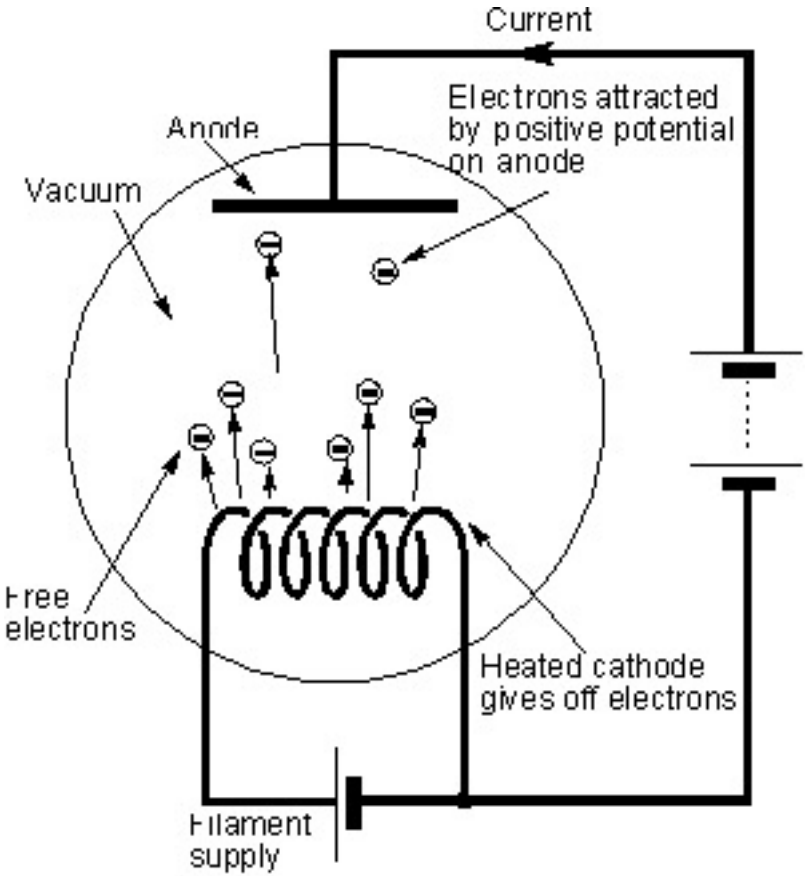


Gli inventori del transistor bipolare (premi Nobel nel 1956): da sinistra; e John Bardeen, William P. Shockley, e Walter H. Brattain (il primo ha vinto un secondo premio Nobel nel 1972 insieme a Cooper e Schrieffer per la teoria della superconduttività).

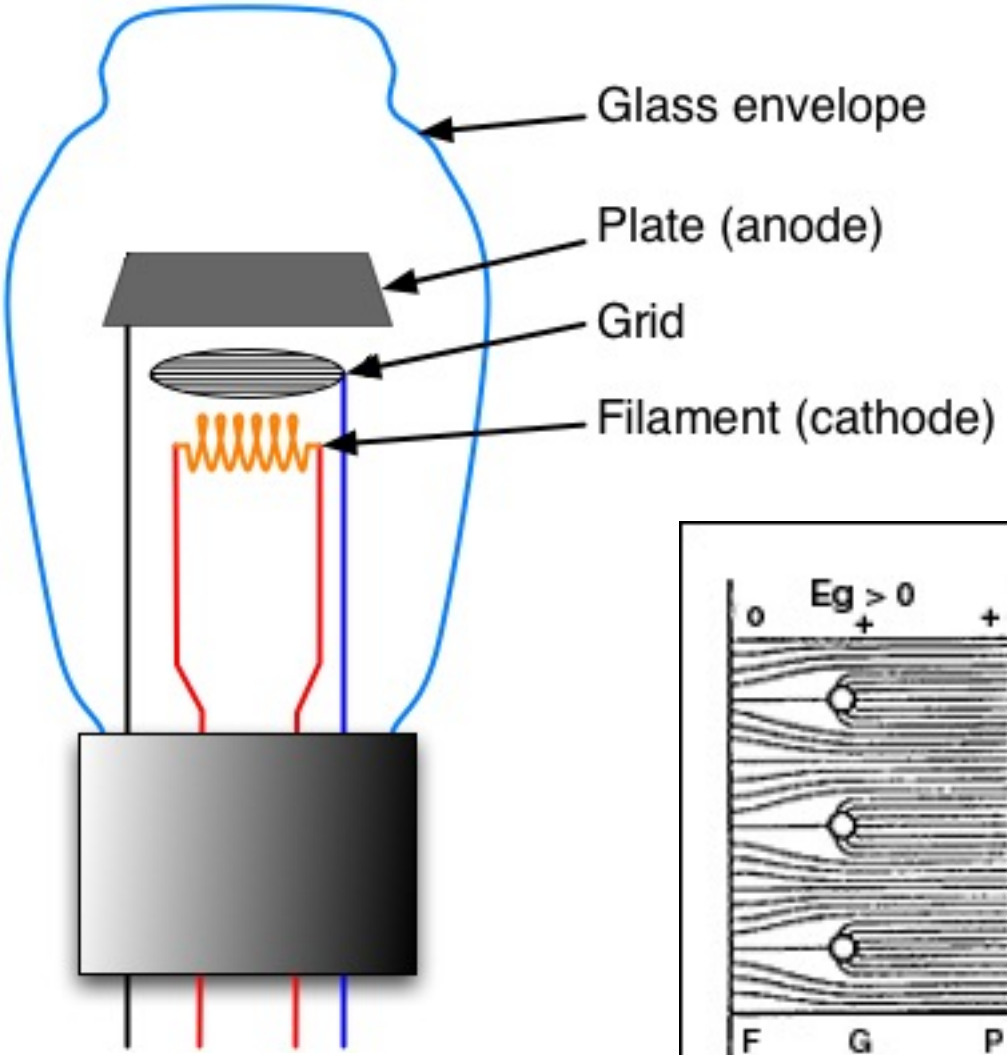

microelectronics group
A replica of the first transistor,
invented at Bell Labs,
December 23, 1947
Lucent Technologies
Bell Labs Innovations
50 Years and Counting...

Diodo a vuoto





Triodo



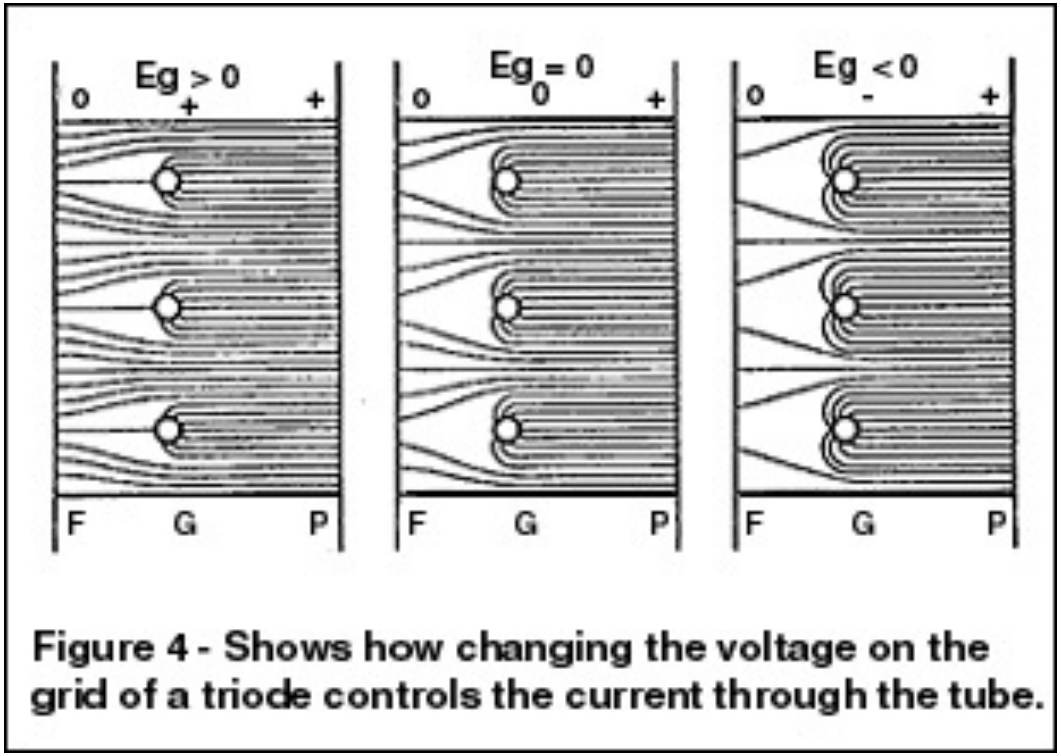
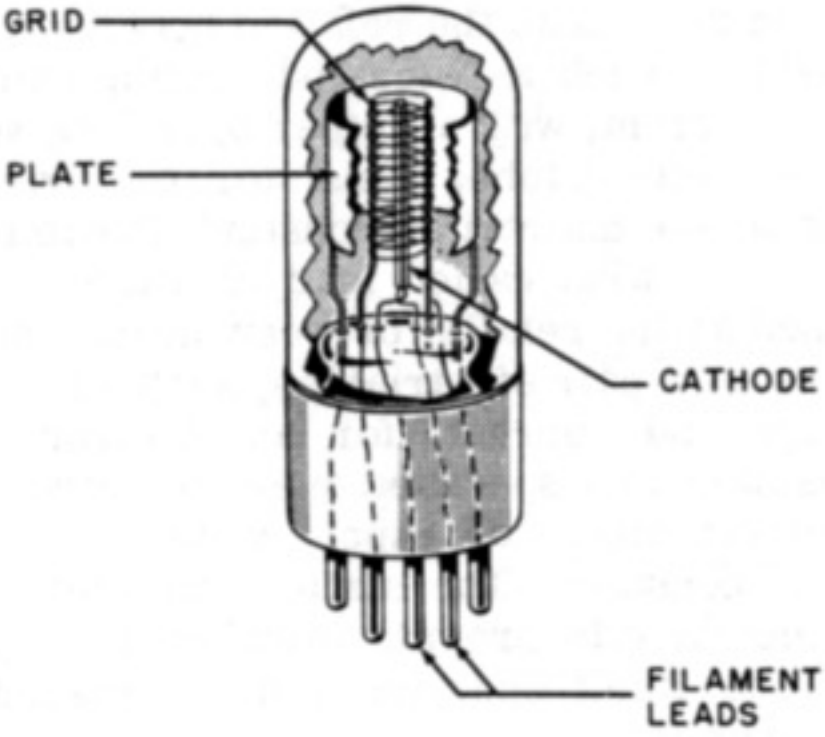
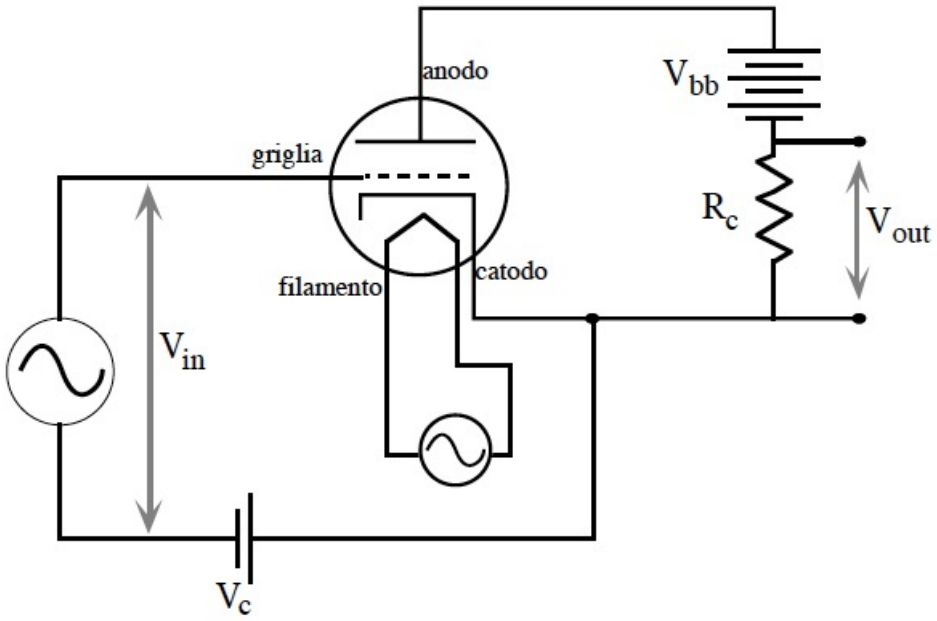
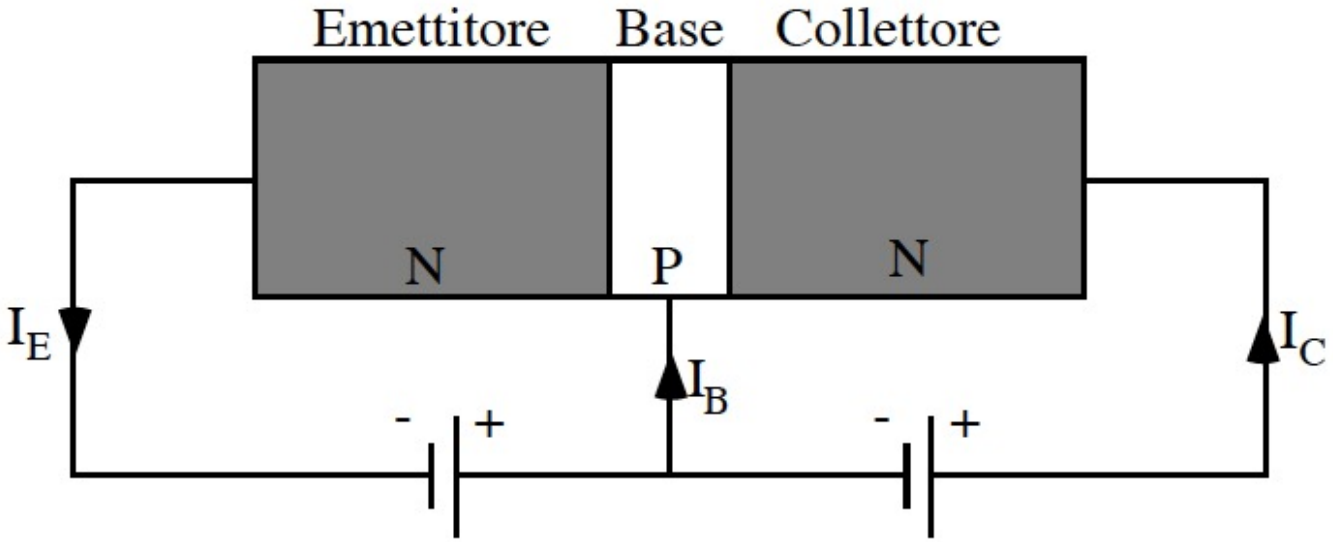


Figure 4 - Shows how changing the voltage on the grid of a triode controls the current through the tube.

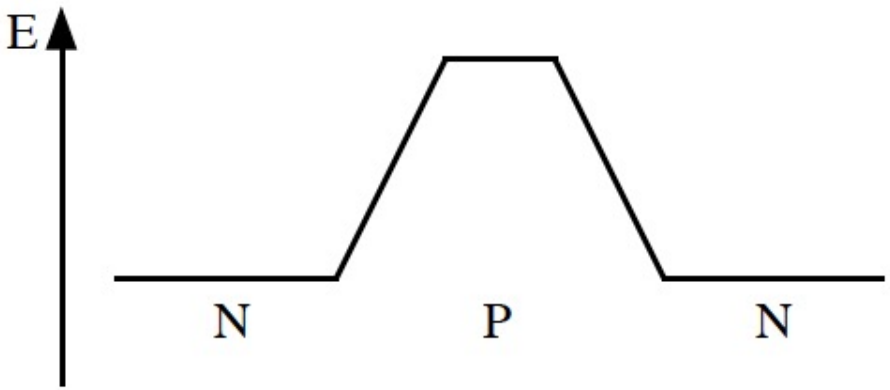

GRID
PLATE
CATHODE
FILAMENT
LEADS

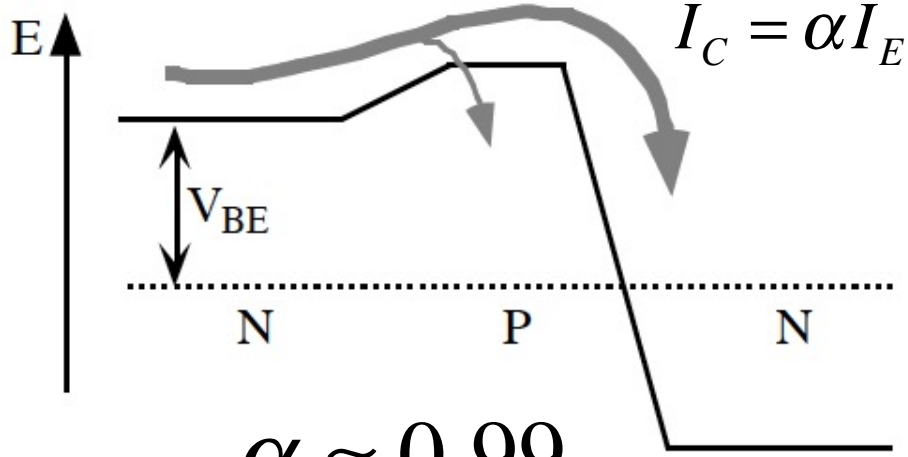

anodo
griglia
filamento
catodo
V_{bb}
R_c
V_{out}
V_{in}
V_c


EZ80
MADE IN HOLLAND

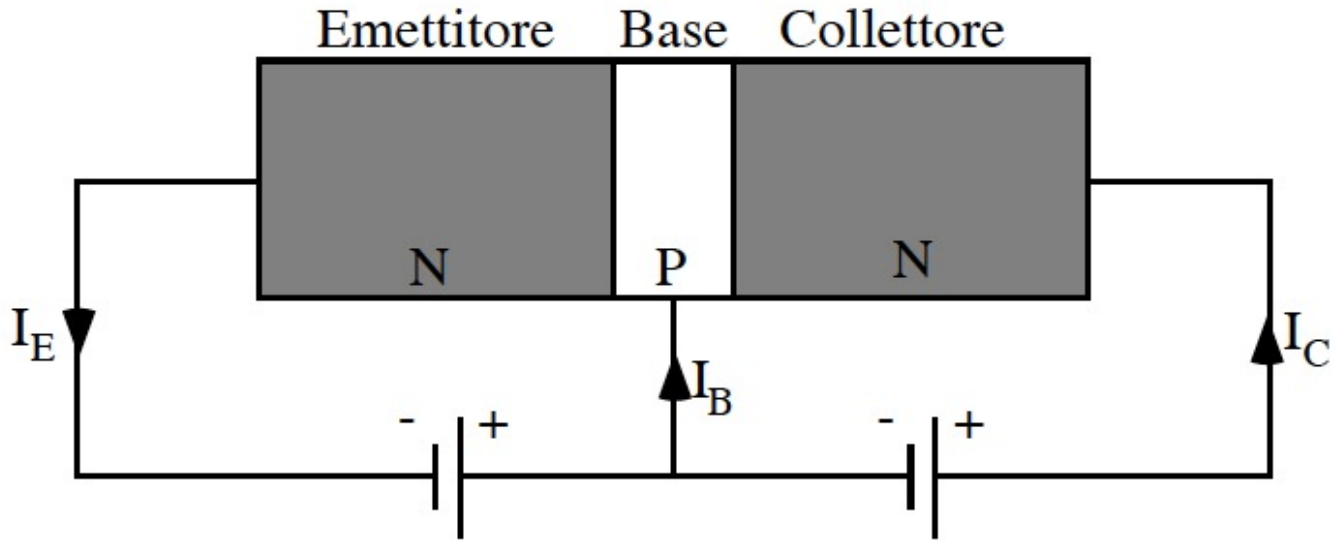


Buona parte della corrente di emettitore va nel collettore



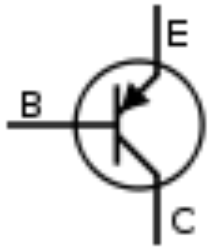


$$\alpha \approx 0.99$$

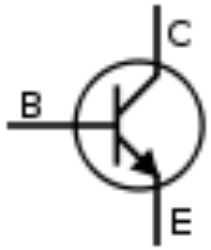


$$I_E = I_B + I_C \quad \text{e inoltre} \quad I_C = \alpha I_E$$

$$\Rightarrow \quad I_E = \frac{1}{1-\alpha} I_B \quad \text{e} \quad I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B$$



transistor bipolare
PNP

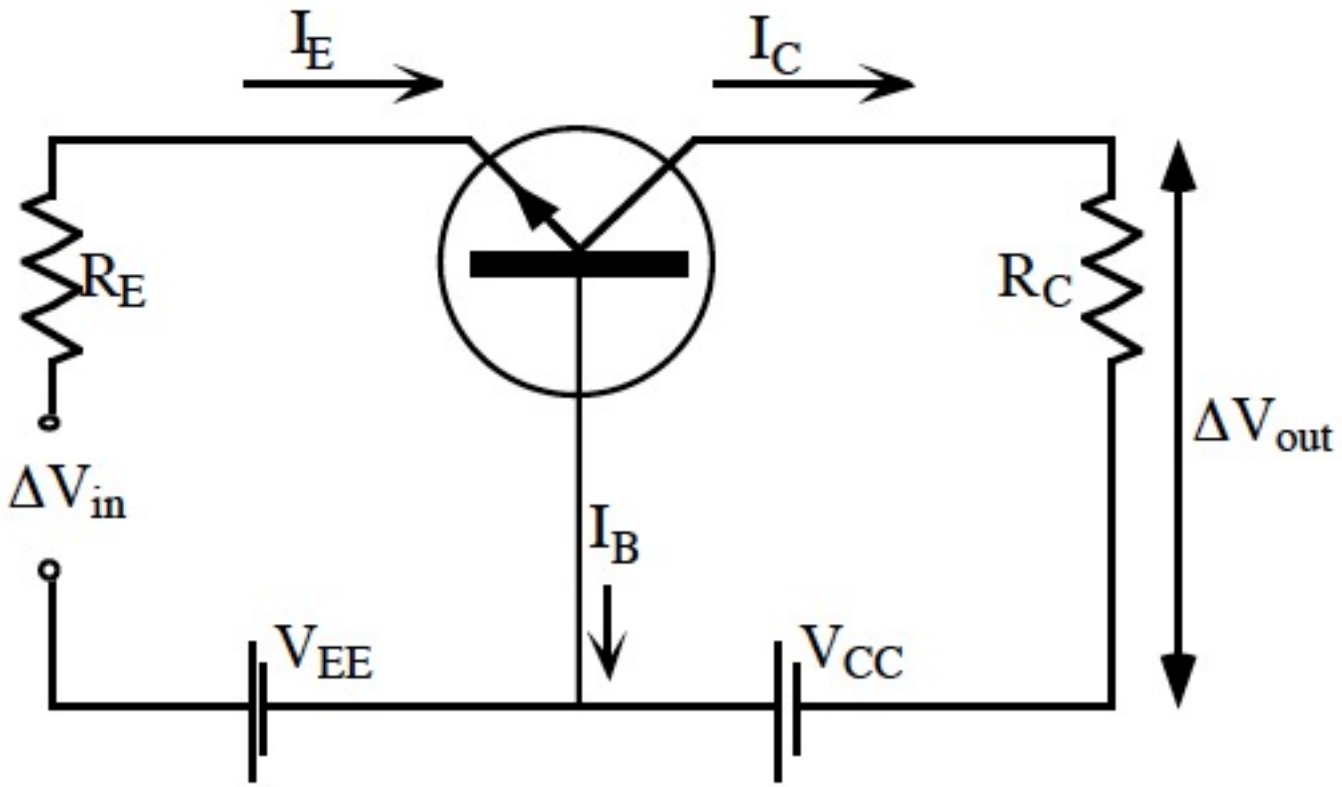


transistor bipolare
NPN

Le regole basilari del funzionamento dei transistor *npn* sono le seguenti:

1. Il collettore deve essere "più positivo" dell'emettitore
2. Le giunzioni base-emettitore e base collettore sono due diodi (e quindi $V_B \approx V_E + 0.6$ Volt)
3. I_B, I_C, I_E hanno dei valori massimi che non possono superare, pena la distruzione del transistor
4. $$I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B$$

Configurazione a base comune



$$\Delta V_{in} + V_{EE} = R_E I_E + V_{BE}$$

$$V_{out} = R_C I_C$$

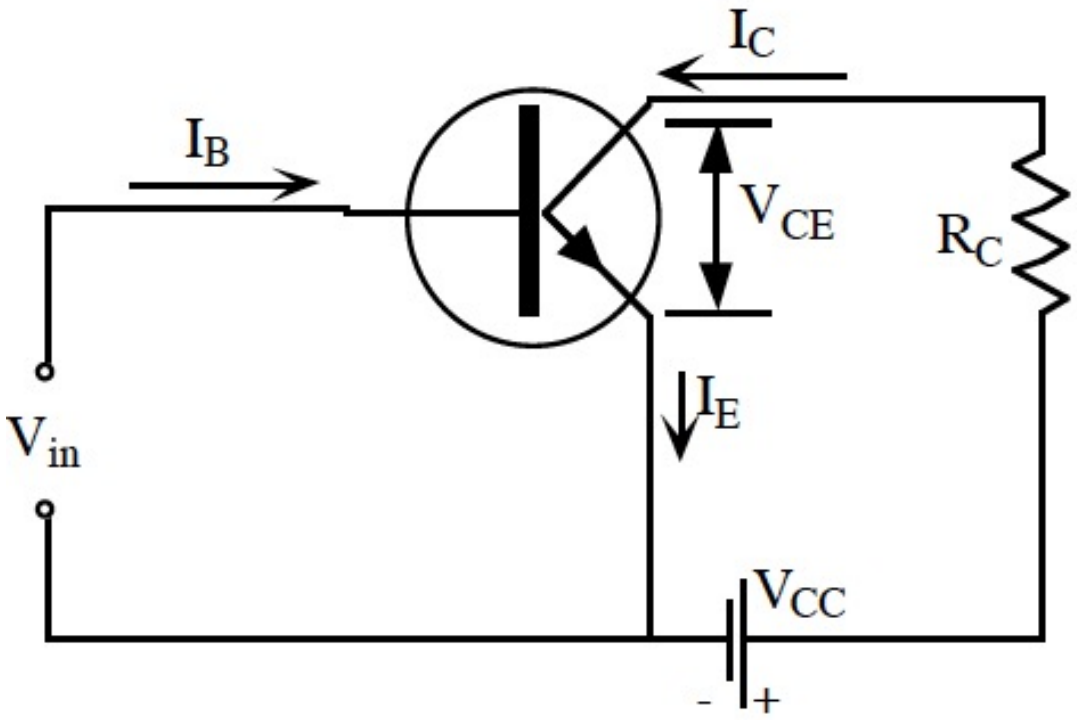
$$R_C I_C - V_{BC} = V_{CC}$$

$$I_C = I_E - I_B = \alpha I_E$$

$$\Delta I_C = \alpha \Delta I_E = \alpha \frac{\Delta V_{in}}{R_E}$$

$$\Delta V_{out} = R_C \Delta I_C = \alpha \frac{R_C}{R_E} \Delta V_{in}$$

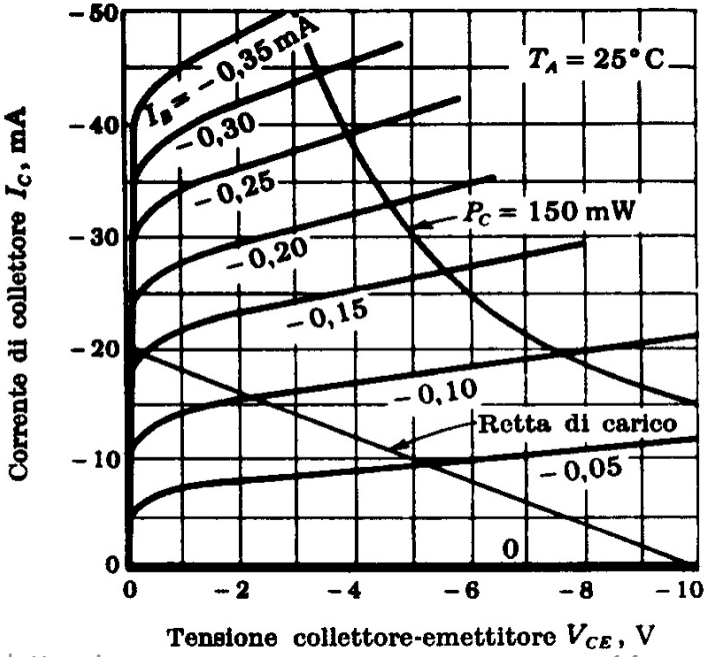
Configurazione a emettitore comune e curve caratteristiche



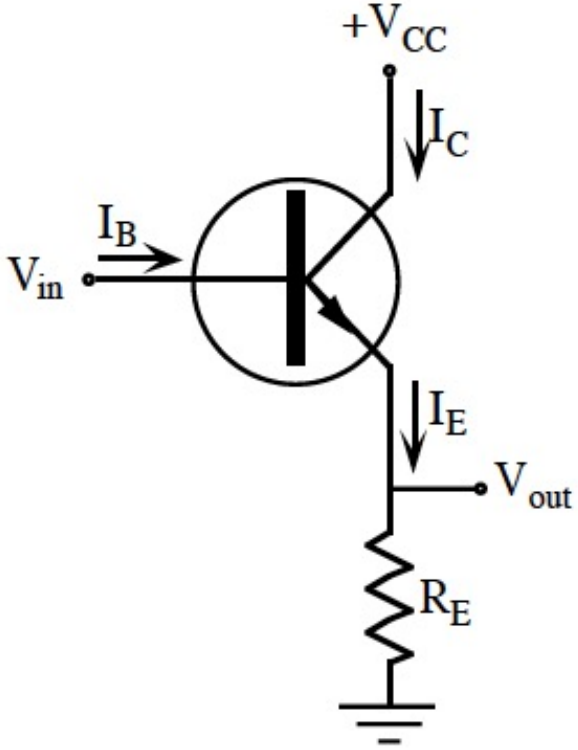
$$V_{CC} = V_{CE} + I_C R_C$$

$$I_C = I_C\left(I_B, V_{CE}\right)$$

soluzione con il metodo della retta di carico



Emitter follower



$$V_{in} - V_{out} = V_{BE} \approx 0.6V$$

$$I_E = I_B + I_C = (1+\beta) I_B$$

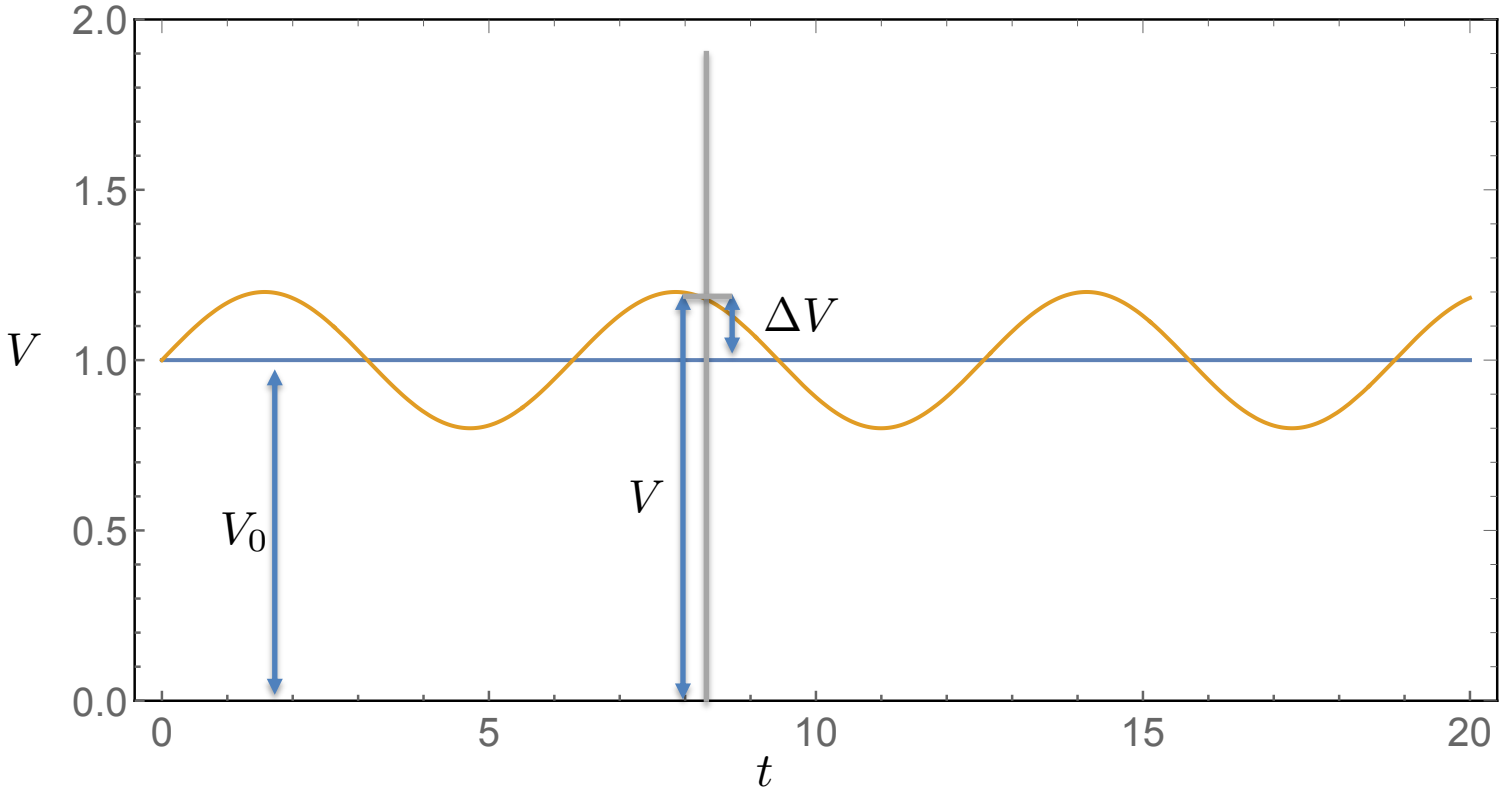
$$\Delta V_{in} \approx \Delta V_{out}$$

$$\Delta I_E = (1+\beta) \Delta I_B$$

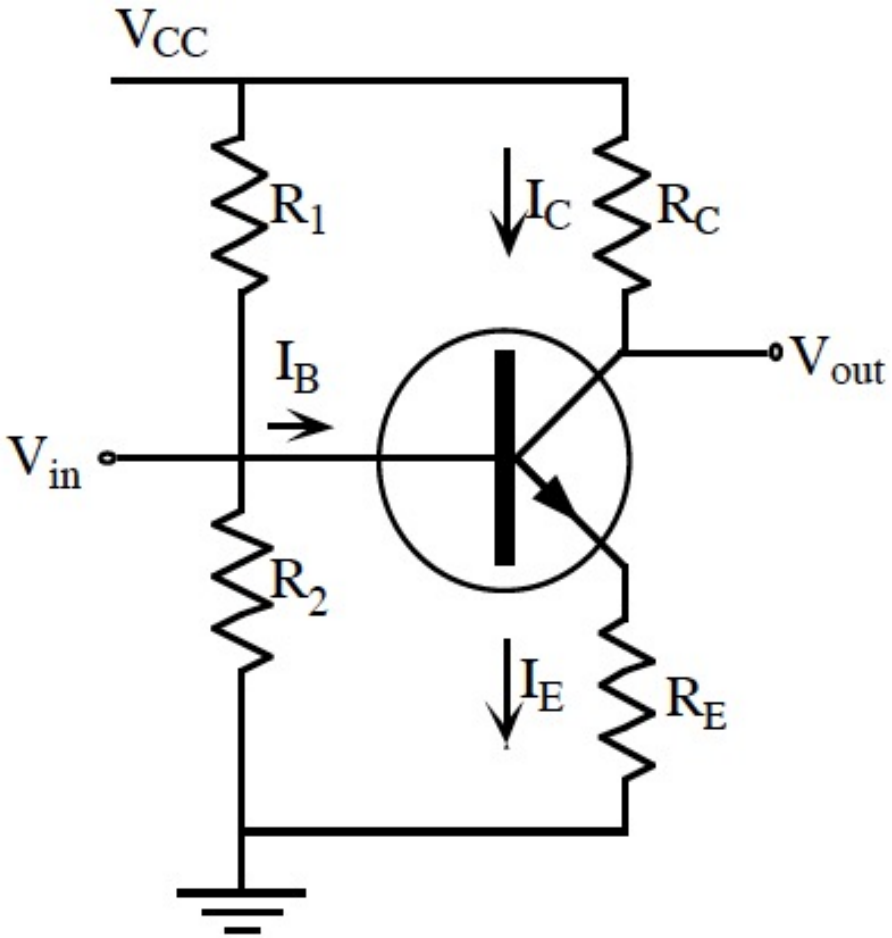
$$Z_{in} = \frac{\Delta V_{in}}{\Delta I_B} \approx (1+\beta) \frac{\Delta V_{out}}{\Delta I_E} = (1+\beta) Z_{out}$$

applicazioni: adattamento di impedenza, aumento della potenza del segnale

Illustrazione della differenza tra quantità statiche e dinamiche



Amplificatore ad emettitore comune



$$V_{out} = V_C = V_{CC} - I_C R_C$$

$$\Delta V_{in} = \Delta V_B \approx \Delta V_E$$

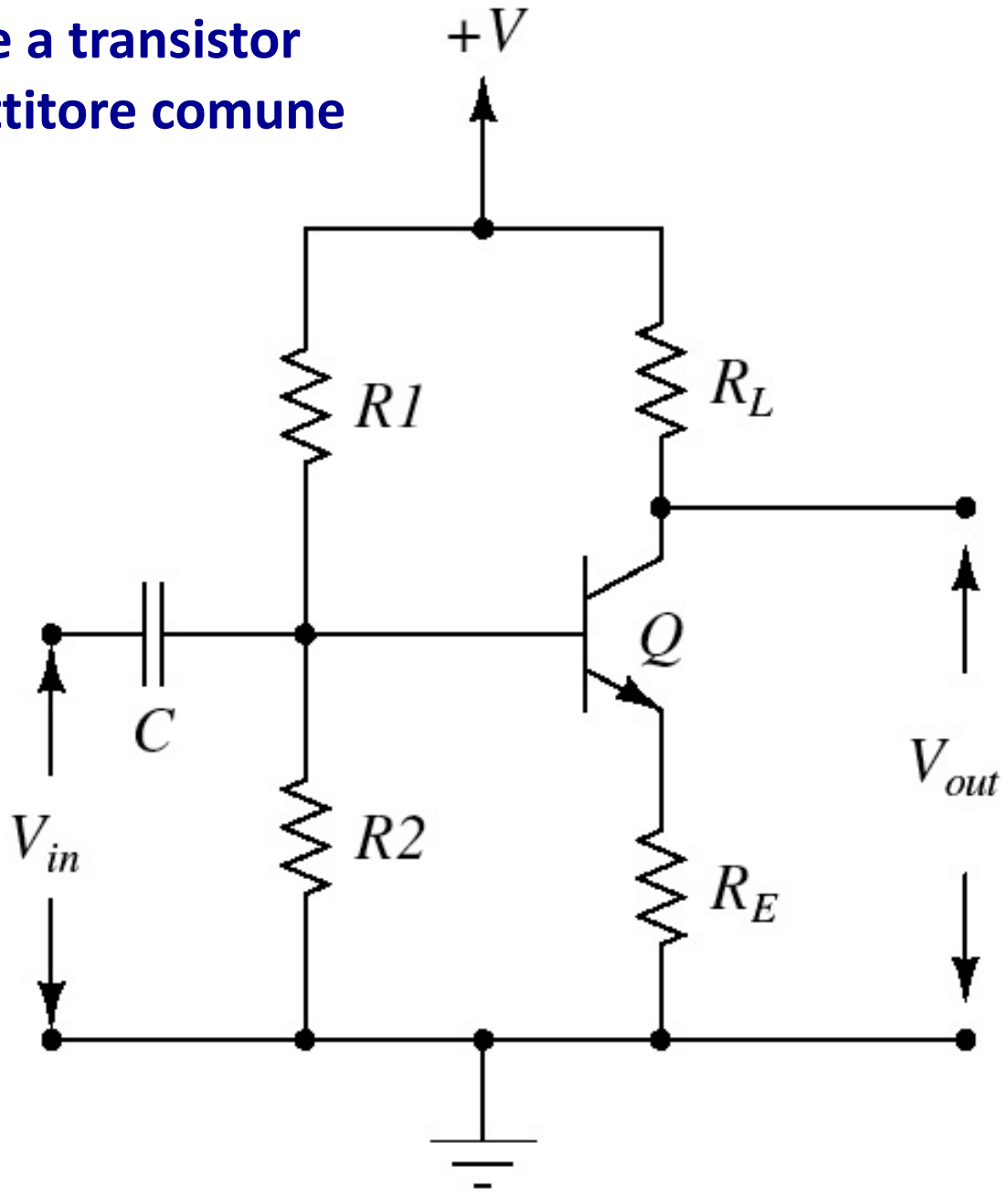
$$\Delta V_E = R_E \Delta I_E \approx R_E \Delta I_C$$

$$\Delta V_{out} = \Delta V_C = -R_C \Delta I_C$$

$$G = \frac{\Delta V_{out}}{\Delta V_{in}} \approx -\frac{R_C}{R_E}$$

amplificatore invertente!

Progetto di un amplificatore a transistor nella configurazione a emettitore comune con un transistor 2N3904



NPN switching transistor 2N3904

FEATURES

- Low current (max. 200 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- High-speed switching.

DESCRIPTION

NPN switching transistor in a TO-92; SOT54 plastic package. PNP complement: 2N3906.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter

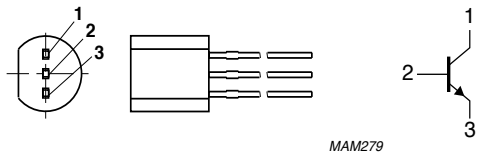


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

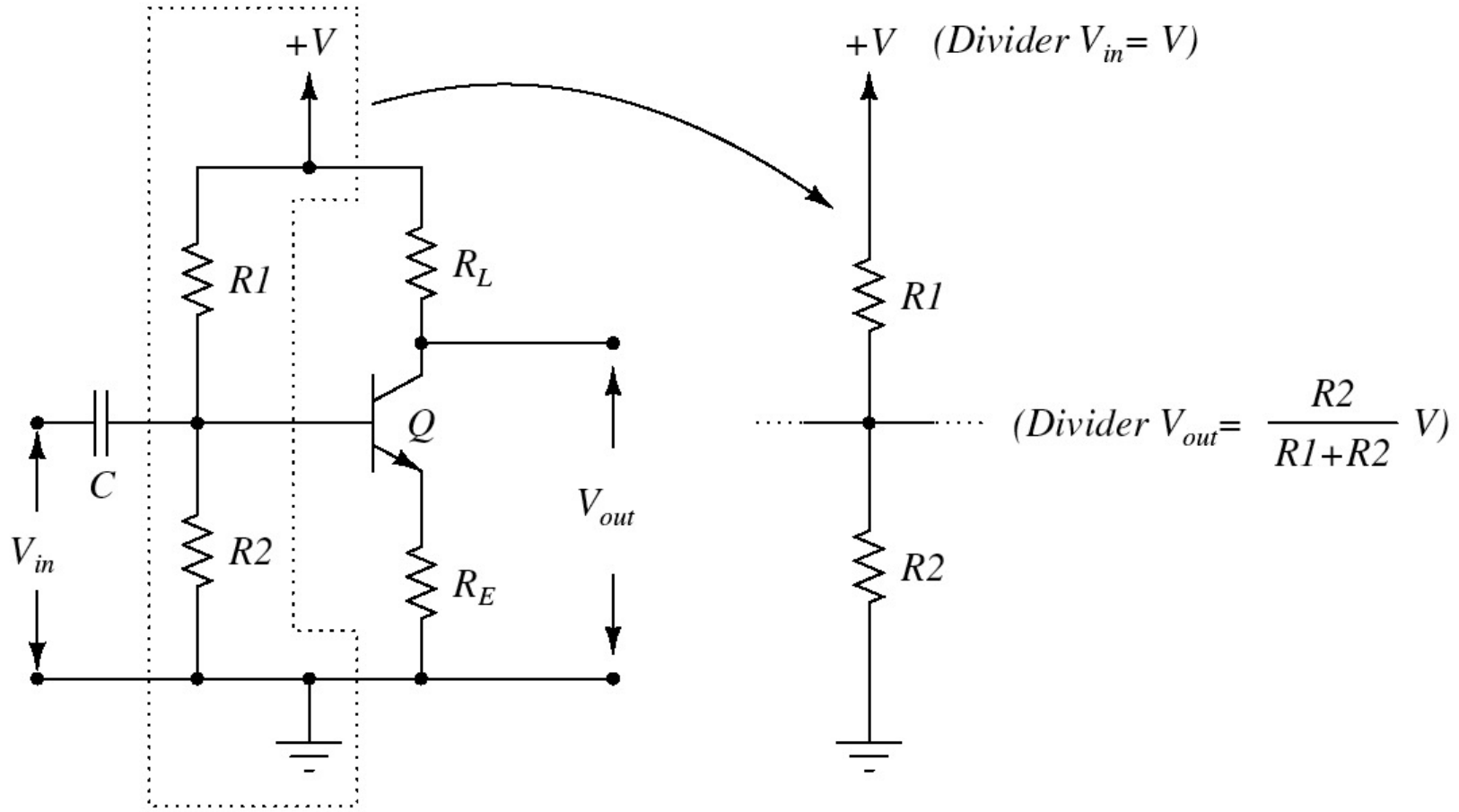
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	200	mA
I_{CM}	peak collector current		–	300	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

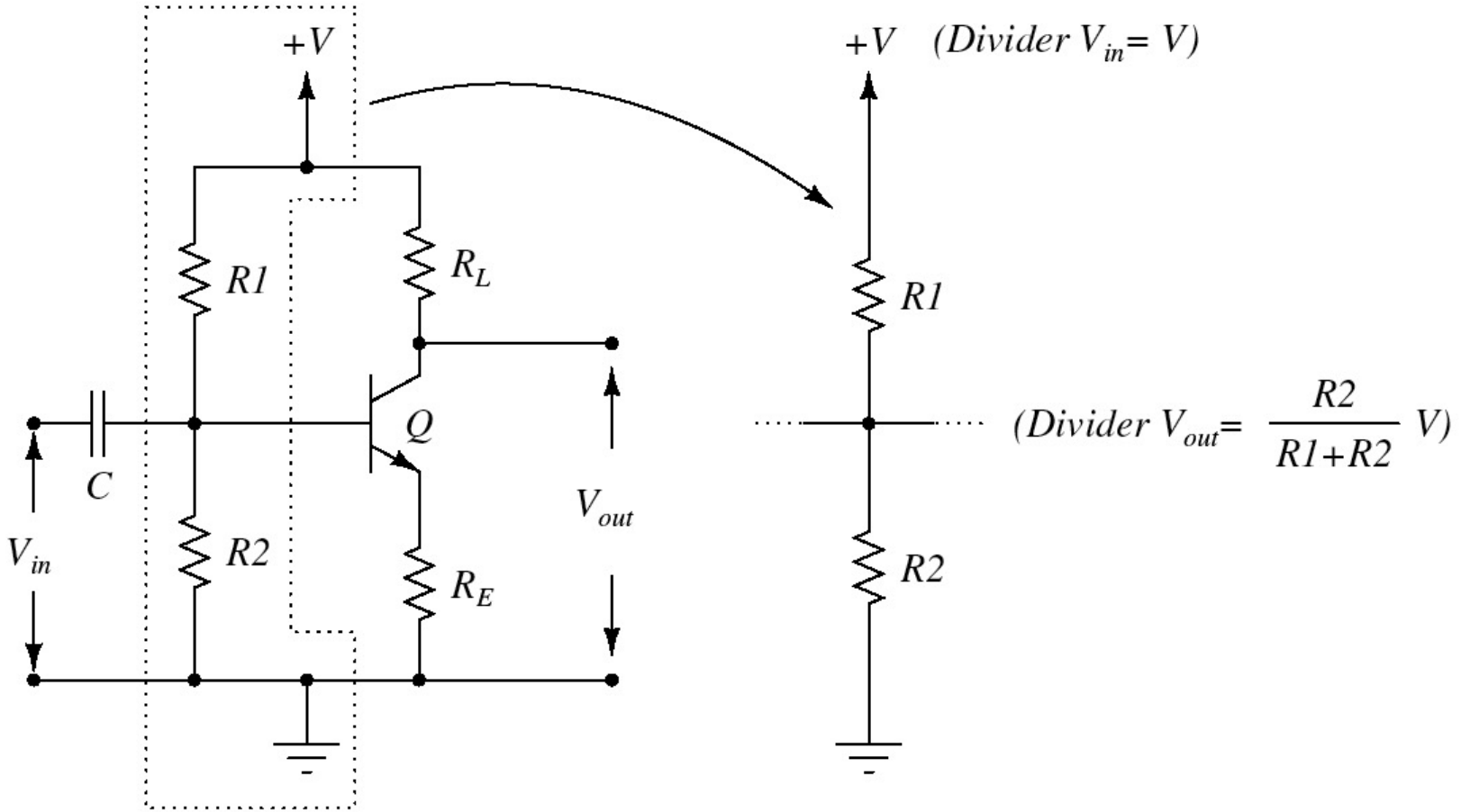
Note

1. Transistor mounted on an FR4 printed-circuit board.



Nel circuito possiamo isolare una parte (segnata nel tratteggio) che rappresenta un partitore che costituisce la rete di polarizzazione della base: la scelta delle resistenze del partitore seleziona il punto di lavoro dell'amplificatore.

In modo del tutto analogo le resistenze R_L, R_E e il transistor costituiscono una specie di partitore con una resistenza variabile (il transistor): la conseguenza è che la tensione di uscita può variare tra 0V e la tensione di alimentazione $+V$.



$$\Delta V_{in} = \Delta V_B \approx \Delta V_E = R_E \Delta I_E \approx R_E \Delta I_C$$

$$\Delta V_{out} = \Delta V_C = -R_L \Delta I_C$$

$$G = \frac{\Delta V_{out}}{\Delta V_{in}} \approx -\left(\frac{R_L}{R_E} \right)$$

Definizione dei parametri del circuito

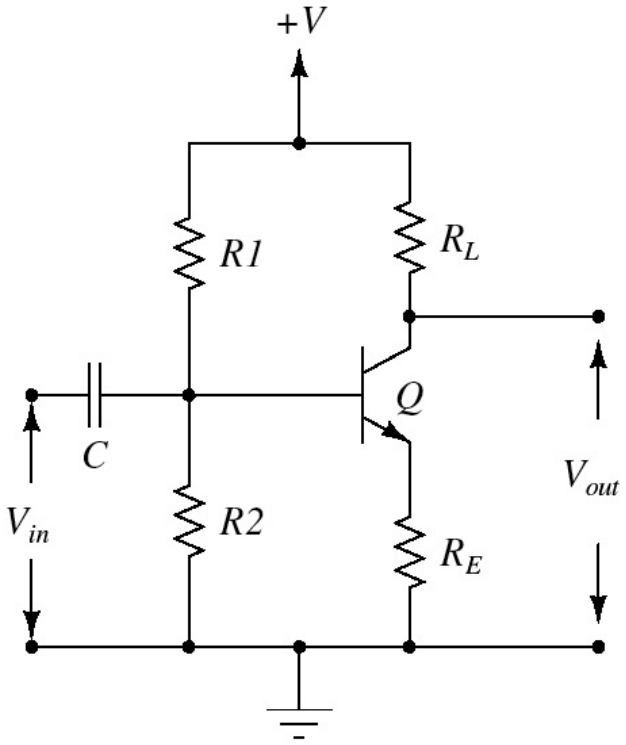
- la prima scelta l'abbiamo già fatta: abbiamo preso una configurazione di amplificatore a emettitore comune.

- a questo punto scegliamo la tensione di alimentazione: come si è visto questo determina l'escursione massima in tensione del segnale amplificato. Questa scelta dipende da molti fattori, tra cui il tipo di alimentatore disponibile e le caratteristiche dei transistor che abbiamo a disposizione: in pratica si tratta sempre di una tensione dell'ordine della decina di volt.
  Noi scegliamo una tensione di 10V che è compatibile con la tensione massima emettitore-collettore di questo transistor (40V) ed è facile da ottenere con gli alimentatori normalmente disponibili in laboratorio.

• **scegliamo ora la corrente quiescente della maglia di uscita.** *Questa corrente viene determinata a partire dalle caratteristiche del transistor.* In questo caso la corrente di collettore massima accettabile è di 200 mA, mentre la dissipazione termica massima è di 500 mW. Così con una tensione (massima) emettitore-collettore di 10V si ottiene la dissipazione (massima) di 0.5W con una corrente di 50 mA.

Questo sta all'interno del limite di 200 mA, ma è una corrente piuttosto alta se prendiamo delle resistenze di polarizzazione dell'ordine del kOhm (non possiamo prendere delle resistenze troppo piccole se non vogliamo che un carico tra quelli ordinariamente disponibili modifichi eccessivamente la rete di polarizzazione del transistor). *Infatti la dissipazione di potenza su 1 kOhm diventa in questo caso 2.5 W, una potenza piuttosto elevata, che comporta l'utilizzo di componenti meccanicamente piuttosto grandi.*

Se vogliamo utilizzare le normali resistenze da 1/4 W o da 1/2 W, dobbiamo abbassare la corrente: prendiamo un valore più piccolo, I_C = 4 mA. Con questa corrente il "partitore" di uscita (transistor + resistenza di emettitore) si comporta in modo che la resistenza equivalente totale sia 10V/4mA = 2.5 kOhm. La tensione quiescente di uscita viene posta allora a V/2 (= 5V) se si prende R_L = 2.5 kOhm /2 = 1.25 kOhm.



È buona pratica prendere la resistenza di emettitore grande almeno $R_L/10$: qui noi prendiamo $R_E=R_L/3$, vale a dire $R_E \approx 417$ Ohm. Questo significa che l'amplificatore ha guadagno G=3 e che la tensione di emettitore è

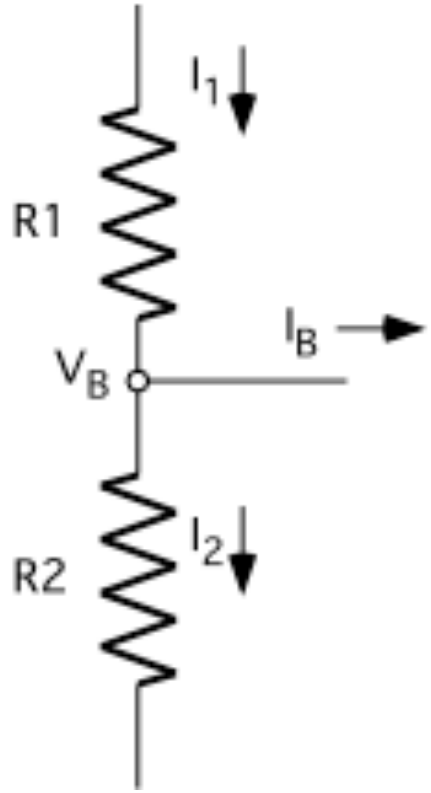
$$V_E \approx 417\Omega \cdot 4\text{mA} \approx 1.7V$$

e la tensione di base è circa 0.6V più alta, vale a dire circa $V_B \approx 2.3V$.

• per completare la scelta delle resistenze dobbiamo determinare i valori delle resistenze R1 e R2: per farlo in modo corretto dovremmo conoscere l'esatto valore di *beta* del nostro transistor, ma dal datasheet si trova che esso varia tipicamente tra 70 e 300, e per questo noi prendiamo il valore *beta* = 100.

Questo vuol dire che la corrente di base è 100 volte più piccola della corrente di collettore, e quindi vale 40µA.

La figura mostra come si divide la corrente nel partitore di ingresso; devono valere quindi le seguenti equazioni:



$$I_1 = I_2 + I_B$$

$$I_1 R_1 = V - V_B$$

$$I_2 R_2 = V_B$$

$$I_1 = \frac{V_B}{R_2} + I_B$$

$$I_1 = \frac{V - V_B}{R_1}$$

$$I_2 = \frac{V_B}{R_2}$$

Il sistema non si può risolvere per trovare le correnti e le resistenze a meno che non si imponga una condizione aggiuntiva. Adesso però si può notare che la corrente nella resistenza R_2 deve essere molto maggiore della corrente di base, in modo che un cambiamento della corrente di base non influenzi il comportamento della rete: prendiamo dunque $I_2 = 10\, I_B$, allora

$$I_1 = \frac{V_B}{R_2} + I_B$$

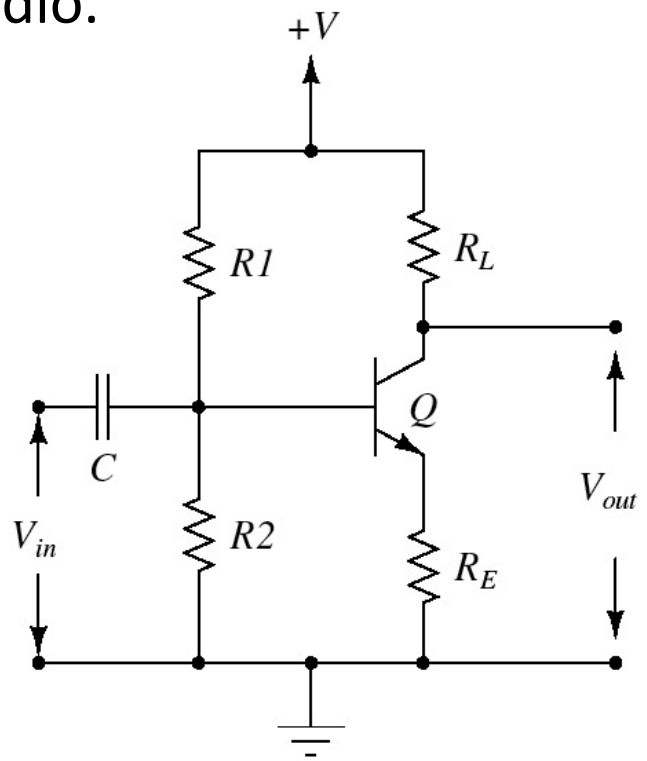
$$I_1 = \frac{V - V_B}{R_1}$$

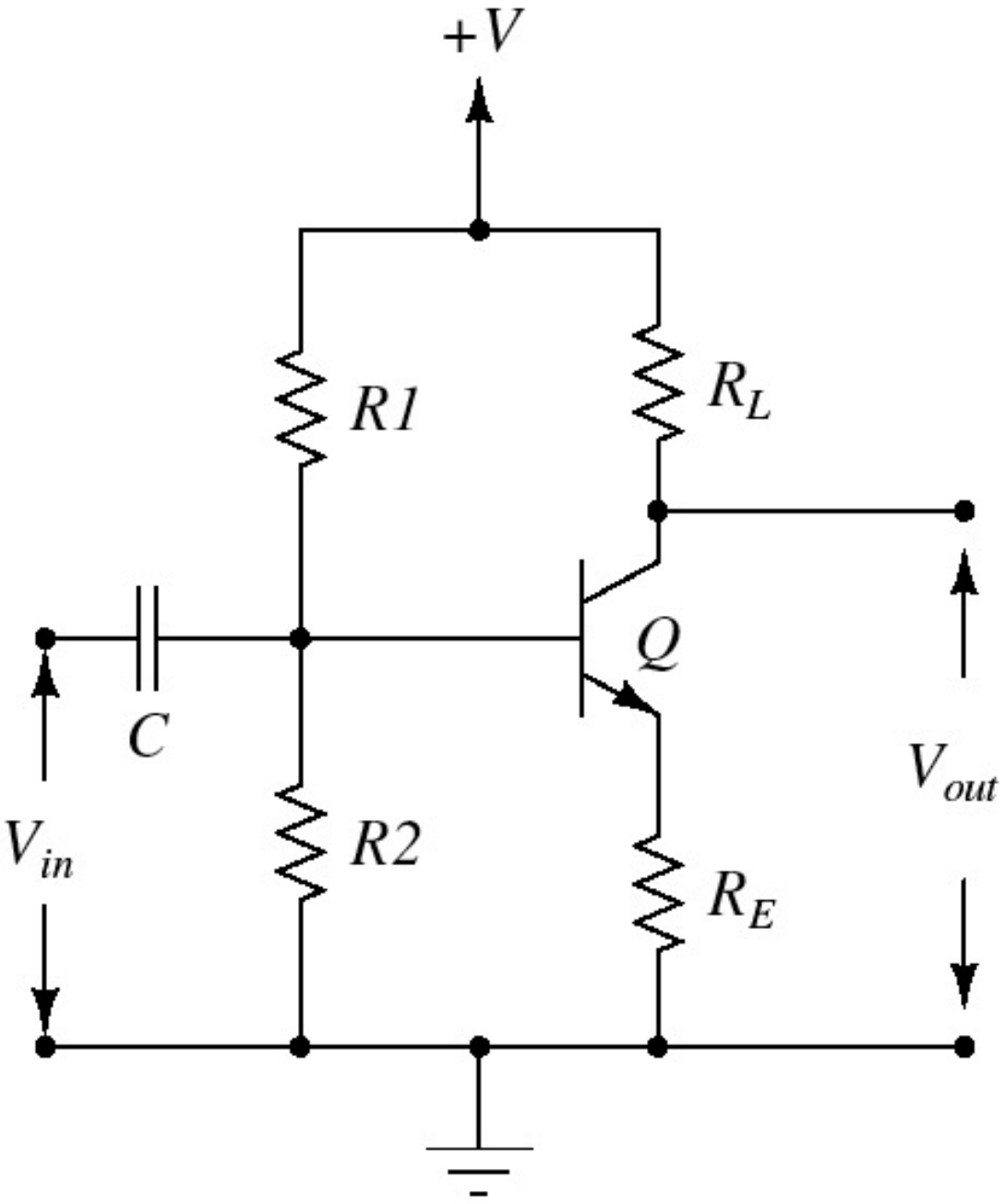
$$I_2 = \frac{V_B}{R_2}$$

$$\frac{V_B}{R_2} \approx \frac{2.3V}{R_2} \approx 0.4mA; \quad R_2 \approx 5.75k\Omega$$

$$I_1 \approx 0.44mA \approx \frac{V - V_B}{R_1} = \frac{10V - 2.3V}{R_1} = \frac{7.7V}{R_1}; \quad R_1 \approx 17.5k\Omega$$

• la scelta del condensatore di disaccoppiamento dipende dalla resistenza R2 (che mette a terra il segnale in ingresso): insieme il condensatore e R2 costituiscono un filtro RC passa alto con una frequenza di taglio $1/R_2C$; ad esempio, se si prende un comune condensatore (non polarizzato) da 4.7 µF si ottiene una frequenza di taglio di 12 Hz; questa frequenza è adeguata per un amplificatore audio.

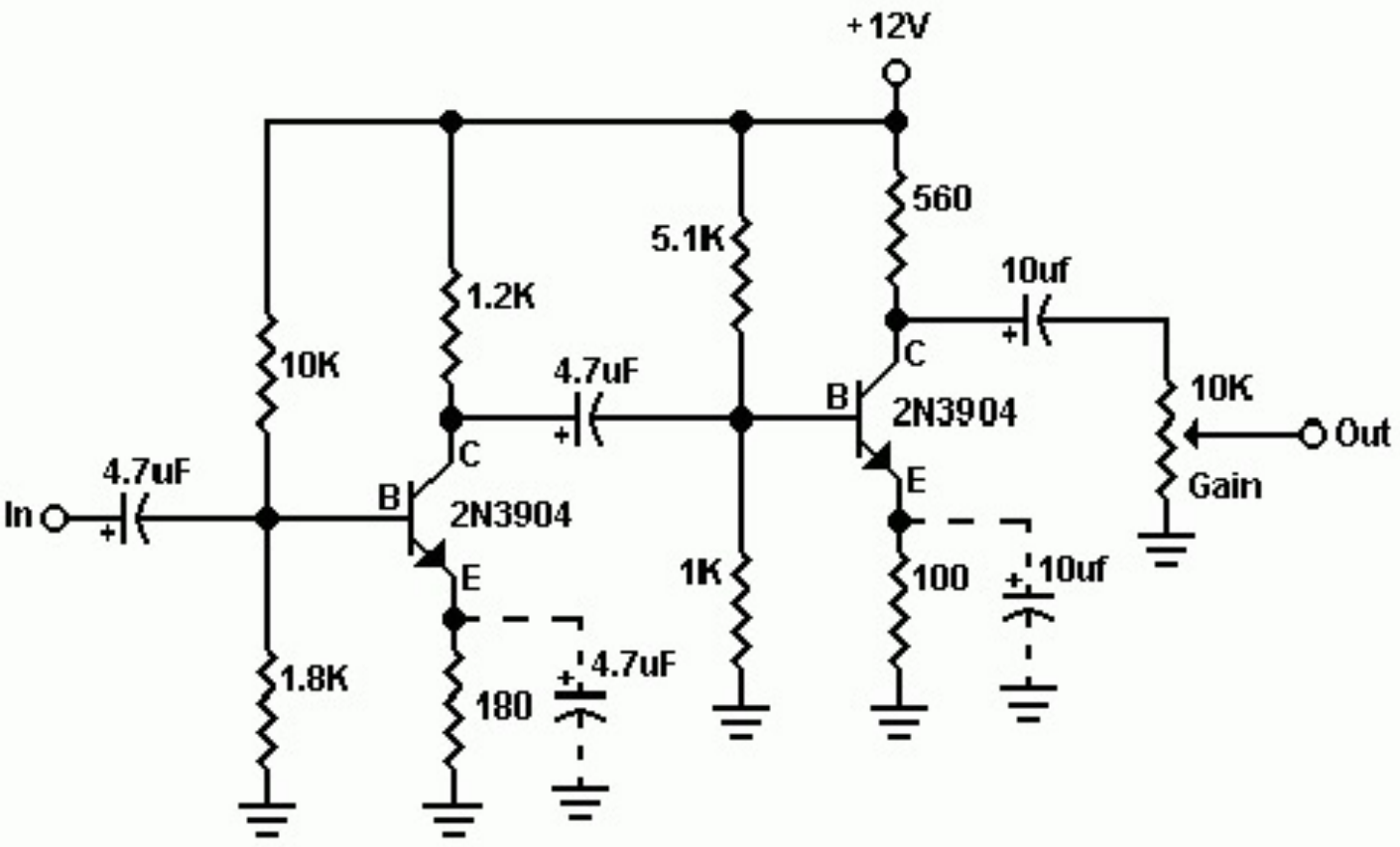




R_1 = 18 kΩ
R_2 = 6 kΩ
R_L = 1.25 kΩ
R_E = 420 Ω
C = 4.7 µF

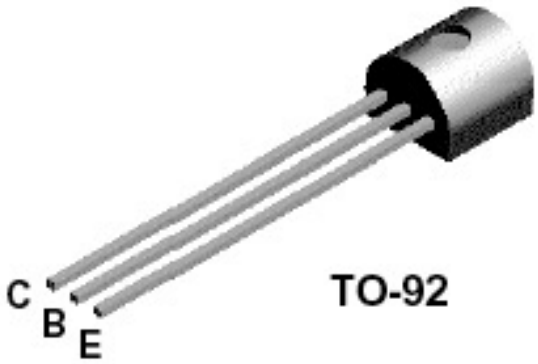
Q = 2N3904

L’amplificazione non è elevata e potrebbe essere necessario aggiungere degli ulteriori stadi di amplificazione, come nella figura seguente, simile al circuito che abbiamo discusso, che mostra due emitter follower in cascata



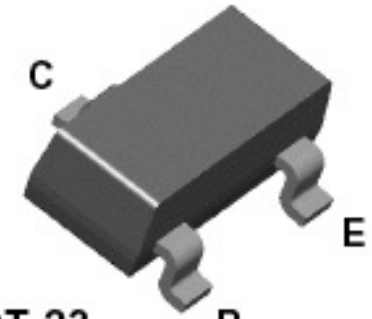
FAIRCHILD
SEMICONDUCTOR™

2N3904



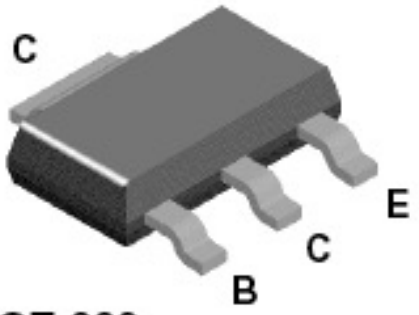
TO-92

MMBT3904



SOT-23
Mark: 1A

PZT3904



SOT-223

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

NGSPICE

MIXED MODE - MIXED LEVEL CIRCUIT SIMULATOR

BASED ON BERKELEY'S SPICE3F5

NGSPICE SUMMARY

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- F.A.Q.
- Tutorials

Sourceforge Developer Pages

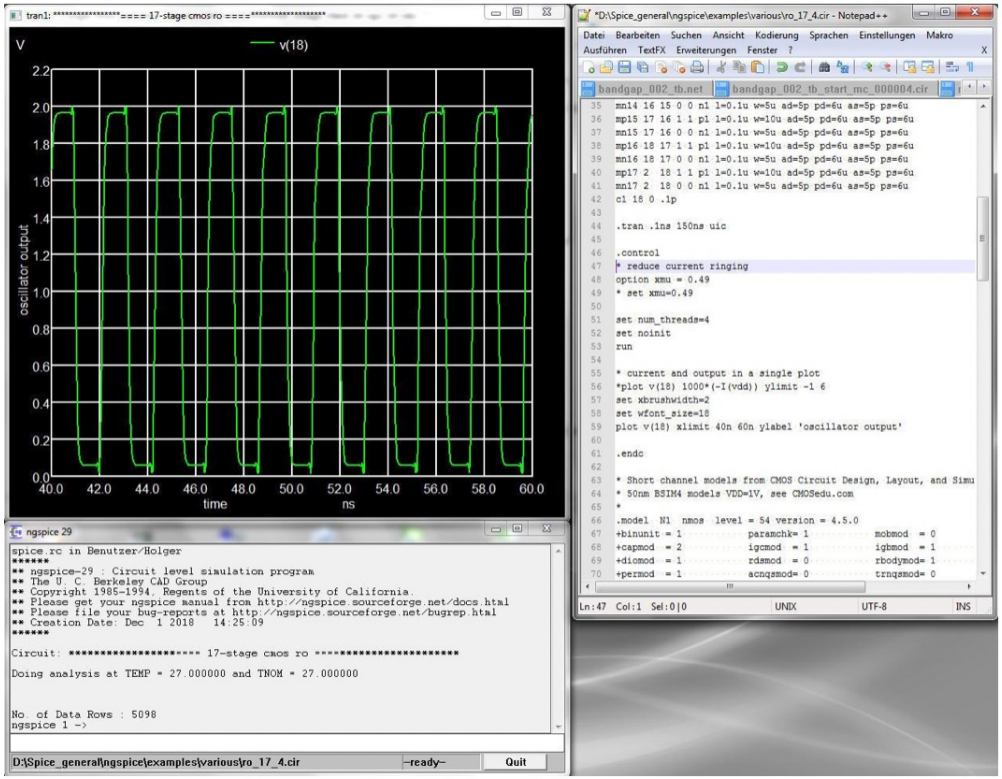
ngspice - open source spice simulator

ngspice is the open source spice simulator for electric and electronic circuits.

Such a circuit may comprise of JFETs, bipolar and MOS transistors, passive elements like R, L, or C, diodes, transmission lines and other devices, all interconnected in a netlist. Digital circuits are simulated as well, event driven and fast, from single gates to complex circuits. And you may enter the combination of both analog and digital as a mixed-signal circuit.

ngspice offers a wealth of device models for active, passive, analog, and digital elements. Model parameters are provided by our collections, by the semiconductor device manufacturers, or from semiconductor foundries. The user adds her circuits as a netlist, and the output is one or more graphs of currents, voltages and other electrical quantities or is saved in a data file.

ngspice does not provide schematic entry. Its input is command line or file based. There are however third party interfaces available.



https://www.macspice.com

MacSpice 3

by Charles D. H. Williams

Introduction

MacSpice simulates and analyses electronic circuits that can range in complexity from a single resistor to an integrated circuit comprising tens-of-thousands of devices. It has users who range in experience from novices to retired integrated circuit designers. It is used at various universities internationally for research and teaching.

MacSpice runs on Intel architecture Apple Macintosh computers. It is compatible with, Berkeley Spice 3f5 but incorporates many improvements to Spice 3f5 – from simple bug-fixes to entirely new commands, algorithms and solution strategies. For example: the memory leaks that affected Spice 3f5 have been cured; new algorithms have been developed to facilitate the simulation of large circuits, and to reduce simulation time; MacSpice provides a robust multi-parameter optimizer and facilities for inter-process communication with other applications.

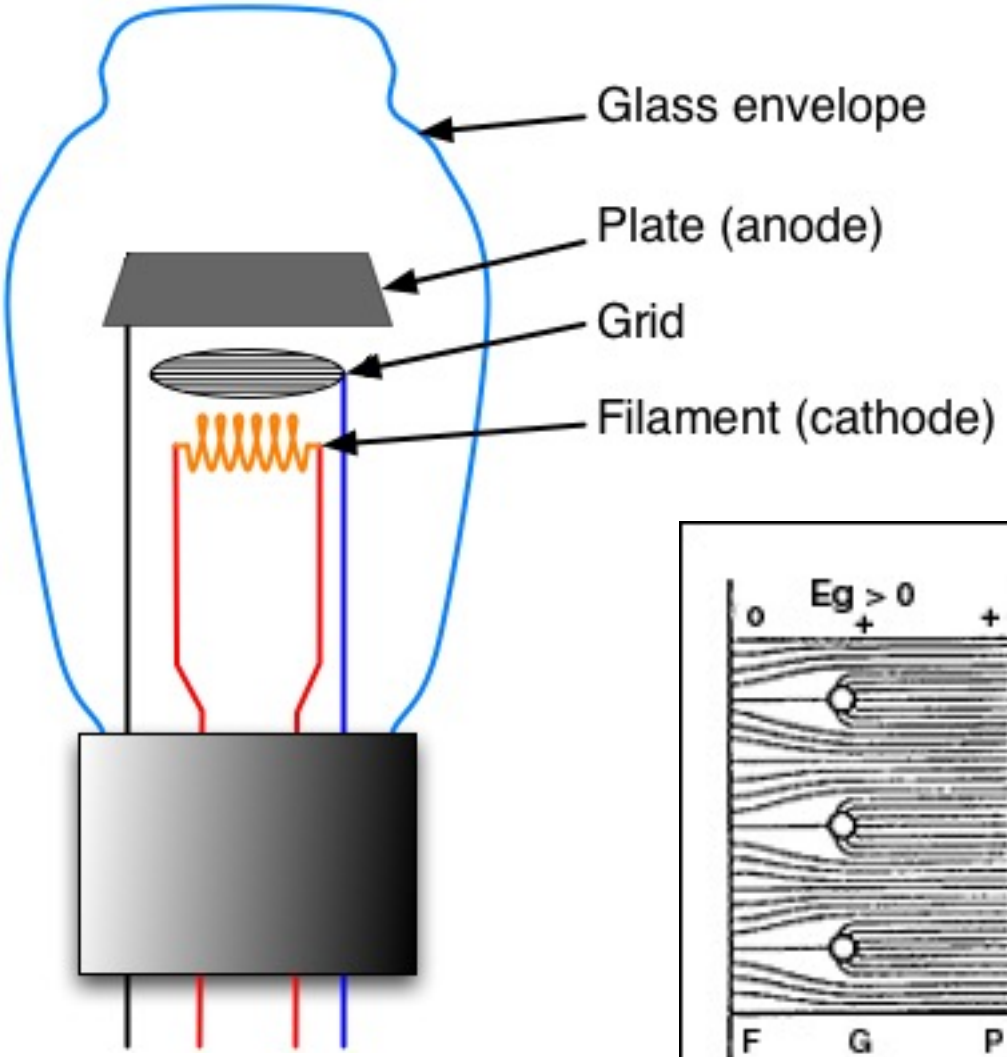
Spice models

File per il transistor 2N3904

```
*               Model for 2N3904 NPN BJT (from Eval library in Pspice)
.model Q2N3904  NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259
+               Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+               Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+               Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
```

Idea per possibile presentazione per l'esame... utilizzare Spice con i modelli di resistenze, condensatori e transistor per costruire una simulazione del circuito amplificatore

Triodo



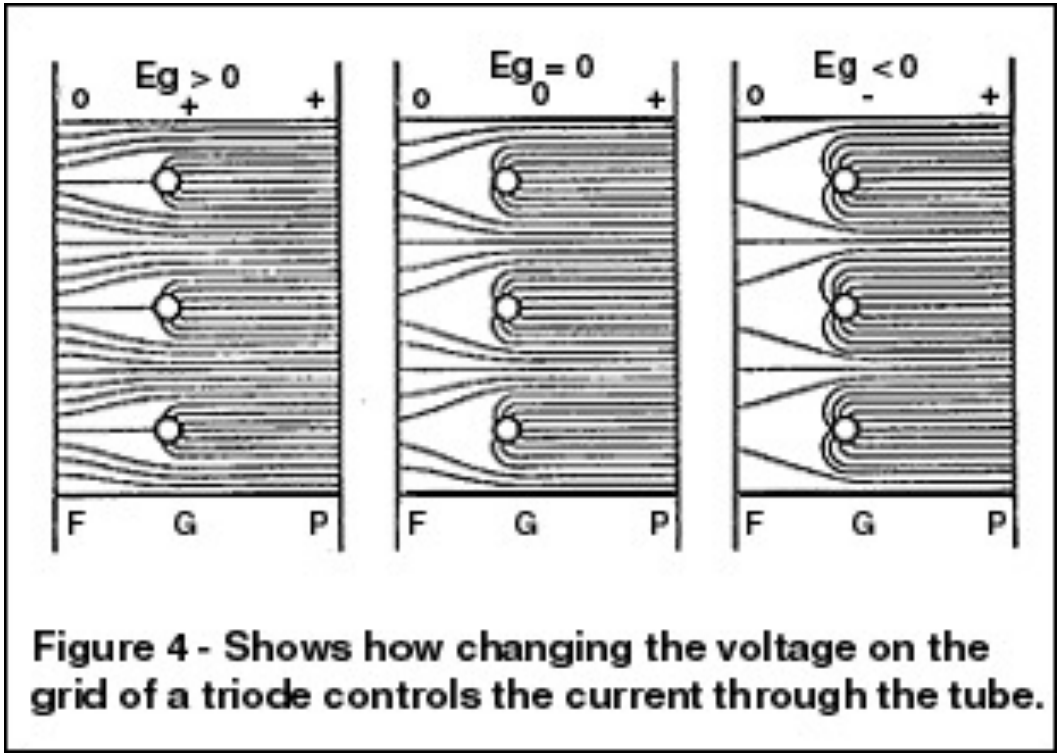
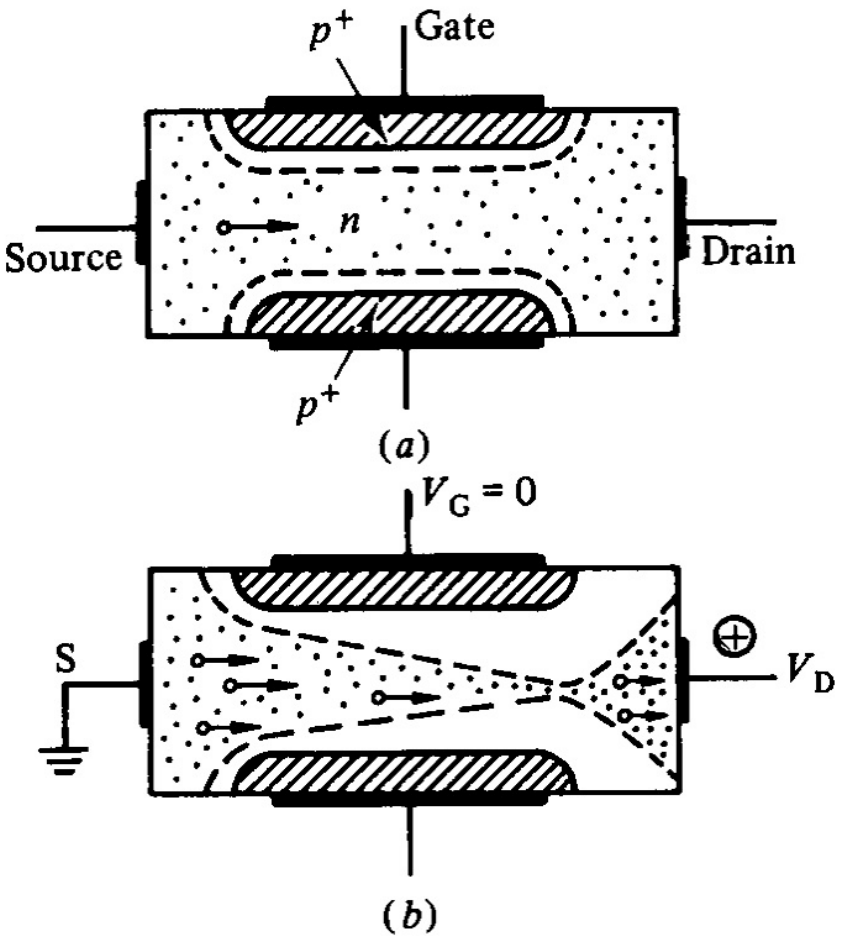
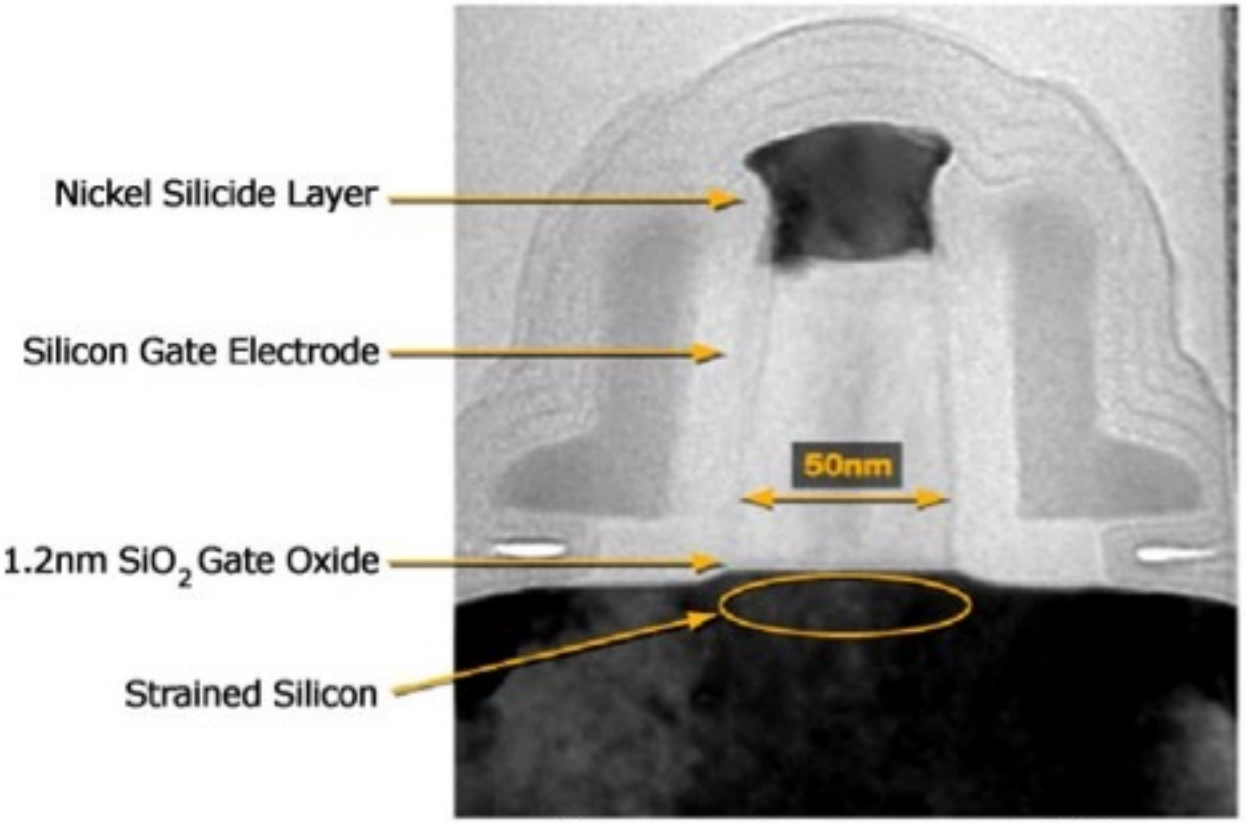


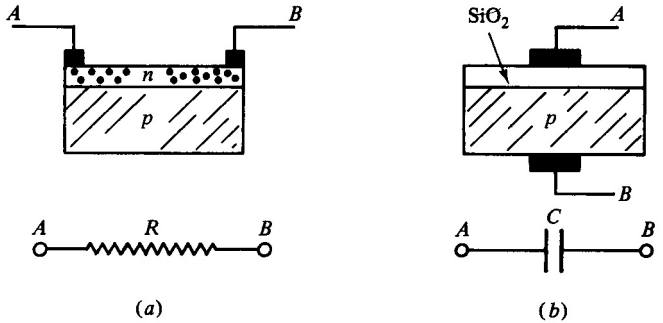
Figure 4 - Shows how changing the voltage on the grid of a triode controls the current through the tube.

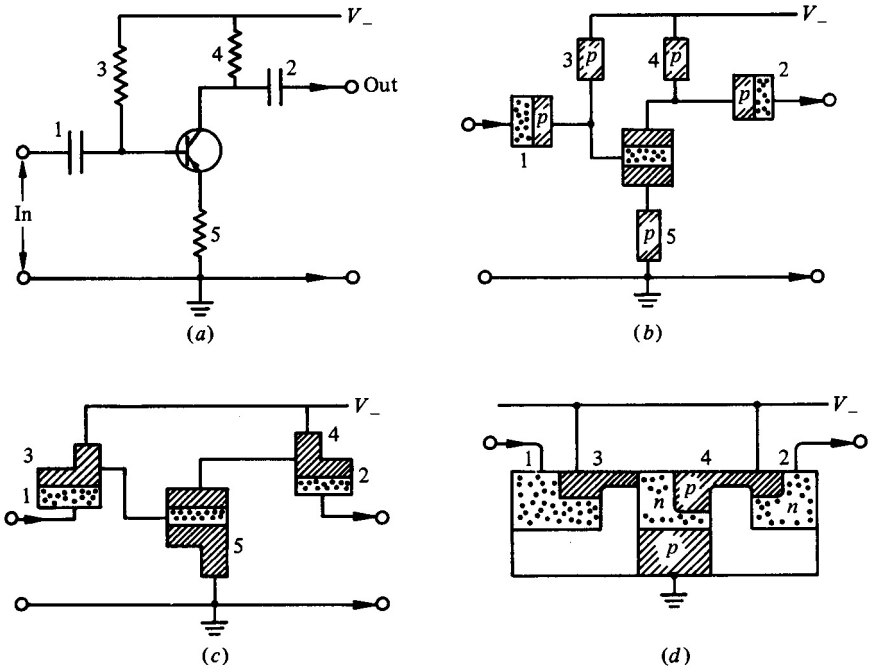
I transistor a effetto di campo (FET)

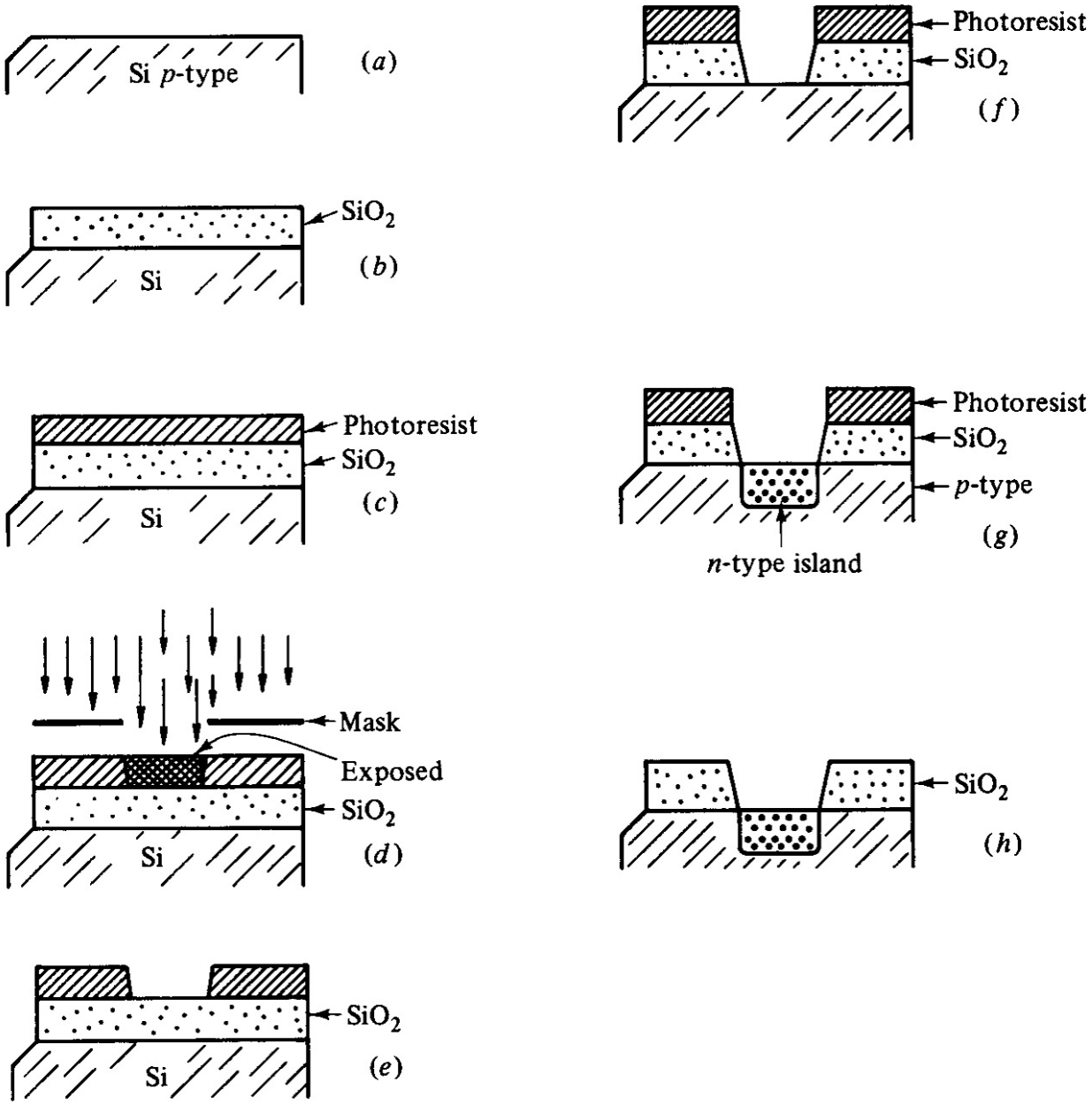


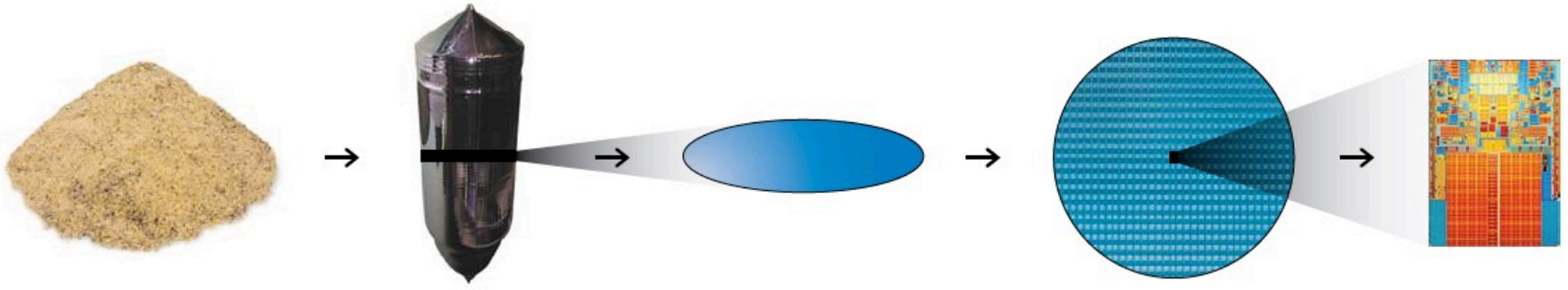


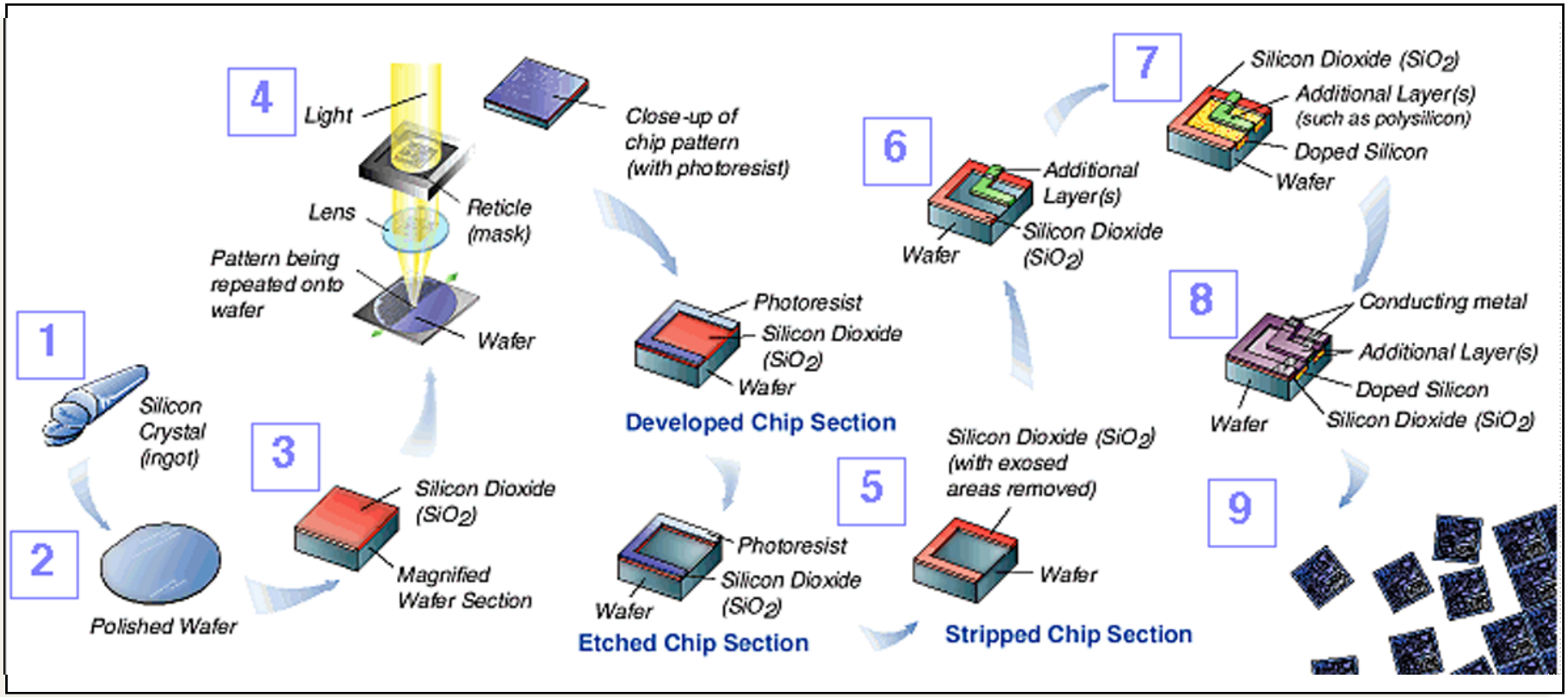
50nm transistor dimension is ~2000x smaller than diameter of human hair

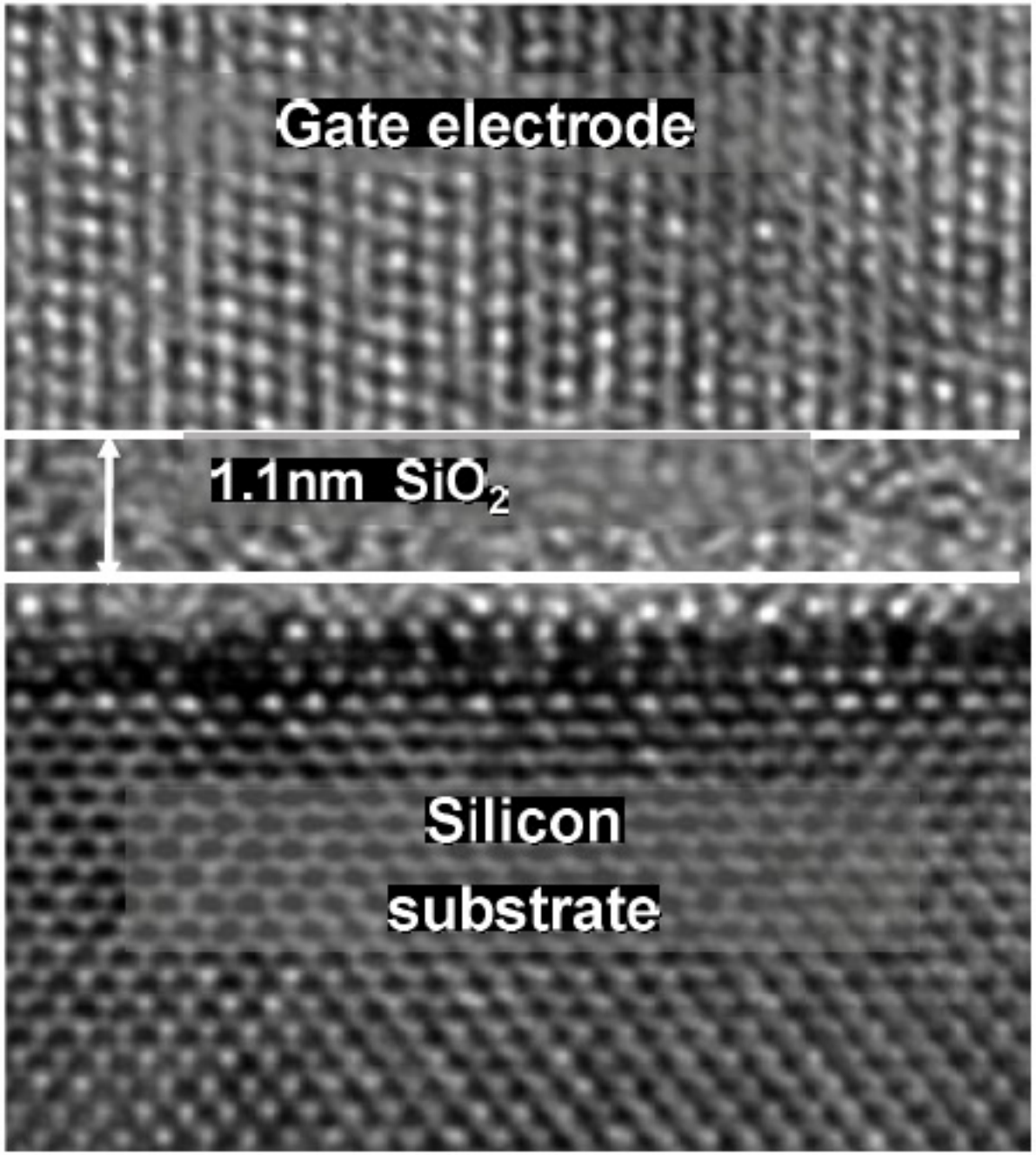

A
B
n
p
A
R
B
(a)
SiO2
A
p
B
A
C
B
(b)


V_
3
4
2
Out
1
In
5
(a)
V_
3
p
4
p
2
p
p
1
p
5
(b)
V_
3
4
1
2
5
(c)
V_
1
3
4
2
n
p
n
p
(d)


Si p-type
(a)
SiO2
Si
(b)
Photoresist
SiO2
Si
(c)
Mask
Exposed
SiO2
Si
(d)
SiO2
Si
(e)
Photoresist
SiO2
(f)
Photoresist
SiO2
p-type
n-type island
(g)
SiO2
(h)


Sand
Purified silicon ingot
Wafer sliced from ingot and polished
Processed wafer
Completed die from finished wafer

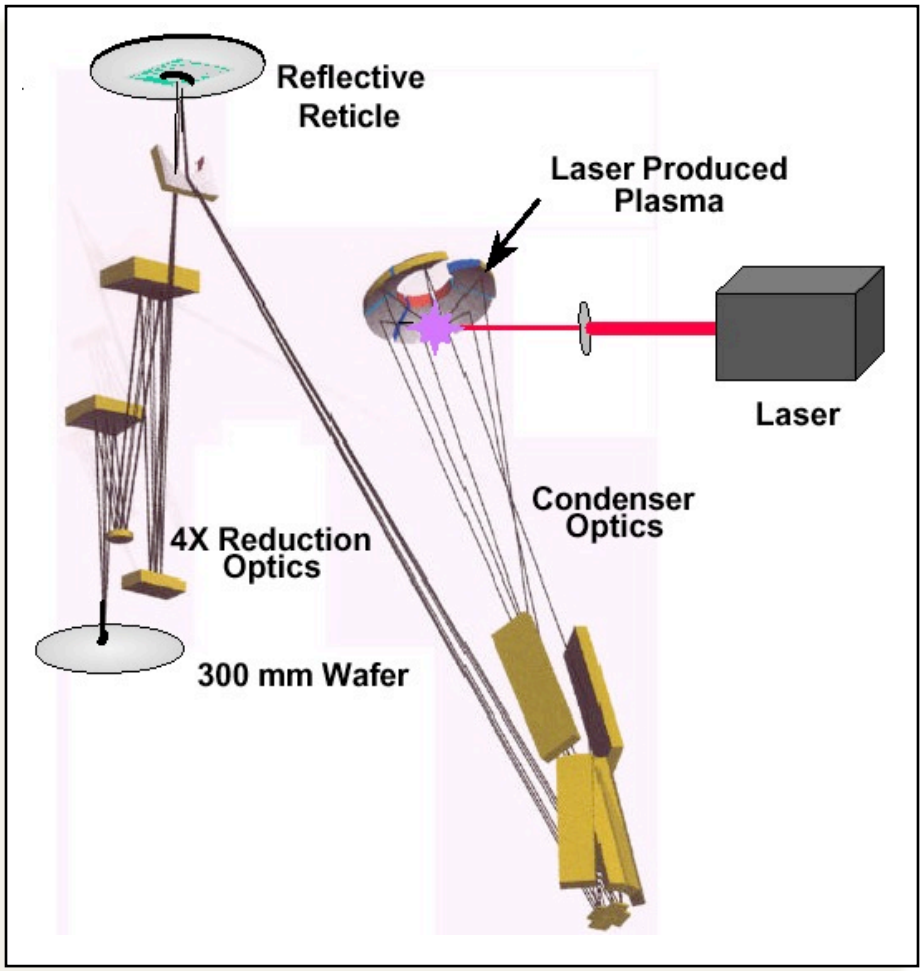

1
Silicon Crystal (ingot)
2
Polished Wafer
3
Silicon Dioxide (SiO_2)
Magnified Wafer Section
4
Light
Reticle (mask)
Lens
Pattern being repeated onto wafer
Wafer
Close-up of chip pattern (with photoresist)
Photoresist
Silicon Dioxide (SiO_2)
Wafer
Developed Chip Section
5
Photoresist
Silicon Dioxide (SiO_2)
Wafer
Etched Chip Section
Silicon Dioxide (SiO_2) (with exosed areas removed)
Wafer
Stripped Chip Section
6
Additional Layer(s)
Silicon Dioxide (SiO_2)
Wafer
7
Silicon Dioxide (SiO_2)
Additional Layer(s) (such as polysilicon)
Doped Silicon
Wafer
8
Conducting metal
Additional Layer(s)
Doped Silicon
Silicon Dioxide (SiO_2)
Wafer
9


Gate electrode
1.1nm SiO_2
Silicon
substrate

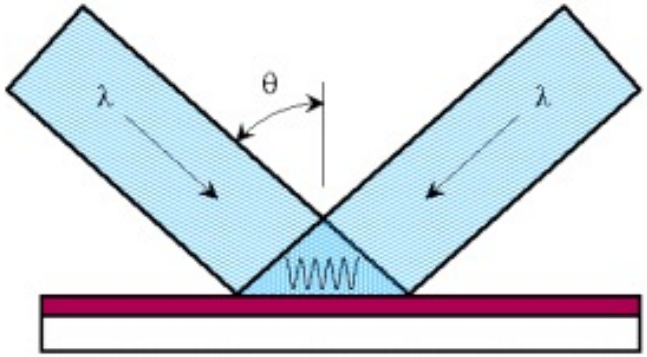
Litografia ad alta risoluzione

richiede l'uso di sorgenti ultraviolette a piccola lunghezza d'onda (< 200 nm)

- laser ad eccimeri oppure lampada a plasma
- focalizzazione per mezzo di elementi ottici riflettenti asferici
- nel caso di radiazione EUV (11-13 nm) gli specchi devono essere lavorati con una tolleranza di ~0.1 nm



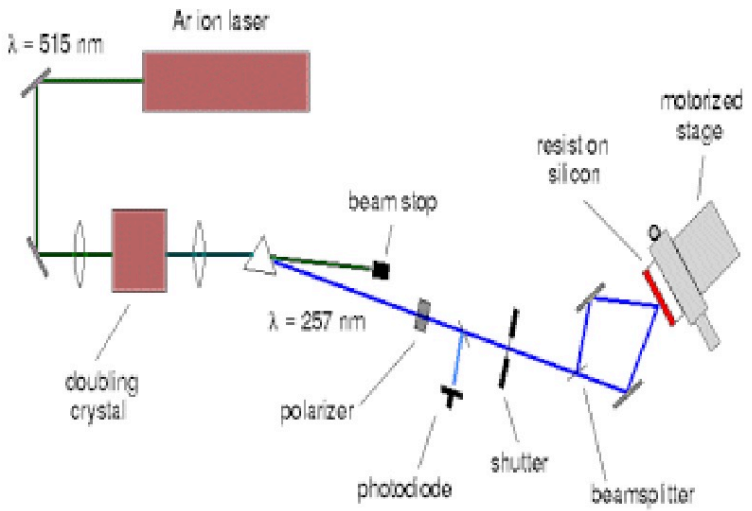
Interferometric Lithography

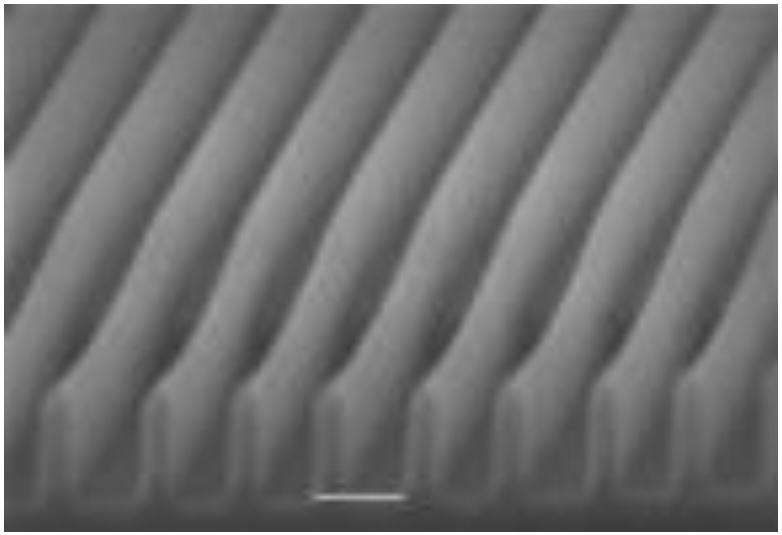


$$\text{period} = \frac{\lambda}{2\sin(\theta)}$$

135 nm at 257 nm/80°

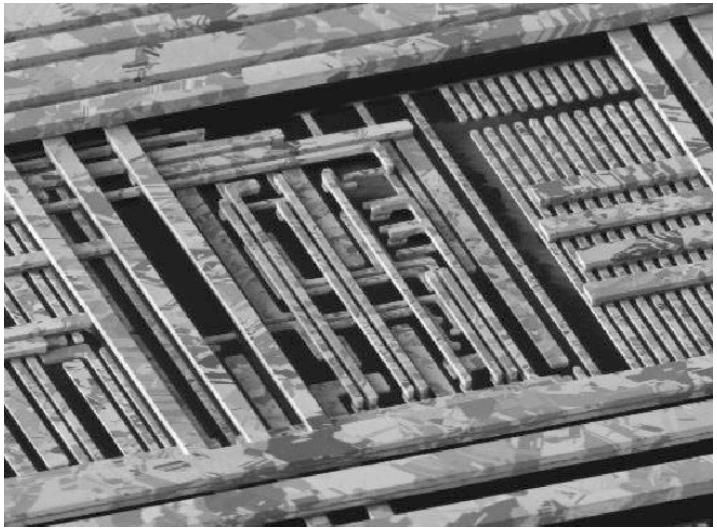
Interferometric Lithography Tool

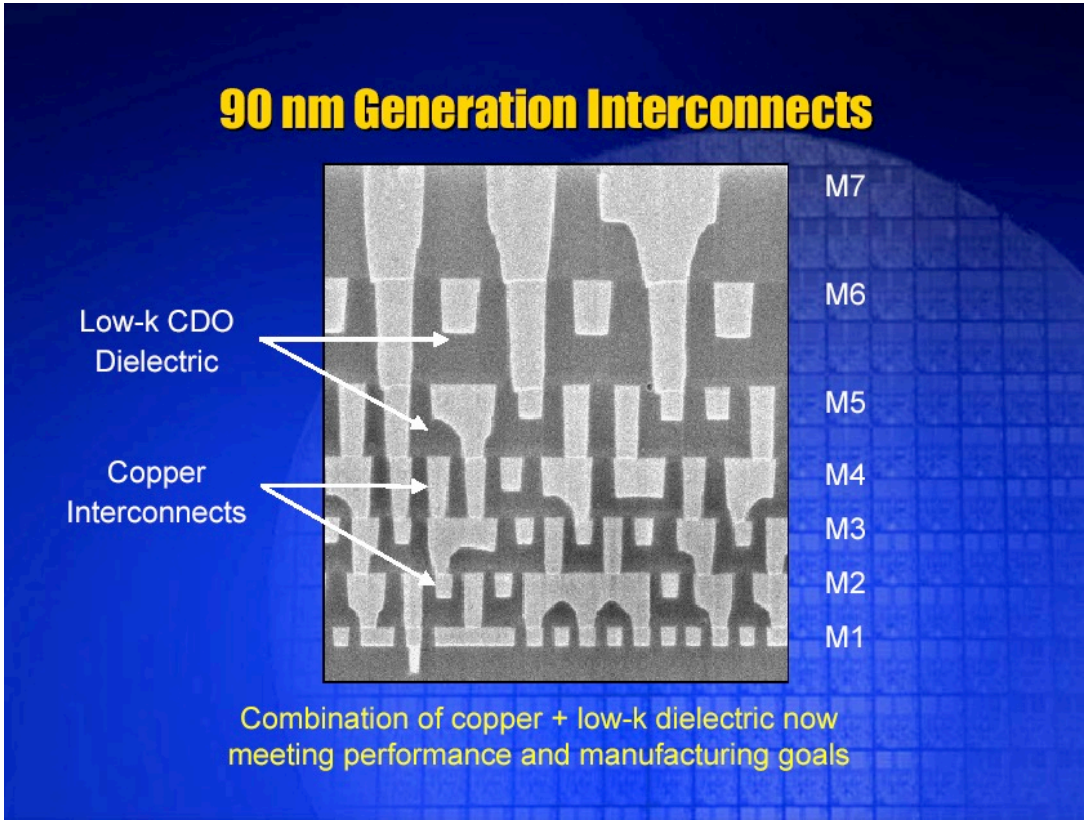




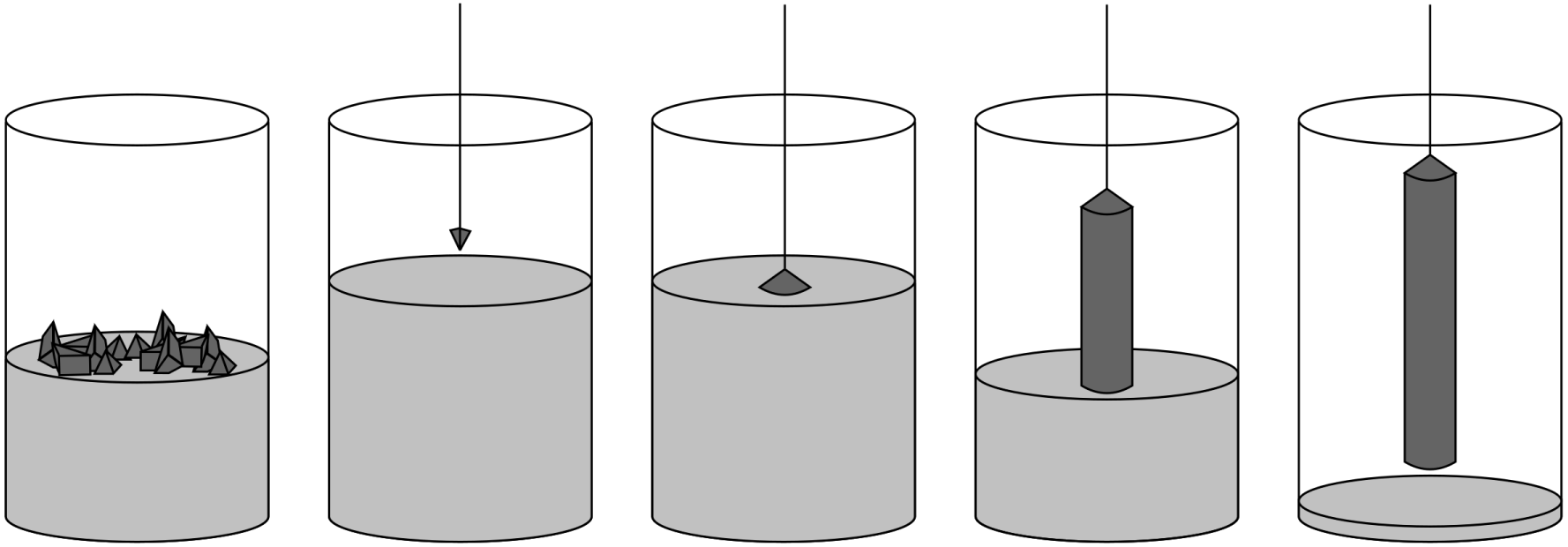
Strutture da 100 nm costruite con litografia interferometrica

La struttura dei microcircuiti è realmente tridimensionale ...





Il processo Czochralski per la crescita dei cristalli di silicio



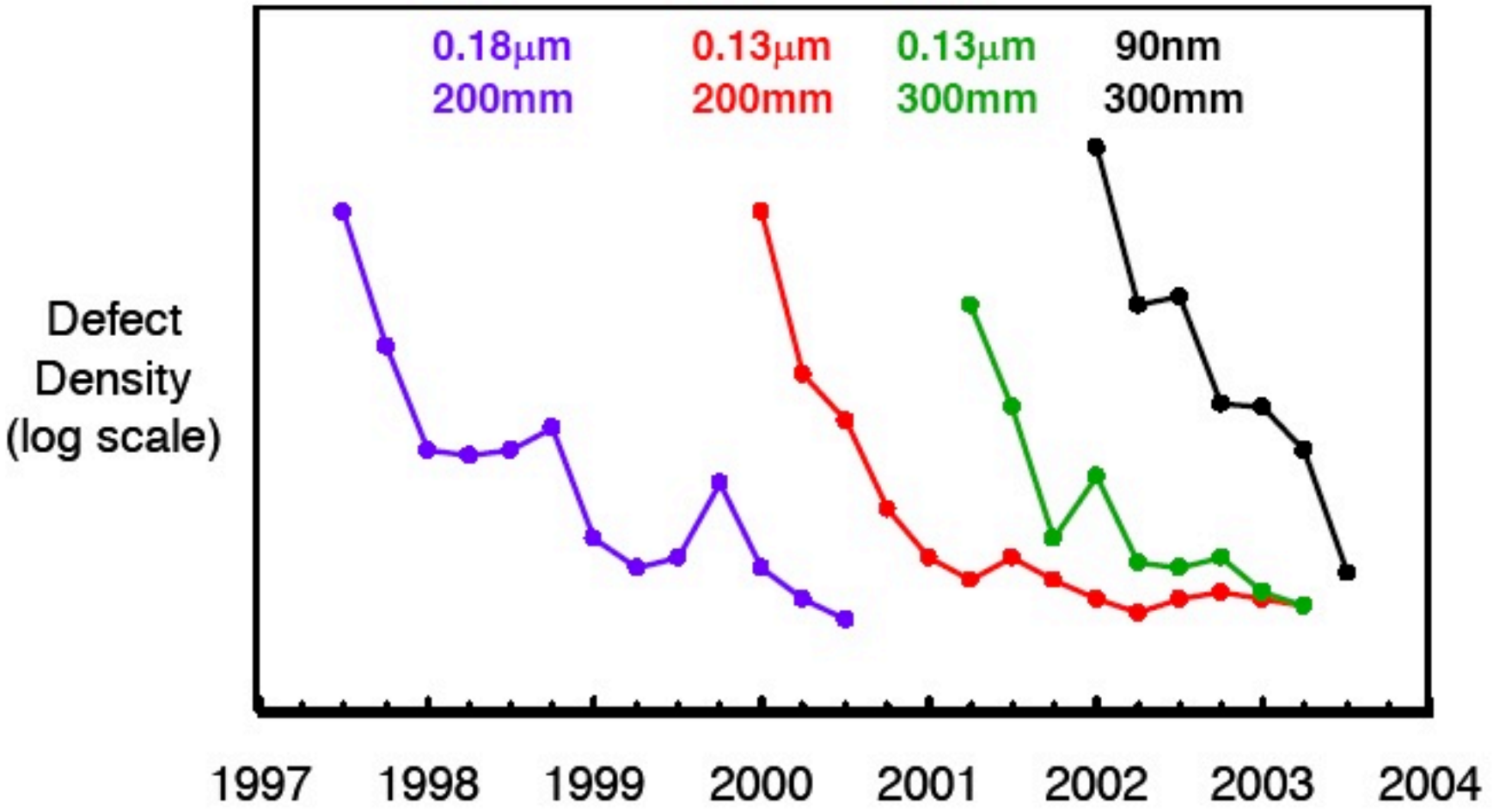
Melting of polysilicon, doping

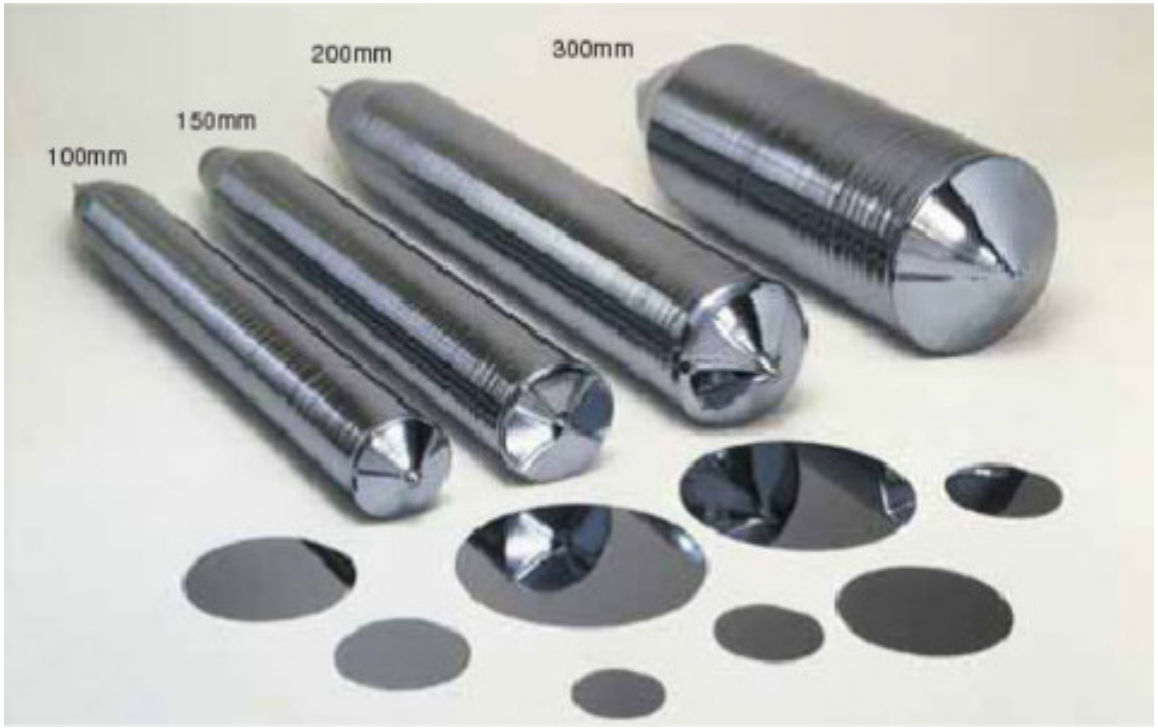
Introduction of the seed crystal

Beginning of the crystal growth

Crystal pulling

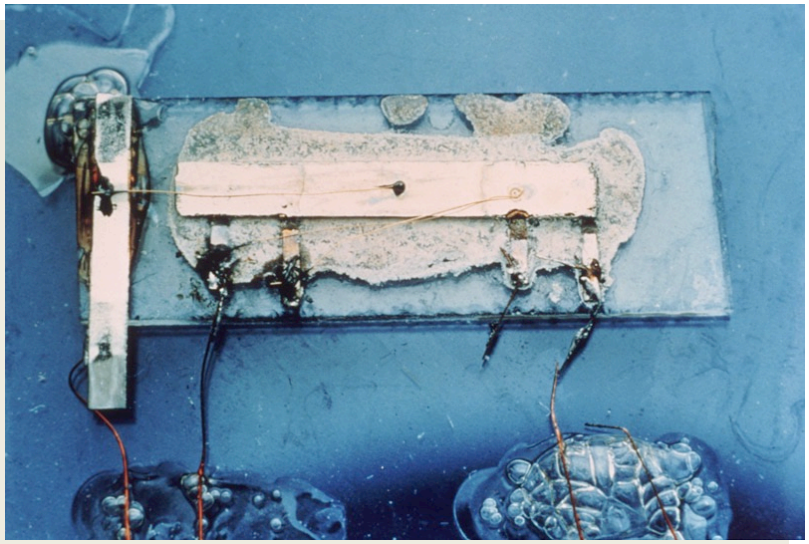
Formed crystal with a residue of melted silicon


0.18μm
200mm
0.13μm
200mm
0.13μm
300mm
90nm
300mm
Defect
Density
(log scale)
1997
1998
1999
2000
2001
2002
2003
2004


100mm
150mm
200mm
300mm

Jack S. Kilby premio Nobel per la Fisica 2000 (con Zhores e Alferov)

Il primo IC (1958)

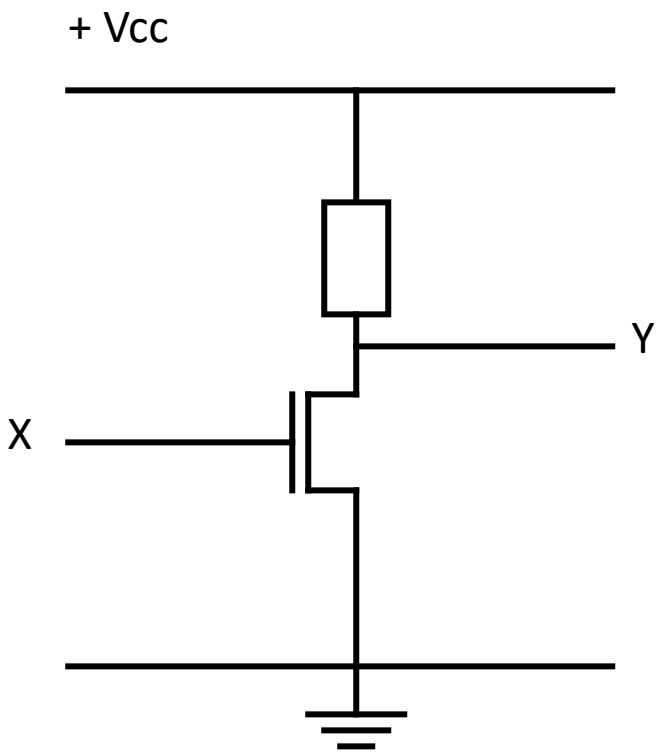


Jack Kilby mentre esamina un wafer da 300 mm

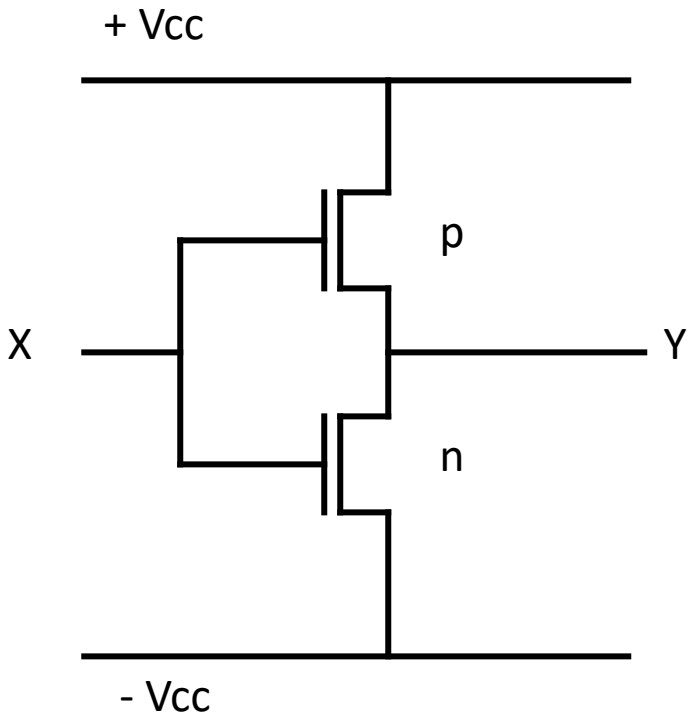
La prima calcolatrice tascabile (1967) inventata alla TI da Jack Kilby, Jerry Merryman, e James Van Tassel

La tecnologia CMOS

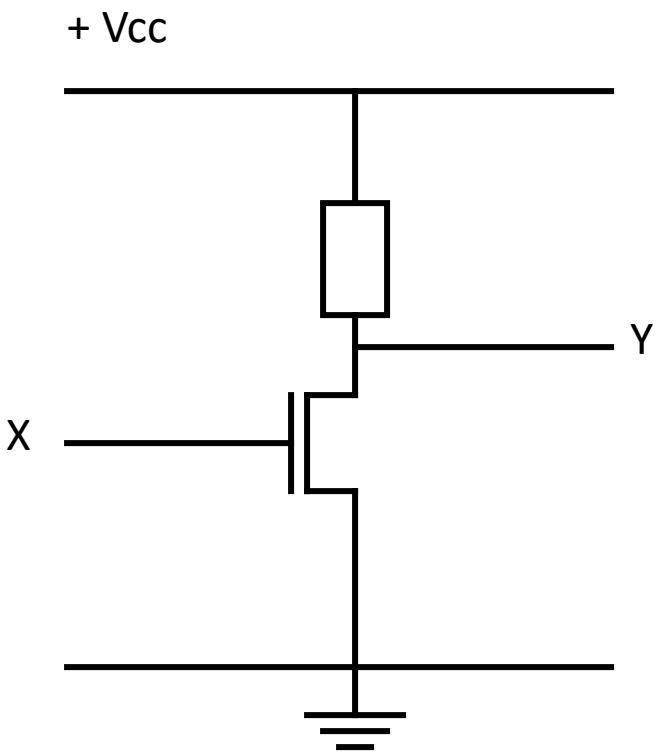
Invertitore MOS



Invertitore CMOS

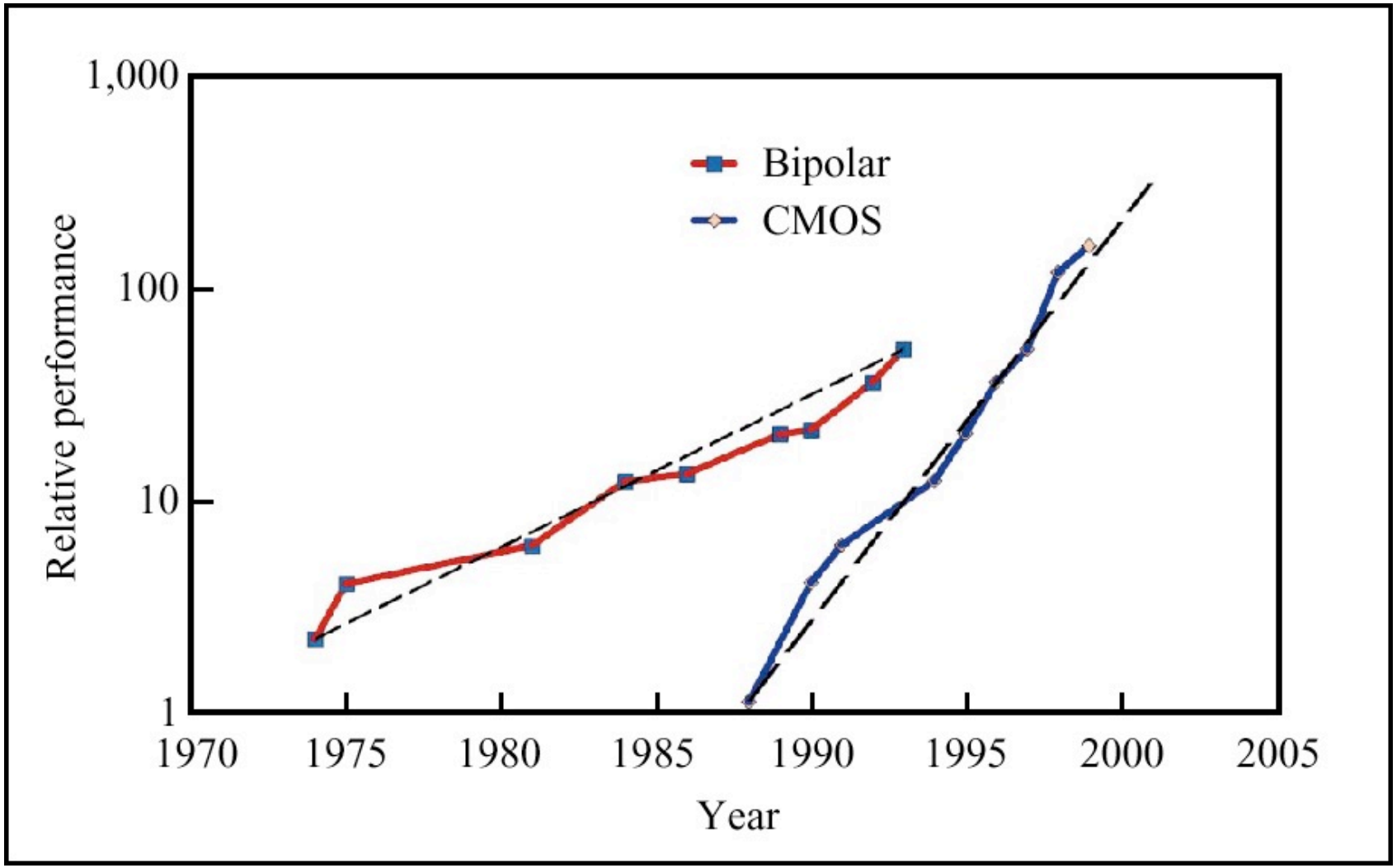


Invertitore MOS

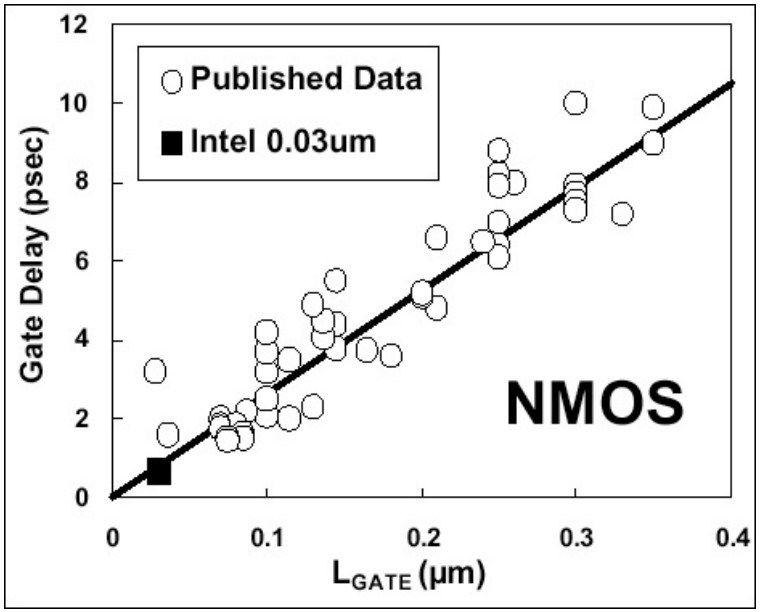


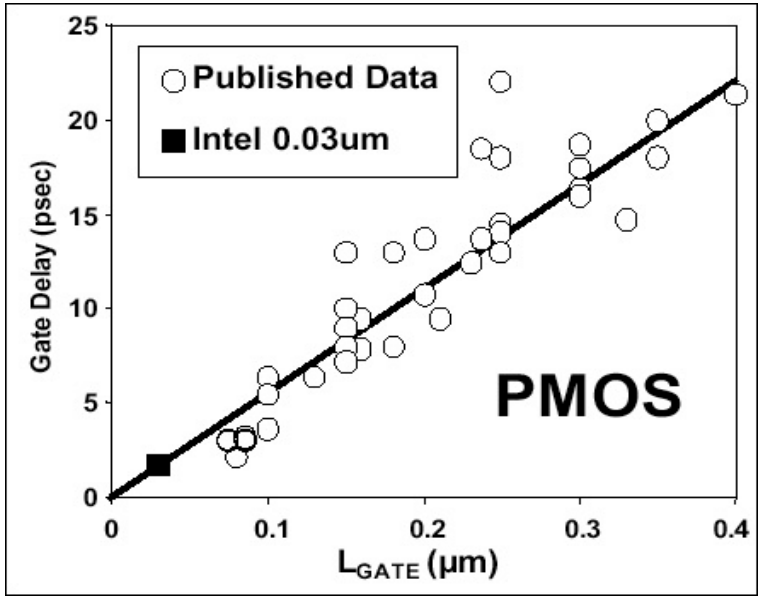
"A transistor is a three-connection device: one input is connected to the gate signal, one to ground, and the other to a positive voltage via a resistor. The central property of the transistor is that if the gate has a distinctly positive voltage the component conducts, but if the gate is zero or distinctly negative, it does not. Now look at the behavior of the output voltage as we input a voltage to the gate. If we input a positive voltage, which by convention we label a 1, the transistor conducts: a current flows through it, and the output voltage becomes zero, or binary 0. On the other hand, if the gate was a little bit negative, or zero, no current flows, and the output is the same as + V, or 1. Thus, the output is the opposite of the input, and we have a NOT gate."

(descrizione tratta da R. P. Feynman: "Feynman Lectures on Computation", Addison-Wesley, 1996)

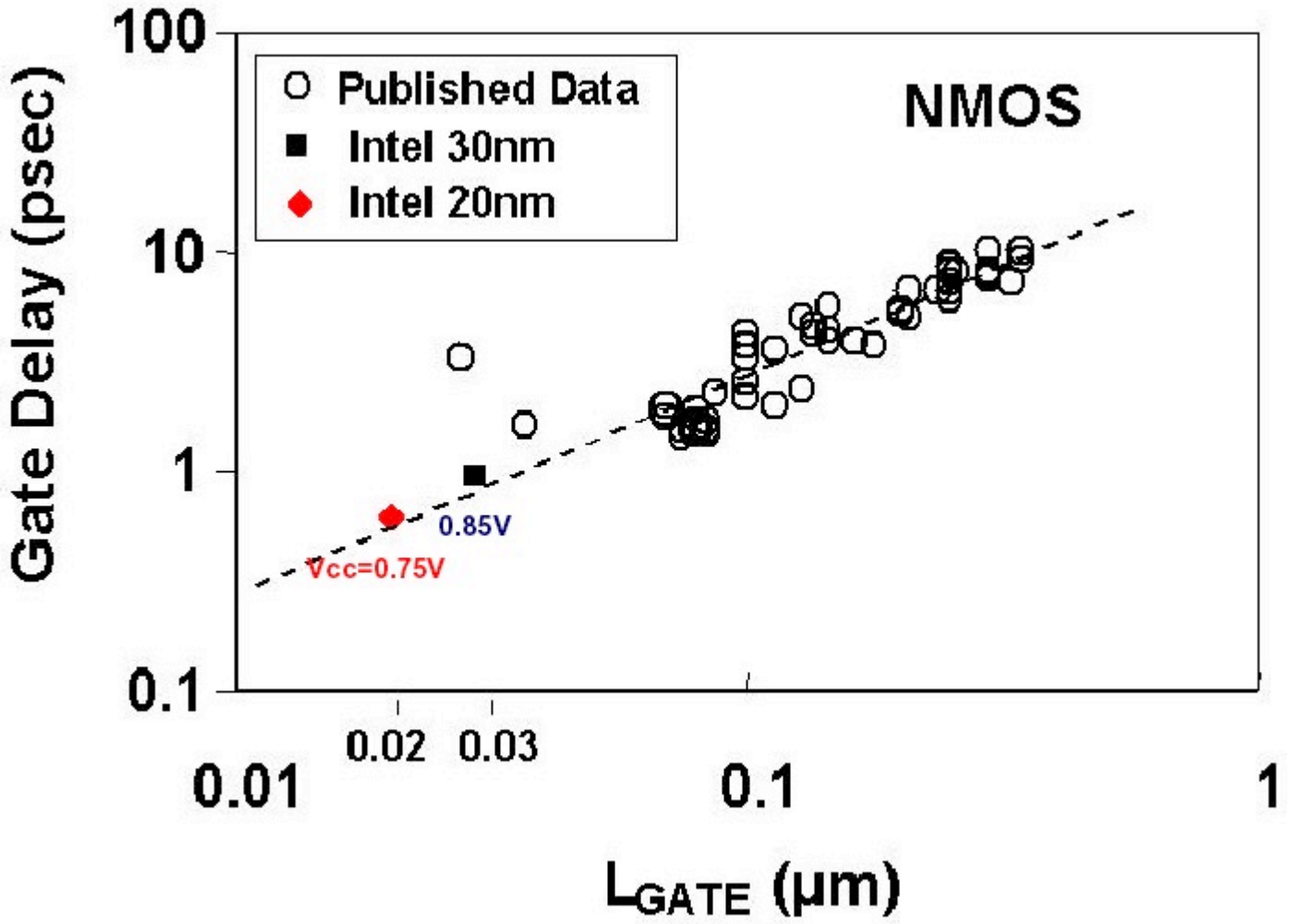


Velocità relative di servers basati su transistors bipolari e CMOS





Tempi di transito estremamente brevi nei transistor da 30 nm
Frequenza di funzionamento di un singolo transistor almeno 500 MHz


Gate Delay (psec)
100
10
1
0.1
Published Data
Intel 30nm
Intel 20nm
NMOS
0.85V
Vcc=0.75V
0.02
0.03
0.01
0.1
1
LGATE (μm)

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

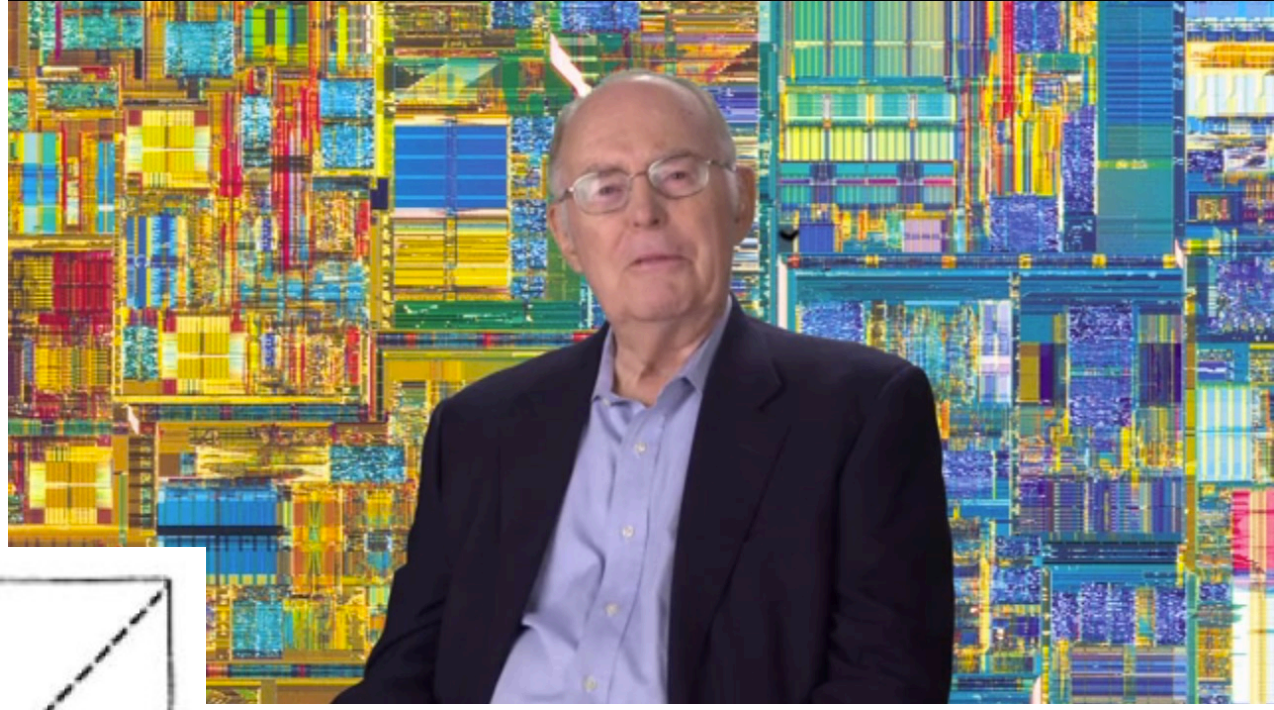
Electronics, Volume 38, Number 8, April 19, 1965

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

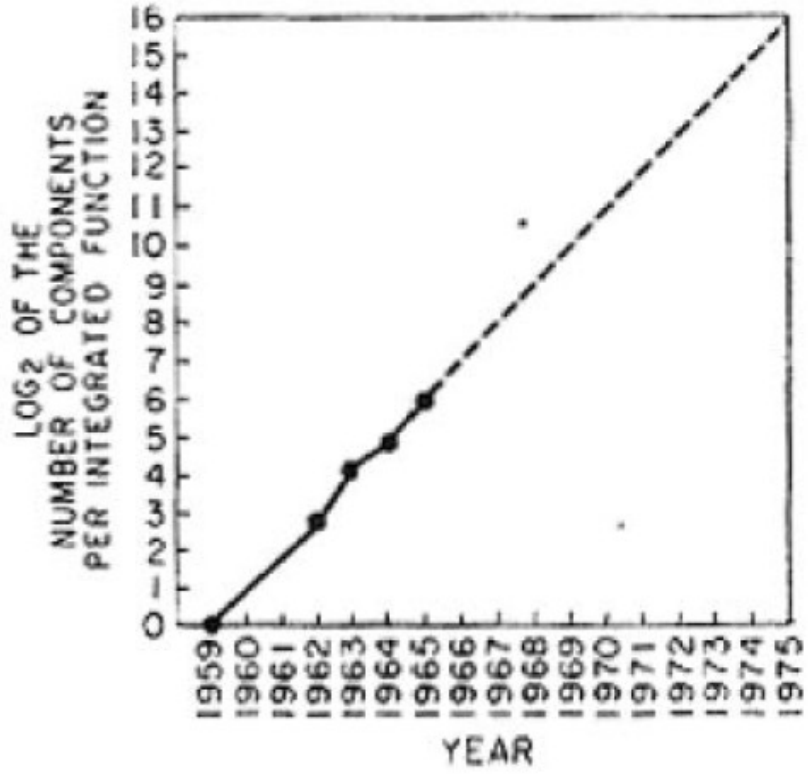
Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

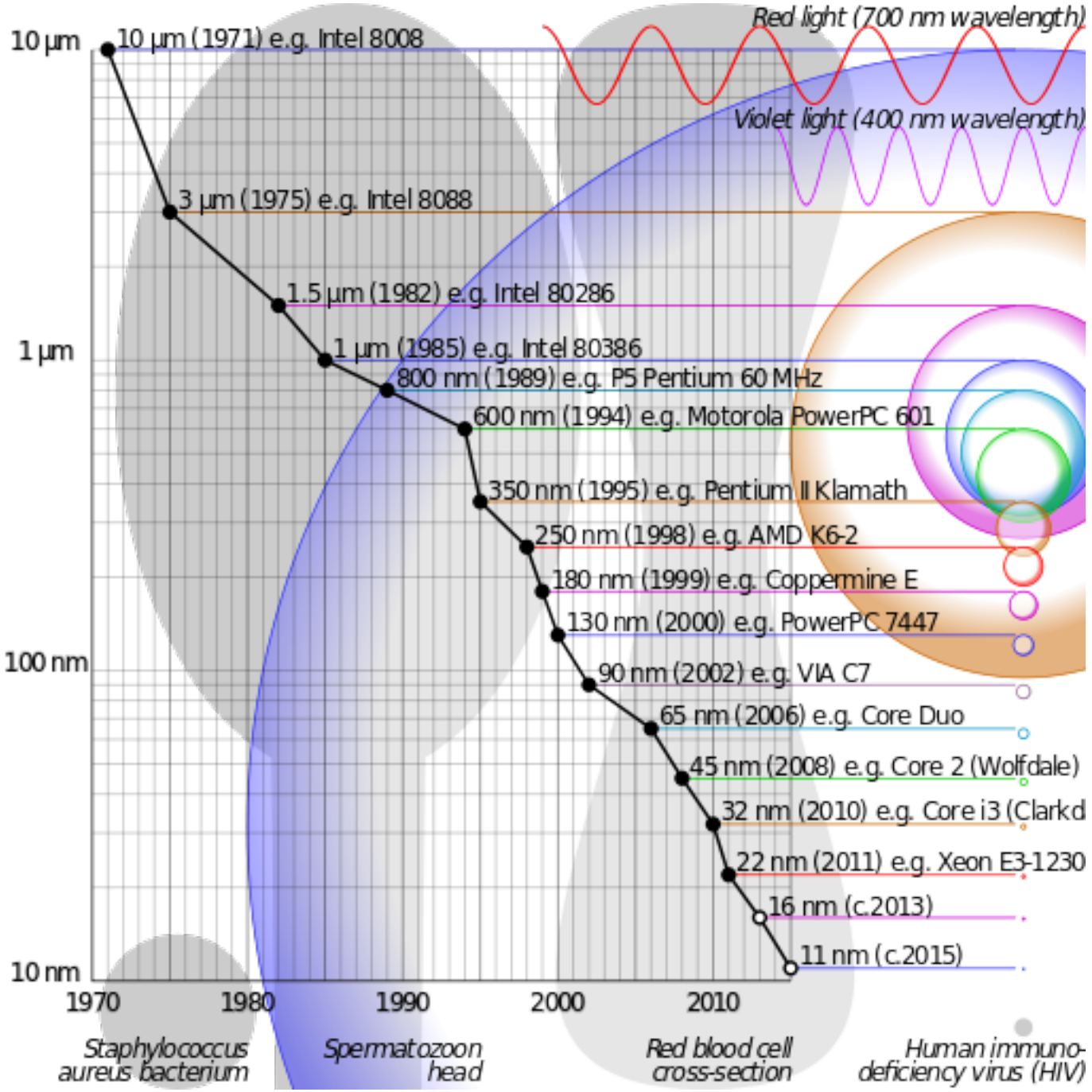
Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.



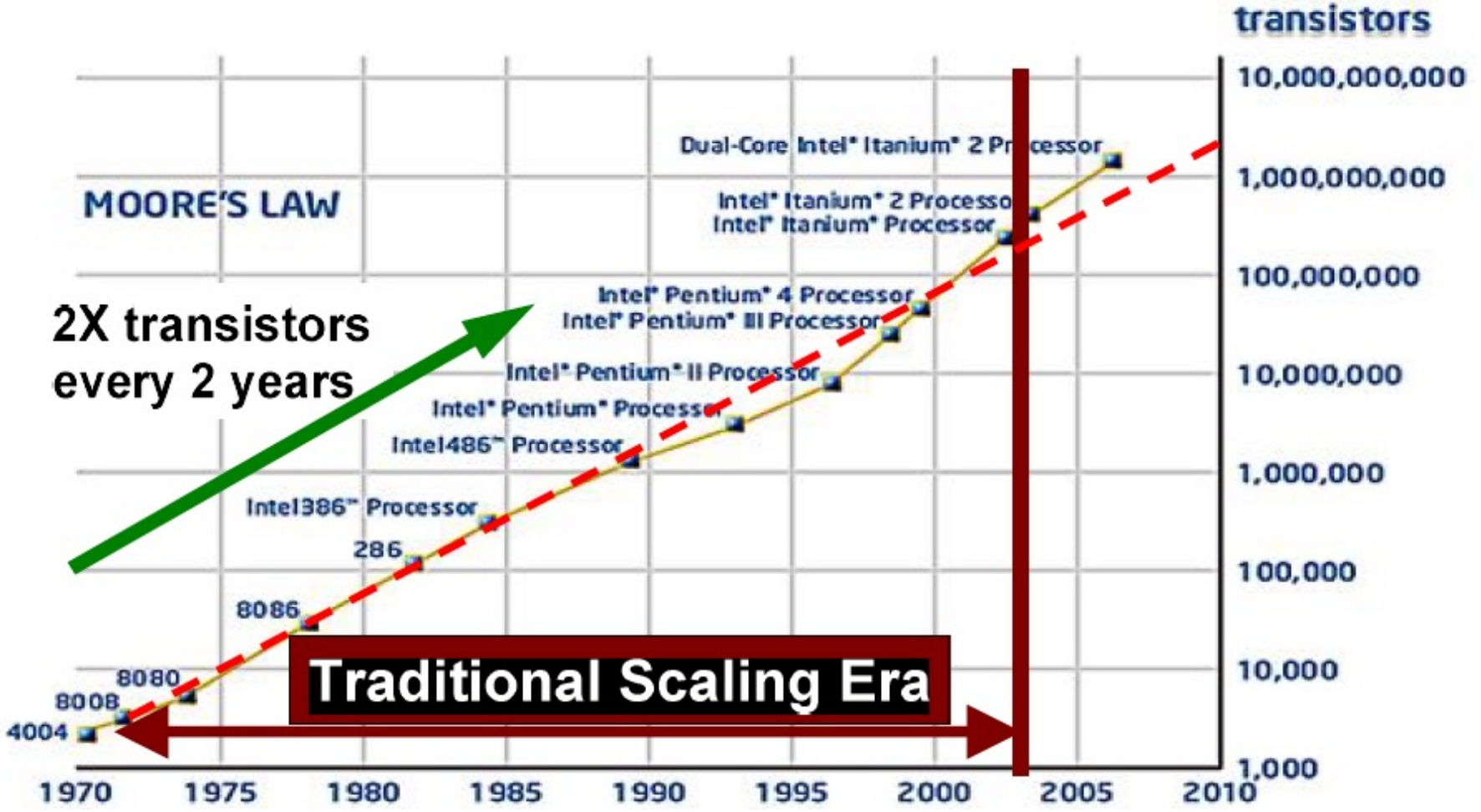
Gordon Moore

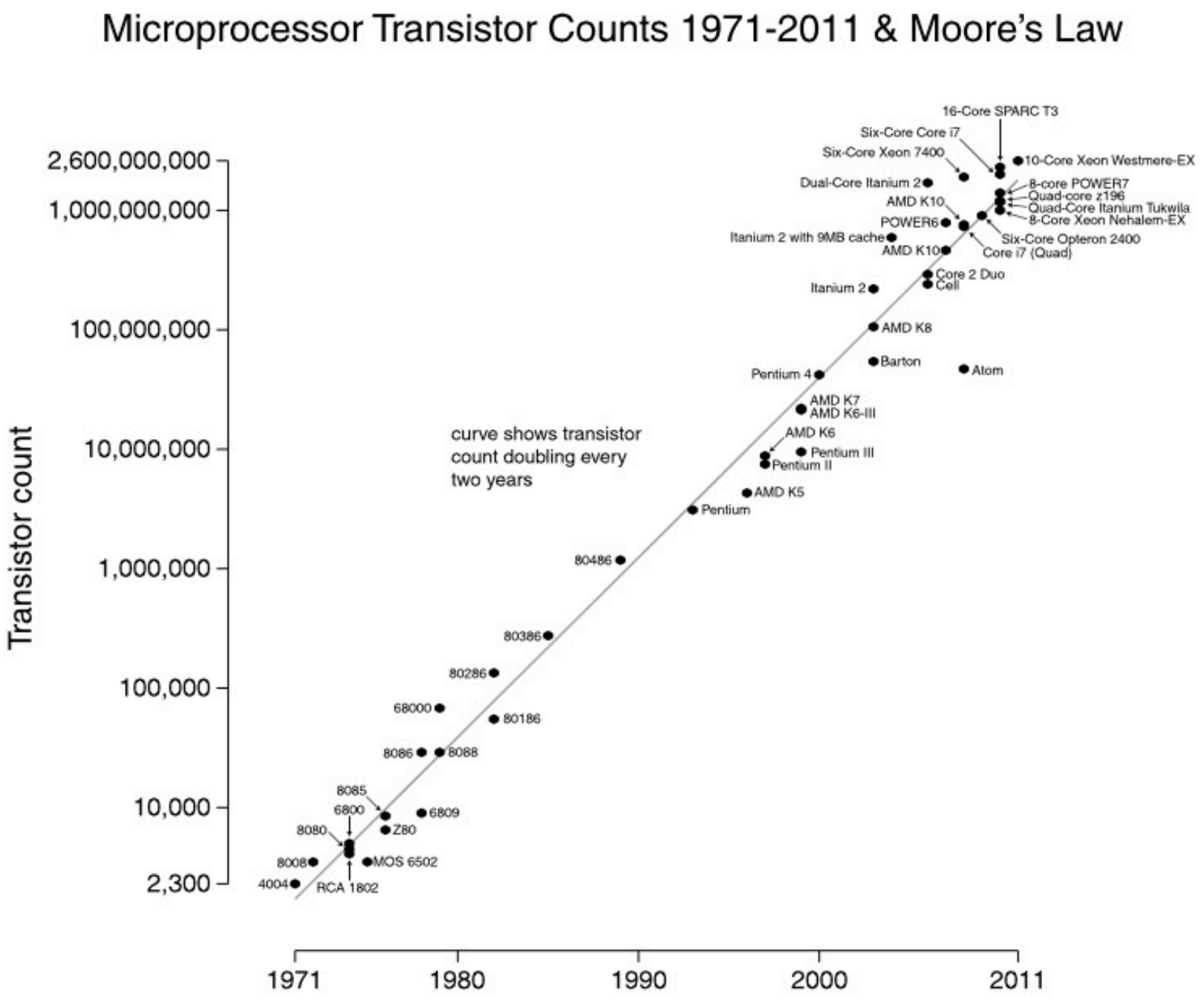


(si veda https://www.sciencehistory.org/historical-profile/gordon-e-moore per un breve film biografico su Gordon Moore)


Red light (700 nm wavelength)
Violet light (400 nm wavelength)
10 µm
1 µm
100 nm
10 nm
10 µm (1971) e.g. Intel 8008
3 µm (1975) e.g. Intel 8088
1.5 µm (1982) e.g. Intel 80286
1 µm (1985) e.g. Intel 80386
800 nm (1989) e.g. P5 Pentium 60 MHz
600 nm (1994) e.g. Motorola PowerPC 601
350 nm (1995) e.g. Pentium II Klamath
250 nm (1998) e.g. AMD K6-2
180 nm (1999) e.g. Coppermine E
130 nm (2000) e.g. PowerPC 7447
90 nm (2002) e.g. VIA C7
65 nm (2006) e.g. Core Duo
45 nm (2008) e.g. Core 2 (Wolfdale)
32 nm (2010) e.g. Core i3 (Clarkd
22 nm (2011) e.g. Xeon E3-1230
16 nm (c.2013)
11 nm (c.2015)
1970
1980
1990
2000
2010
Staphylococcus aureus bacterium
Spermatozoon head
Red blood cell cross-section
Human immuno-deficiency virus (HIV)

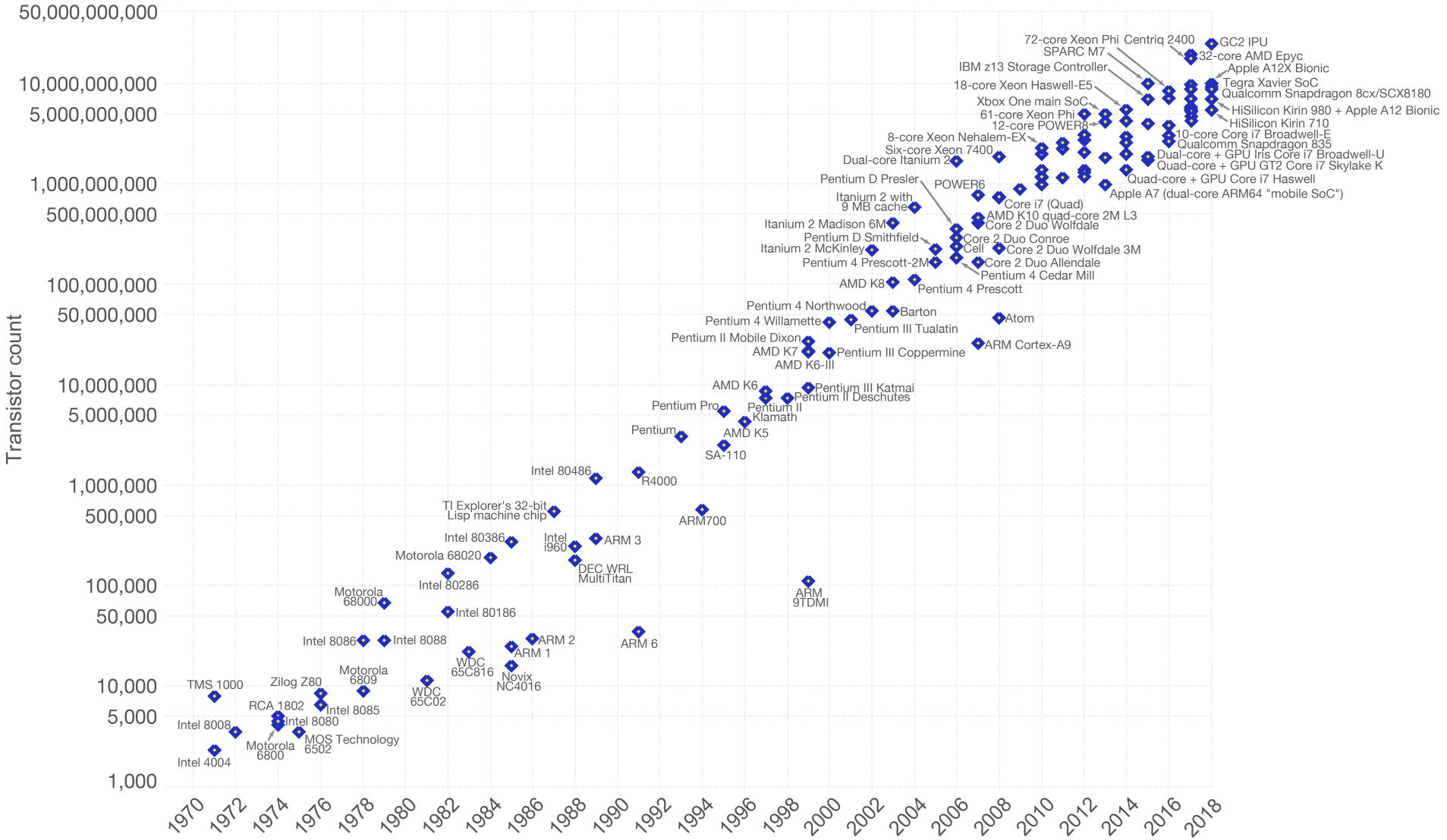
40+ Years of Moore's Law at INTEL: From Few to Billions of Transistors




Microprocessor Transistor Counts 1971-2011 & Moore's Law
Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
1971
1980
1990
2000
2011
curve shows transistor count doubling every two years
16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
AMD K10
Quad-Core Itanium Tukwila
POWER6
8-Core Xeon Nehalem-EX
Itanium 2 with 9MB cache
Six-Core Opteron 2400
AMD K10
Core i7 (Quad)
Core 2 Duo
Itanium 2
Cell
AMD K8
Barton
Atom
Pentium 4
AMD K7
AMD K6-III
AMD K6
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
6809
8080
Z80
8008
MOS 6502
4004
RCA 1802

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.

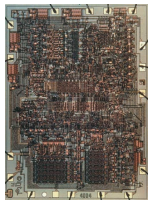


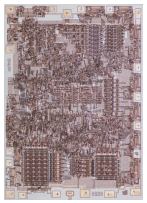
Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)

The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Intel Chips

Decades of Intel chips, including the 22nm 3rd generation Intel® Core™ processor with its revolutionary 3-D Tri-Gate transistors, illustrate Intel's unwavering commitment to delivering technology and manufacturing leadership to the devices you use every day. As you advance through the chart, the benefits of Moore's Law, which states that the number of transistors roughly doubles every couple of years, are evident as Intel increases transistor density and innovates the architecture designs that deliver more complex, powerful, and energy-efficient chips that transform the way we work, live, and play.


1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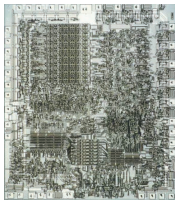
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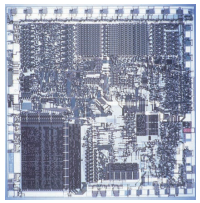
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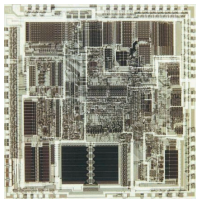
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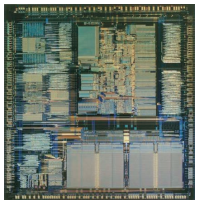
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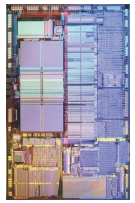
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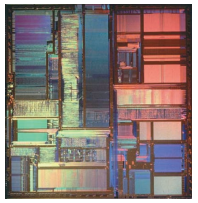
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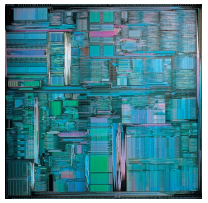
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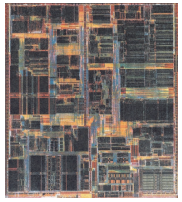
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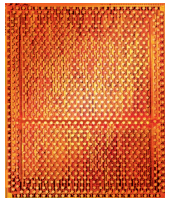
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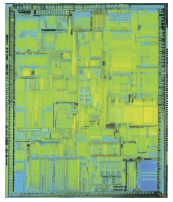
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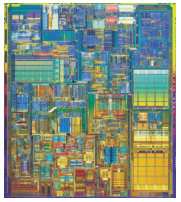
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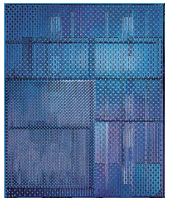
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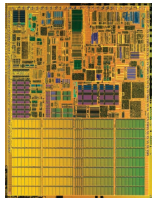
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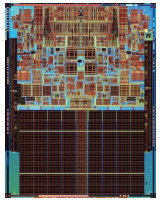
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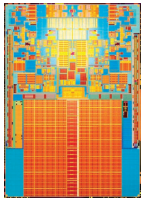
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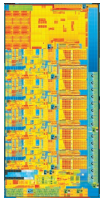
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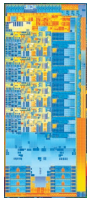

20

1
1971
Intel® 4004 processor
Initial clock speed: 108KHz
Transistors: 2,300
Manufacturing technology: 10 micron

2
1972
Intel® 8008 processor
Initial clock speed: 800KHz
Transistors: 3,500
Manufacturing technology: 10 micron

3
1974
Intel® 8080 processor
Initial clock speed: 2MHz
Transistors: 4,500
Manufacturing technology: 6 micron

4
1978
Intel® 8086 processor
Initial clock speed: 5MHz
Transistors: 29,000
Manufacturing technology: 3 micron

5
1982
Intel® 286™ processor
Initial clock speed: 6MHz
Transistors: 134,000
Manufacturing technology: 1.5 micron

6
1985
Intel386™ processor
Initial clock speed: 16MHz
Transistors: 275,000
Manufacturing technology: 1.5 micron

7
1989
Intel486™ processor
Initial clock speed: 25MHz
Transistors: 1.2 million
Manufacturing technology: 1 micron

8
1993
Intel® Pentium® processor
Initial clock speed: 66MHz
Transistors: 3.1 million
Manufacturing technology: 0.8 micron

9
1995
Intel® Pentium® Pro processor
Initial clock speed: 200MHz
Transistors: 5.5 million
Manufacturing technology: 0.35 micron

10
1997
Intel® Pentium® II processor
Initial clock speed: 300MHz
Transistors: 7.5 million
Manufacturing technology: 0.25 micron

10
1997
Intel® Pentium® II processor
Initial clock speed: 300MHz
Transistors: 7.5 million
Manufacturing technology: 0.25 micron

11
1998
Intel® Celeron® processor
Initial clock speed: 266MHz
Transistors: 7.5 million
Manufacturing technology: 0.25 micron

12
1999
Intel® Pentium® III processor
Initial clock speed: 600MHz
Transistors: 9.5 million
Manufacturing technology: 0.25 micron

13
2000
Intel® Pentium® 4 processor
Initial clock speed: 1.5GHz
Transistors: 42 million
Manufacturing technology: 0.18 micron

14
2001
Intel® Xeon® processor
Initial clock speed: 1.7GHz
Transistors: 42 million
Manufacturing technology: 0.18 micron

15
2003
Intel® Pentium® M processor
Initial clock speed: 1.7GHz
Transistors: 55 million
Manufacturing technology: 90nm

16
2006
Intel® Core™2 Duo processor
Initial clock speed:: 2.66GHz
Transistors: 291 million
Manufacturing technology: 65nm

17
2008
Intel® Core™2 Duo processor
Initial clock speed: 2.4GHz
Transistors: 410 million
Manufacturing technology: 45nm

18
2008
Intel® Atom™ processor
Initial clock speed: 1.86GHz
Transistors: 47 million
Manufacturing technology: 45nm

19
2010
2nd generation Intel® Core™ processor
Initial clock speed: 3.8GHz
Transistors: 1.16 billion
Manufacturing technology: 32nm

20
2012
3rd generation Intel® Core™ processor
Initial clock speed: 2.9GHz
Transistors: 1.4 billion
Manufacturing technology: 22nm


SNEAK PEEK INTO THE FUTURE
2018
2019
2020
14NM/10NM PLATFORM
CASCADE LAKE
14NM
SHIPPING Q4'18
COOPER LAKE
14NM
ICE LAKE
10NM
INTEL OPTANE PERSISTENT MEMORY
INTEL DLBOOST: VNNI
SECURITY MITIGATIONS
NEXT GEN INTEL DLBOOST: BFLOAT16
LEADERSHIP PERFORMANCE
intel
DATA-CENTRIC

Intel's 10nm Products Revealed So Far		
Data by Intel, October, 2020		
Product	**Technology**	**Application**
Cannon Lake	1st generation 10nm	Notebooks, low-power desktops
Ice Lake	2nd generation 10nm	Notebooks, low-power desktops
Ice Lake-SP		Datacenters
Lakefield (compute tile)		Notebooks, hybrids
Atom P5900 'Snow Ridge'		5G base stations, edge applications
Atom x6000e 'Elkhart Lake'		IoT, edge applications
Tiger Lake	10nm SuperFin	Notebooks, compact desktops
DG1, SG1 GPU		Notebooks, datacenters
Ponte Vecchio (base tile)		HPC
Alder Lake	10nm Enhanced SupeFin	Notebooks, desktops
Xe-HP GPU		Datacenters
Sapphire Rapids		Datacenters
Ponte Vecchio (rambo cache)		HPC

Leggi di scala nei microcircuiti

il problema delle interconnessioni

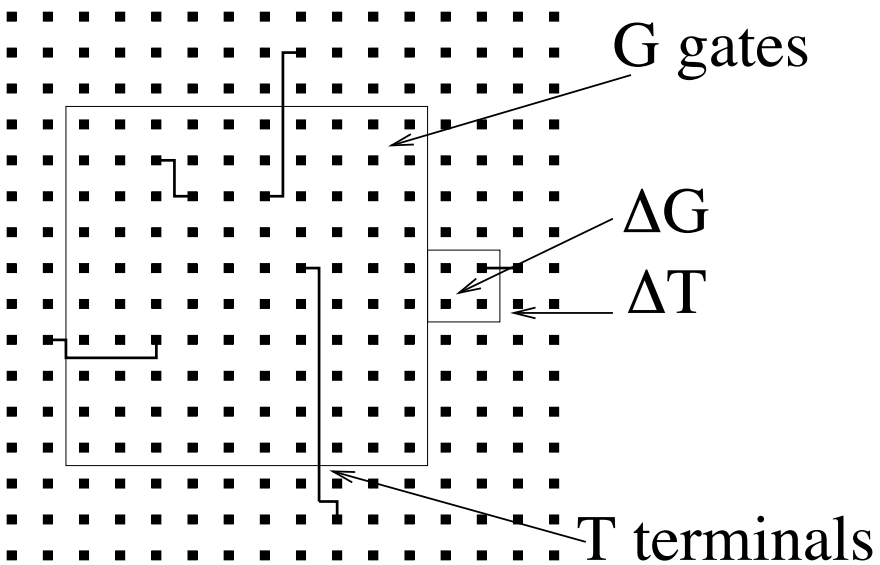
Regola di Rent (Rent's rule):

numero di terminali esterni $\propto N^r$

N = numero di componenti interni
$r \approx 0.65 - 0.7$

4004 (1971) 16 terminali
Pentium 4 (2001) 423 terminali
Pentium 4 (2003) 478 terminali

Nel 2000 Christie e Strooband hanno prodotto una dimostrazione euristica della regola di Rent (Christie e Strooband , IEEE Transactions on Very Large Scale Integration (VLSI) Systems · December 2000)



Nella regione iniziale ci sono G porte logiche e il circuito globale richiede T terminali, così che la "densità di terminali" è T/G (terminali per gate).

Se si perturba questa regione aggiungendo un piccolo numero di porte logiche, e assumendo una semplice dipendenza lineare

$$T = tG$$

si trova allora il numero di nuovi terminali

$$\Delta T = \frac{T}{G}\Delta G = t\Delta G$$

Se ora si assume anche che ci sia una certa ottimizzazione del circuito, si deve presumere che il numero di terminali aggiunti sia inferiore al numero dei terminali di una singola porta

$$\Delta T = p\frac{T}{G}\Delta G \quad \Rightarrow \quad T = tG^p$$

Leggi di scala nei microcircuiti

la dissipazione di potenza

Possiamo schematizzare i transistor e le connessioni nei circuiti CMOS per mezzo di piccole capacità che dobbiamo caricare e scaricare.

La scarica avviene in modo da dissipare l'energia contenuta nel condensatore che viene convertita in calore.

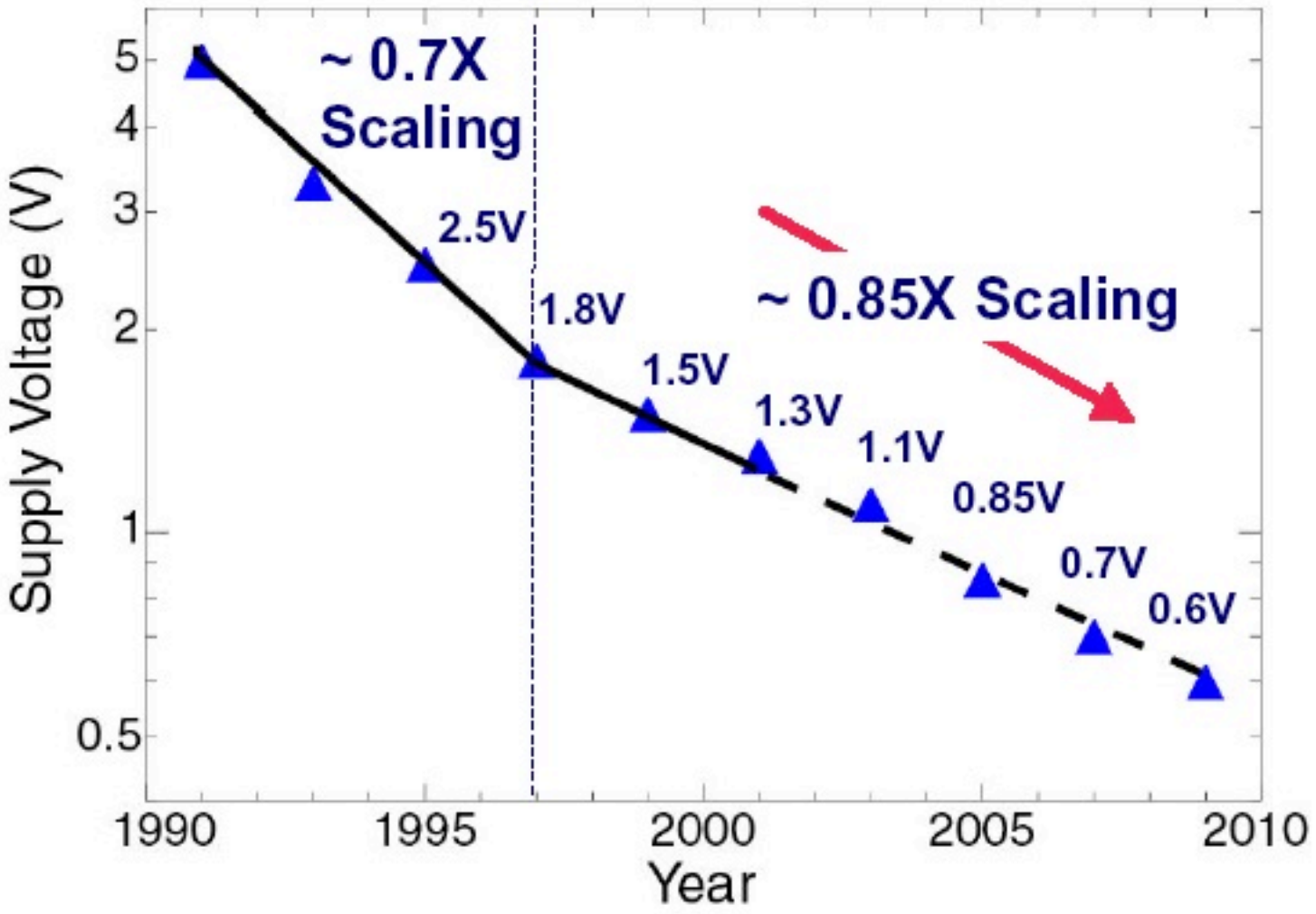
Un bit viene immagazzinato in una capacità (associata ad un transistor MOS) del valore di circa 10^{-18} F, e quindi l'energia accumulata con una tensione di alimentazione di 1 V è

$$\frac{1}{2}CV^2 \sim 10^{-18}\mathrm{J}$$

Se ci sono ~ 20 miliardi di transistor che scaricano questa energia ad ogni ciclo di clock e se si prende una frequenza di clock di 1 GHz si vede che la potenza dissipata dal circuito è

$$\sim 20\ \mathrm{W}$$

che è un valore vicino al consumo reale dei processori Intel I9.


~ 0.7X
Scaling
~ 0.85X Scaling
2.5V
1.8V
1.5V
1.3V
1.1V
0.85V
0.7V
0.6V
Supply Voltage (V)
5
4
3
2
1
0.5
1990
1995
2000
2005
2010
Year

Leggi di scala nei microcircuiti

la tensione di funzionamento

V diminuisce meno velocemente della lunghezza caratteristica dei componenti circuitali perchè:

1. a causa del limite del rumore imposto dalle fluttuazioni termiche $k_B T/e \approx 0.026$ V a temperatura ambiente
2. c'è una tensione caratteristica del semiconduttore (la tensione di gap) $V_g \approx 1$ V

... e inoltre

- lo spessore del gate è limitato dalla tensione di rottura del dielettrico. Si può diminuirlo se si aumenta il drogaggio e si diminuisce la tensione (limite di Hoeneisen e Mead)
- l'energia immagazzinata dipende dalla capacità e questa è inversamente proporzionale allo spessore del gate

State of the Union: Commission sets out new ambitious mission to lead on supercomputing

Brussels, 18 September 2020

Today, the Commission takes further steps in the Digital Decade agenda to strengthen Europe's digital sovereignty, as announced by President Ursula **von der Leyen** in her State of the Union Address on Wednesday.

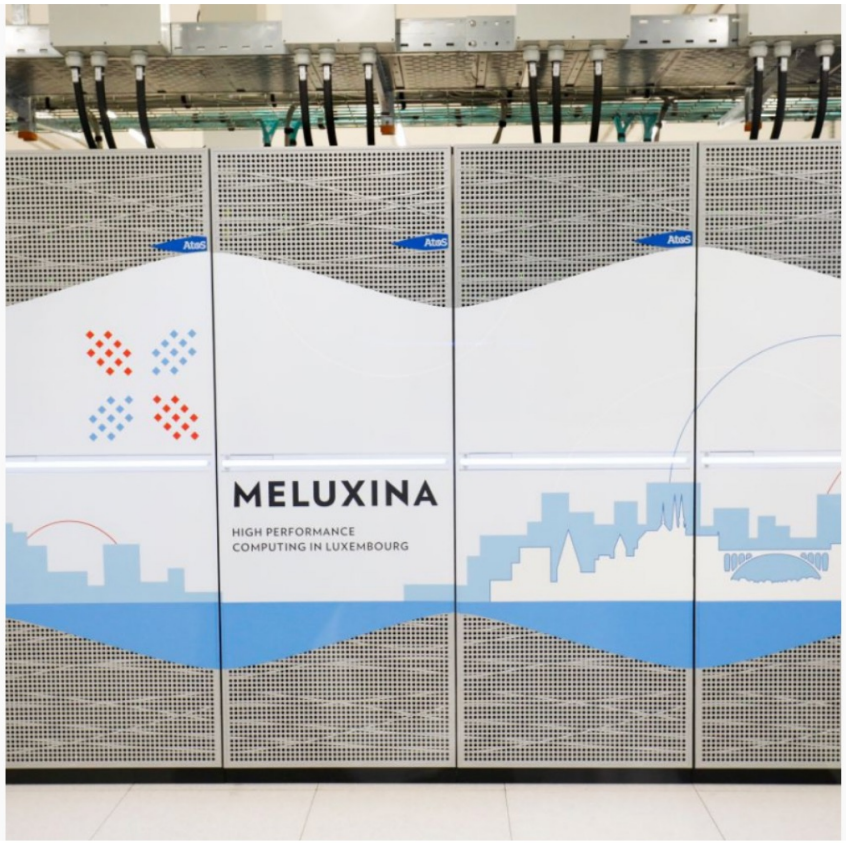
The Commission has proposed a new Regulation for the European High Performance Computing Joint Undertaking to maintain and advance Europe's leading role in supercomputing and quantum computing. It will support research and innovation activities for new supercomputing technologies, systems and products, as well as foster the necessary skills to use the infrastructure and form the basis for a world-class ecosystem in Europe. The proposal would enable an investment of €8 billion in the next generation of supercomputers – a substantially larger budget compared to the current one.

Building on Europe's success in next-generation high-performance computing, supercomputing will play a key role in Europe's path towards recovery. It has been identified as a strategic investment priority, and will underpin the entire digital strategy, from big data analytics and artificial intelligence to cloud technologies and cybersecurity. In addition, in a Recommendation also adopted today, the Commission calls on Member States to boost ultra-fast network connectivity and develop a joint approach to 5G rollout.

Tech Infrastructures

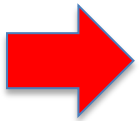
New EuroHPC JU: €7 billion for the acquisition of exascale supercomputers

Published on: 14/07/2021

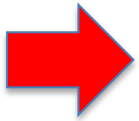


Top 500 – June 2021

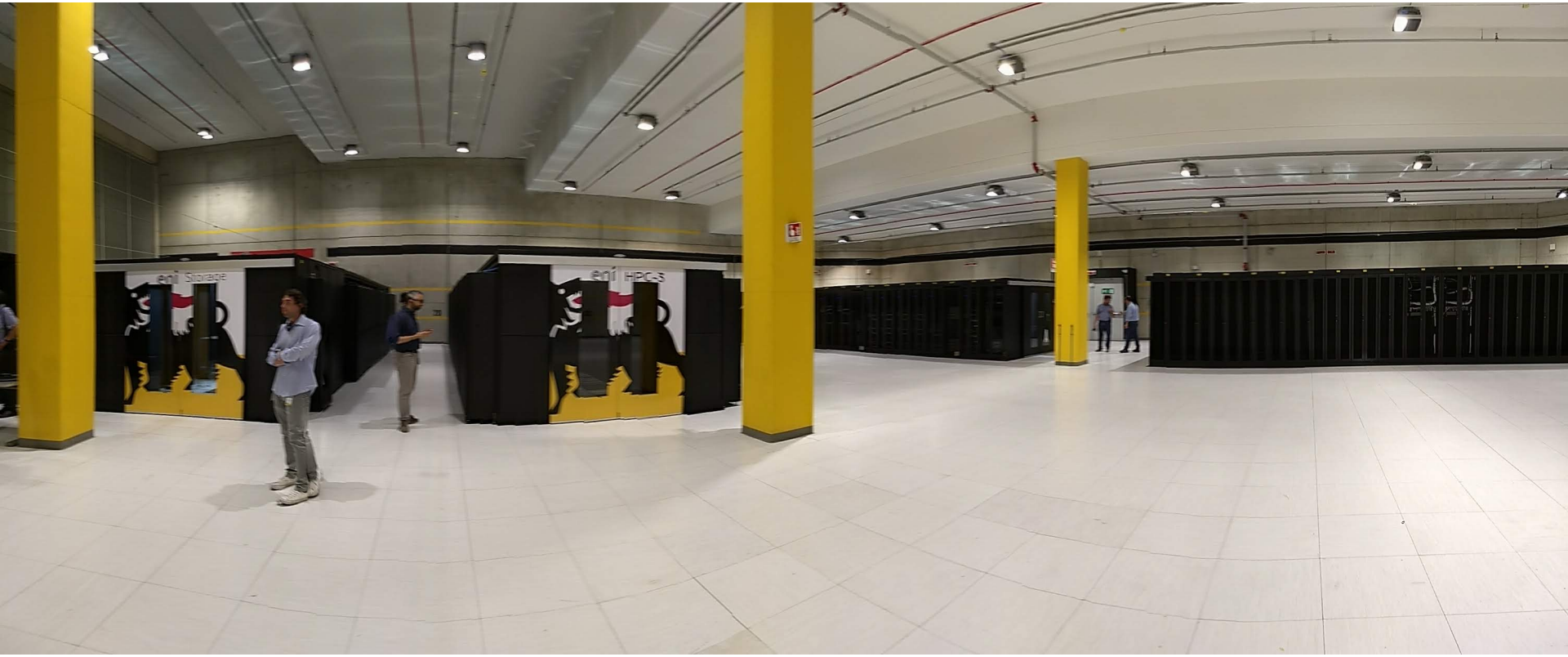
Rank	System	Cores	Rmax (TFlop/s)	Rpeak (TFlop/s)	Power (kW)
1	**Supercomputer Fugaku** - Supercomputer Fugaku, A64FX 48C 2.2GHz, Tofu interconnect D, Fujitsu RIKEN Center for Computational Science Japan	7,630,848	442,010.0	537,212.0	29,899
2	**Summit** - IBM Power System AC922, IBM POWER9 22C 3.07GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM DOE/SC/Oak Ridge National Laboratory United States	2,414,592	148,600.0	200,794.9	10,096
3	**Sierra** - IBM Power System AC922, IBM POWER9 22C 3.1GHz, NVIDIA Volta GV100, Dual-rail Mellanox EDR Infiniband, IBM / NVIDIA / Mellanox DOE/NNSA/LLNL United States	1,572,480	94,640.0	125,712.0	7,438
4	**Sunway TaihuLight** - Sunway MPP, Sunway SW26010 260C 1.45GHz, Sunway, NRCPC National Supercomputing Center in Wuxi China	10,649,600	93,014.6	125,435.9	15,371
5	**Perlmutter** - HPE Cray EX235n, AMD EPYC 7763 64C 2.45GHz, NVIDIA A100 SXM4 40 GB, Slingshot-10, HPE DOE/SC/LBNL/NERSC United States	706,304	64,590.0	89,794.5	2,528
6	**Selene** - NVIDIA DGX A100, AMD EPYC 7742 64C 2.25GHz, NVIDIA A100, Mellanox HDR Infiniband, Nvidia NVIDIA Corporation United States	555,520	63,460.0	79,215.0	2,646

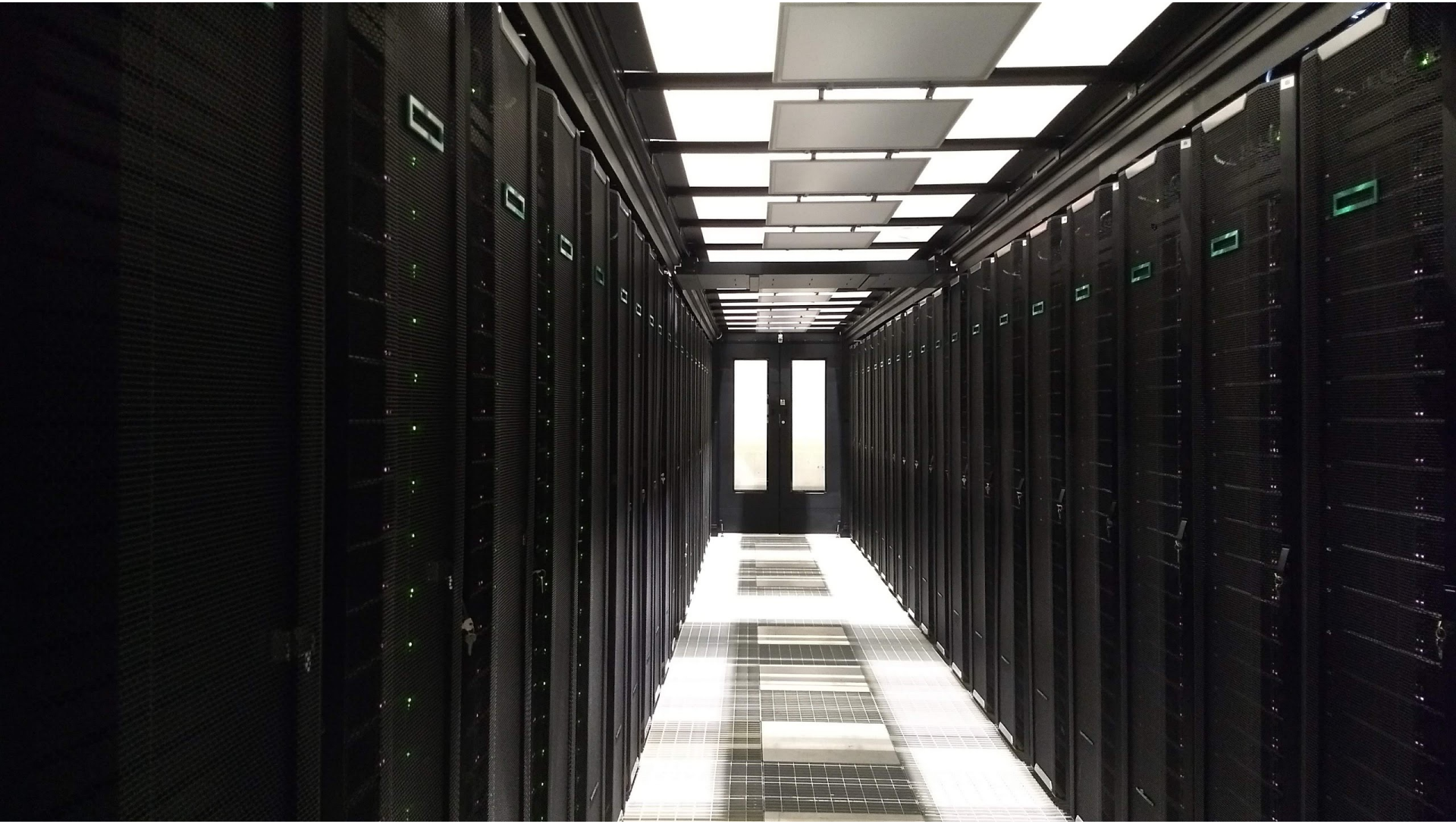


9	**HPC5** - PowerEdge C4140, Xeon Gold 6252 24C 2.1GHz, NVIDIA Tesla V100, Mellanox HDR Infiniband, Dell EMC Eni S.p.A. Italy	669,760	35,450.0	51,720.8	2,252
10	**Frontera** - Dell C6420, Xeon Platinum 8280 28C 2.7GHz, Mellanox InfiniBand HDR, Dell EMC Texas Advanced Computing Center/Univ. of Texas United States	448,448	23,516.4	38,745.9	
11	**Dammam-7** - Cray CS-Storm, Xeon Gold 6248 20C 2.5GHz, NVIDIA Tesla V100 SXM2, InfiniBand HDR 100, HPE Saudi Aramco Saudi Arabia	672,520	22,400.0	55,423.6	
12	**ABCI 2.0** - PRIMERGY GX2570 M6, Xeon Platinum 8360Y 36C 2.4GHz, NVIDIA A100 SXM4 40 GB, Infiniband HDR, Fujitsu National Institute of Advanced Industrial Science and Technology (AIST) Japan	504,000	22,208.7	54,341.0	1,600
13	**Wisteria/BDEC-01 (Odyssey)** - PRIMEHPC FX1000, A64FX 48C 2.2GHz, Tofu interconnect D, Fujitsu Information Technology Center, The University of Tokyo Japan	368,640	22,121.0	25,952.3	1,468
14	**Marconi-100** - IBM Power System AC922, IBM POWER9 16C 3GHz, Nvidia Volta V100, Dual-rail Mellanox EDR Infiniband, IBM CINECA Italy	347,776	21,640.0	29,354.0	1,476

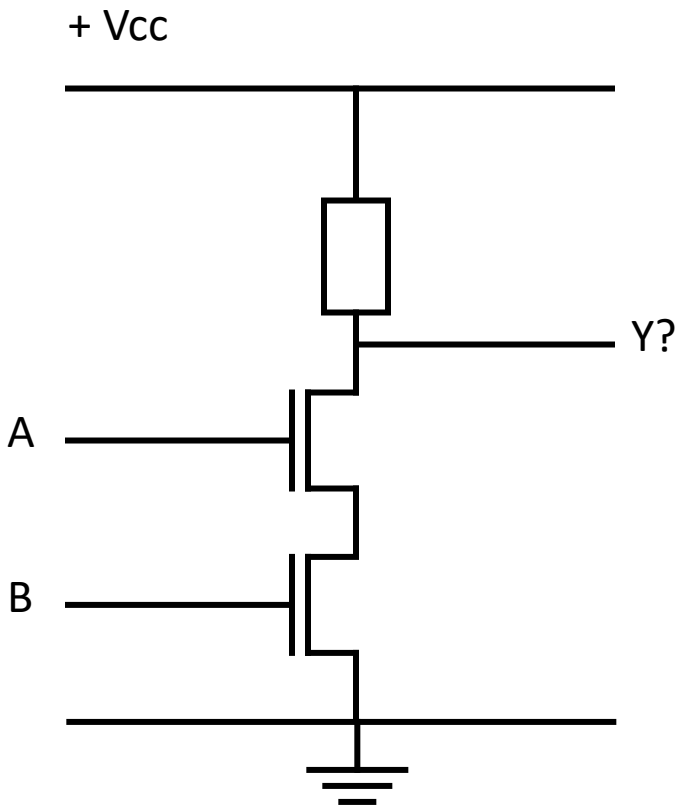


ENI Green Data Center


eni Storage
eni HPC5



Esercizio: se A, B, segnali logici (ossia segnali che possono essere alti – a tensione Vcc – oppure bassi – a tensione 0), che tipo di funzione logica viene eseguita da questo circuito in tecnologia MOS? Come si potrebbe costruire un equivalente circuito in tecnologia CMOS?



Ultimate physical limits to computation

Seth Lloyd

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Computers are physical systems: the laws of physics dictate what they can and cannot do. In particular, the speed with which a physical device can process information is limited by its energy and the amount of information that it can process is limited by the number of degrees of freedom it possesses. Here I explore the physical limits of computation as determined by the speed of light *c*, the quantum scale $\hbar$ and the gravitational constant *G*. As an example, I put quantitative bounds to the computational power of an 'ultimate laptop' with a mass of one kilogram confined to a volume of one litre.

Figure 1 The ultimate laptop. The 'ultimate laptop' is a computer with a mass of 1 kg and a volume of 1 l, operating at the fundamental limits of speed and memory capacity fixed by physics. The ultimate laptop performs $2mc^2/\pi\hbar = 5.4258 \times 10^{50}$ logical operations per second on $\sim 10^{31}$ bits. Although its computational machinery is in fact in a highly specified physical state with zero entropy, while it performs a computation that uses all its resources of energy and memory space it appears to an outside observer to be in a thermal state at $\sim 10^{9}$ degrees Kelvin. The ultimate laptop looks like a small piece of the Big Bang.