SVT-PISA standards

- **VME interface**
- **Fuse**
- **Transient suppressor**
- **Front panel leds**
- **PCB**
- **INIT_ integration**
- **Led driving**
- **VME common functions**
- **Software conventions**
- **Same chip**

SVT-PISA standards

details

- **VME interface:** common FSM + custom logic
  - implemented in all Pisa boards except HB
  - supports SW and BLT, in non-privileged and supervisory modes (AM = 9,b,d,f)
- **Fuse:** pico2 fuse (10A) (spring socket on PCB)
  - AM: still to be specified (maybe 2 separated VCC planes each with a 10A picofuse)
- **Transient suppressor:** motorola 1N5908 (ICTE-5) 1500 W peak power
- **Front panel leds:** some leds common to all boards, other specific.
  - common leds: power, dtack, SVTerror, error, ready (= RunMode), DS & HOLD for all cables
  - we use 2/3 leds packages from MENTOR
- **PCB:**
  - P0 and P3 footprint included in all boards, even if not needed, to maintain the possibility to solder the connectors if necessary
- **INIT_ integration:** the INIT_ is required active for at least 100nsec, an integration logic is implemented to avoid spurious glitches

SVT-PISA standards

details

- **Led driving:** driven by a monostable (74hc123) + logic to get continuos light for long signals
- **VME common functions:**
  - all RAMs are R/W from VME
  - all FIFOs are readable from VME and output FIFOs are also writeable
  - As a non-forcing rule, we tried to define registers with the same function at the same VME address in all the boards
- **Software conventions:** old C standard calls
  - names: merger_TmodeEnable(…)
  - parameters: MERGER_FIFODEPTH 1024
  - global functions: MERGER_DEFINE(…)
  - error codes: EXCEED_FIFO_LENGTH -102 (negative numbers from -100 and below)
- **Chip:** same chips model for same functions
  - Fifo: CY7C4245-10
  - Ram: KM681002B-10
  - Lvds: DS90C031 & 32
  - Abte: 74abte16245DL & 246DL