CLOCK SWITCH U13 116P SOIC

CLKSWTC

117P

VMECLK

REF

P3_CLOCK\I

U12 118P GL2CLK

CYGLUE2

P3_BUS<37..0>\I

P3_BUS<37..0>

P3

CLOCK

AMBUS<37..0>

SELADDR

P3ENABLE

22P

25P

LAY<2..0>

OPC<3..0>

ADD<13..0>

DATA<11..0>

DV<1..0>

SEL<1..0>

DONE

103P

105P

BOARD 1

BOARD 0

LAYER_UP<2..0>

OPCODE_UP<3..0>

ADDRESS_UP<13..0>

DATA_UP<11..0>

SEL_UP1_<0>

SEL_UP2_

DONE_UP_

DV_UP_

MODE<1..0>

LAYER_DW<2..0>

OPCODE_DW<3..0>

ADDRESS_DW<11..0>

DATA_DW<11..0>

SEL_DW_<3..0>

DV_DW_<3..0>

DONE_DW_

SELBOARD

138P

SEL_UP

TMODE

119P

121P

TEST

GL2CLK

REF

LAY2TO1<2..0>

OPC2TO1<3..0>

DT2TO1<11..0>

AD2TO1<11..0>

DONE2TO1

MODE<1..0>

SEL2TO1<3..0>

DV2TO1<3..0>

CLKRESET

AMBOARD_LOW_LEV_CONN

LAY<2..0>

OPC<3..0>

ADD_UP<13..0>

SEL_UP

DONE

DV_UP

OEP3

SELVME

VMECLK

SWTCH

TMODE

MODE<1..0>

VME_CHIP

RESET

OUTADD<13..0>

OUTDV

126P

IV1DAT<31..17>

XTCLK

OZ1

10MHZ

QUARTZOSCIL

129P

VCC

130P

127P

128P

4.7K

C74

133P

U15

131P

132P

MRESET

IV1DAT<31..24>

26P

VMEDT<31..0>

VMEDI<31..0>\I

GA_<4..0>

VMEADD<31..1>\I

VADD<31..1>

AM<5..0>\I

AM<5..0>

LWORD_\I

LWORD_

AS_\I

AS_

DS1_\I

DS1_

DS0_\I

DS0_

DTACK_\I

DTACK_

BERR_\I

BERR_

IACK_\I

IACK_

WRVME_\I

WRVME_

VME_BUS

IV2DAT<11..0>

IV1DAT<31..0>

IVGA_<4..0>

IVADD<31..27>

IVADD<23..1>

IVAM<5..0>

IVLWORD_

IVAS_

IVDS1_

IVDS0_

DTACK

BERR

IVIACK_

OEAB

OEBA

IVWRVME_

ENB

DLATCH

123P

IVGA_<4..0>

IVADD<31..27>

136P

GEOADDR

GA_<4..0>

VMEADD<31..27>

GEADD

PROMAD<15..0>

ENA_PROM

OEPROM

VMEADD<31..1>

AM<5..0>

LWORD_

AS_

DS1_

DS0_

DTACK

BERR

IACK_

OEAB

OEBA

WR

ENB

GO

115P

CAP

FILTER CAPACITORS

125P

LEDS

DTACK

TEST

MODE<1..0>

_DRAWING
AUTHOR=EMILIO MESCHI & FRIENDS
TITLE=AMBOARD_6_97
ABBREV=AMB597
LAST_MODIFIED=Tue Jul 29 10:06:14 1997