INPUT XEPLD BLOCK DIAGRAM. CORRESPONDS TO FIFO_CTR.ABL FIFO_REG.ABL EE_REG.ABL AND PARITY.PLD (VME_REG.ABL NOT INCLUDED). TIME FLOWS LEFT TO RIGHT

DRAWING
Tue Oct 15 11:20:10 1996

VMESS
TMODE
HREVME
HFEF_
POP
RESET
HFFF_
EERESET
INVADD
TRNCOU

N.B. FIFO IS NOT IN XEPLD, IT IS IN HERE ONLY TO SHOW THE TIMING

FIFO
REN_
C
Q
22 HFQ
HFREN_
FD
AND2
OR2
INV
84P

NEXT_S=0 OR NEXT_S=1

FIFO CTR FSM

NEXT_S =STATE IN THE NEXT CLOCK CYCLE

NEXT_S=1
HFQ22
INP END EVENT
FULL
LHREVME
FDR
FREGE
AND4
VMESS AND2

FIFO CTR FSM STATE DIAGRAM

STATE REGISTER: S=[IDLE,READY]

IDLE — NOT IDLE

RESET → S2 — POP → S0 (HFREN_= FULL) — NOT READY

FULL

NOT(HFEF_)

HFQ22 & NOT(HFEF_) → S3 — POP → S1 (FREGE=1, HFREN_= FULL) — READY

HFQ22 & HFEF_

EERESET

FDRE
FREG
21
LEP(FREG21)
EERESET
RESET

FREG

SSCE
SSCE=SSADD CLOCK ENABLE
FDP
PRE
IRECE_
IRE
SSADD
SS_D
INSPD
BUFT

FREGDV
SPYDV_

PARITY0-5
XORBUS
XOR2
GLPAR

8 FREG8 INP PARITY
9 FREG9 INP PARITY ERROR
11 FREG11 INP FIOV ERROR
12 FREG12 INP INVD ERROR
14 FREG14 INP TRNCOU ERROR

EE
EEPAER
EEFIOV
EEINVD
EETROU
OR3
75P

FIFO REGISTER
EE REGISTER