Abstract—In the framework of the INFN R&D projects CASIS and CASIS2, we are developing a new–concept VLSI front-end chip for the read-out of silicon calorimeters for high-energy astroparticle physics experiments. The ASIC has an input dynamic range of 52.6 pC (~11000 minimum ionizing particle, MIP) and features a new Charge Sensitive Amplifier (CSA) architecture, which uses a real-time automatic gain selection circuitry to switch between the input ranges of \([0 \div 500 \text{ MIP}]\) and \([0 \div 11000 \text{ MIP}]\). Following the CSA, a Correlated Double Sampling (CDS) shaper completes the front-end part. The final objective is to design and realize by 2008 a 16-channel chip with digitized outputs, which integrates one 12-bit Cyclic ADC per channel. We report on the design and tests of the second prototype (CASIS1.1) of the chip, which includes a revised and improved version of the Cyclic ADC with respect to that implemented in the first prototype (CASIS1.0).

I. INTRODUCTION AND MOTIVATION

The scope of the INFN CASIS and CASIS2 R&D experiments is to improve the present performance of Si-W calorimeters in view of the future, satellite-borne astroparticle physics experiments, which will measure the cosmic-ray flux well above the TeV region (see e.g. [1] – [3]).

One of the most delicate issues encountered is the lack of suitable front-end electronics required to read the large signals that develop in the calorimeters as a results of the electromagnetic and hadronic interactions of such high-energy particles. In the framework of CASIS and CASIS2, we are developing several prototypes of a VLSI front-end chip to address this problem. The final design objectives are to achieve a dynamic range larger than \(50pC\) (that is about \(10^4 \text{ MIP}\) for \(380\mu m\) thick silicon detectors), good noise performance \((S/N = 5\) for 1 MIP signals at \(300\mu F\) input load capacitance), linearity better than 1% and low power consumption (< 3mW/channel). Furthermore, to avoid driving low-level analog signals (which are obviously very sensitive to pick-up noise) from the output of the front-end chip to some external ADCs, the final chip will also feature one ADC/channel.

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II. FROM CASIS1.0 TO CASIS1.1

The first prototype of the chip (CASIS1.0) was designed and tested in 2005-2006. A thorough description of the CASIS1.0 complete architecture can be found in [4] and [5]; here we only recall some essential features of the chip in order to discuss the improvements introduced with the new version CASIS1.1. The design objectives of CASIS1.0 were to completely fulfill all the specifications mentioned in section I (in terms of dynamic range, noise, linearity and power consumption) for the front-end part (preamplifier/shaper). To allow for the very large design dynamic range, we had developed a new Charge Sensitive Amplifier (CSA) architecture, based on a real-time automatic gain selection circuitry that switches between two input ranges: a “High-Gain” range of \([0 \div 500 \text{ MIP}]\) and a “Low-Gain” range of \([0 \div 11000 \text{ MIP}]\). The CSA is followed by a Correlated Double Sampling (CDS) shaper. Furthermore, a feasibility test for the integration of one ADC per channel was carried out to provide a starting point for future upgrades of the device: hence, a 12-bit, switched-capacitor fully differential cyclic ADC was also designed and integrated in the prototype (see fig. 1 for a block scheme of the ADC).

![Fig. 1. Simplified block scheme of the Cyclic ADC.](image-url)

The CASIS1.0 architecture featured five complete front-end/ADC channels and one additional stand-alone ADC. The results of the measurements performed on the CASIS1.0 prototype had shown that the front-end section of the chip (CSA + CDS) actually fulfilled all the above mentioned design...
specifications [4], [5]. Therefore, the front-end section of the chip has virtually not been modified in the new CASIS1.1 prototype, apart from minor improvements in the CSA feedback and control networks. On the other hand, the tests of the first version of the ADC have demonstrated some problems (namely, percentage of working channels ~ 50% and high power consumption in the non-working channels), which careful circuit analysis and Monte-Carlo simulations have shown to be due to the effects of the random device mismatch on the biasing scheme of the output buffers of the differential operational amplifiers used in the ADC [5]. Therefore, in the new prototype CASIS1.1 we have focused essentially on the ADC, in order to solve the above mentioned problems and to pertain to a satisfactory overall performance in view of the “final” chip version, which we aim at designing by 2008.

Fig. 2(a) sketches the architecture of the Diff. Opamp implemented in the CASIS1.0 ADC (see also fig. 1). It was based on an input differential telescopic cascode amplifier and a class AB output amplifier buffer. In ideal conditions, the voltage at the outputs of the input differential amplifier are balanced around the bias potential $V_{b1}$, thus they can be used to bias the output buffer. In a real situation, instead, device mismatches create an unbalance, which increases or lowers the mean value of $V_{dn}$ and $V_{dp}$, generating a corresponding reduction or rise of the current in the output buffer branches. As a result, the common mode feedback ceases to function and the power consumption could reach very high (or low) values. To solve the problem, we revised the design of the Diff. Opamp, providing a common mode feedback also for the input differential amplifier. This is implemented in the new CASIS1.1 chip by adding two transistors and resizing the current mirror biasing device, as highlighted (in red) in fig. 2(b).

![Fig. 2(a). Simplified schematic diagram of the Diff. Opamp implemented in the ADC of the chip CASIS1.0.](image)

Moreover, we studied also an alternative solution for the Diff. Opamp architecture, in case the above described design would not perform as expected. This second solution is based on a single-stage cascode Operational Transconductance Amplifier (OTA), illustrated schematically in fig. 3. Since with a single-stage amplifier it was not possible to achieve the high open loop gain required for 12-bit resolution, we used the “gain-enhancement” technique [6] to boost the DC gain of the amplifier. Simulation results give for the open-loop DC gain of the OTA Diff. Opamp with gain enhancement illustrated in fig. 3 a value of 112 dB.

![Fig. 2(b). Revised input differential amplifier circuit as implemented in 6 ADC channels of CASIS1.1.](image)

![Fig. 3. Simplified schematic of the OTA Diff. Opamp with gain enhancement used in 3 ADC channels of the CASIS1.1 chip.](image)

Fig. 4 is a micrograph of a die of the CASIS1.1 integrated circuit. The chip features two complete analog channels (double-gain CSA, CDS and output buffer) and nine ADC channels. Six ADC channels (labelled “Type N” and “Type F” in fig. 4) are built using the revised two-stage Diff. Opamp of fig. 2, while three ADCs (labelled “Type O” in fig. 4) use the gain-enhanced differential OTA sketched in fig. 3. The difference between Type N (for “Normal”) and Type F (for
“Fast”) lies in the fact that the latter version has been optimized for speed by reducing the channel length of the transistors in the active load of the input differential amplifier and in the output buffer (see fig. 2(a)). The chip has been designed and realized with the 0.35\(\mu\)m C35B4 CMOS technology of Austria Micro Systems [7], which provides two polysilicon and four metal layers, with a power supply voltage of 3.3\(V\).

III. EXPERIMENTAL RESULTS

An ad-hoc designed printed circuit board has been realized to accommodate the chip under test (encapsulated in a CQFP64 package) in a socket, and to provide all necessary supply and bias voltages and currents. Charge could be injected into any (or both) of the 2 front-end channels by means of a pulse generator and a set of calibrated test capacitors. Another set of calibrated capacitors could be shunted at the preamplifier’s input to simulate various detector capacitive loads. A 16-bit external ADC is used to perform the linearity and noise measurements on the front-end channels, while a 16-bit DAC is used to characterize the ADC response. Moreover, the buffered outputs of the 2 analog chains can be connected to the input of any ADC channel, thus enabling the test of the entire chain.

Table I summarizes these results.

| ENC (rms) | 2280\(e\) + 8\(e\)/(pF) |
| CSA open loop gain | > 110dB |
| Power consumption | 2.8mW/channel |
| Measured sensitivity (High-Gain) | 2.95mV/MIP |
| Measured sensitivity (Low_gain) | 146\(\mu\)V/MIP |
| Max non-linearity (High-Gain) | 0.3% |
| Max non-linearity (Low-Gain) | 0.6% |
| Max dynamic range (Low-Gain) | \(~10000\) MIP or \(52.6\mu\)C |

B. Cyclic ADC

The characterization of the ADC, at the time this paper is being written, is still under way. Therefore, we present hereafter only preliminary and partial results.

The first test that was performed on the ADCs was a fast functionality and power consumption measurement aimed at ensuring that the random device mismatch problem that affected the previous version had been solved. The result of this test has shown that all 171 ADC channels of the 19 chips measured function normally (i.e. all of them convert correctly) and display a normal power consumption (that is about 4mW for Type N and Type O and about 5mW for Type F). This result clearly indicates that both versions of the ADC are immune to the macroscopic device mismatch effects that affected the previous version.

Fig. 5(a). Response of the 9 ADCs of one chip to low-level input signals injected into the input of one front-end channel of the same chip.

Fig. 5(b). Response of the 9 ADCs of one chip to large input signals injected into the input of one front-end channel of the same chip.
Fig. 5 shows linearity measurements performed by connecting (via the printed circuit test board) the buffered output of a front-end channel of one chip to all the ADC channels of the same chip. Fig. 5(a) was obtained by injecting into the input of the front-end channel a series of small signal charges (from 2 to 30 MIP), while fig. 5(b) displays the result of a similar measurement, performed this time by injecting large input signals into the CSA input. All nine ADCs respond correctly to the signal levels from the CDS shaper and display a nicely linear behavior. More precise linearity measurements are under way to quantitatively assess the actual linearity performance of the ADCs.

Concerning the ADC resolution, the first, preliminary indications are also quite encouraging. Fig. 6 shows the response of the nine ADC channels of one chip to an input level, provided by a 16-bit external DAC, which was varied in steps of 400µV.

This test is quite significant, because the ADC design range is 1.7V and for a 12-bit resolution one should have a value of 415 µV for 1-bit. As it is clearly seen in the plot, all ADCs react to the input step by incrementing the counting by 1 channel, thus showing the the gain of the Diff. Opamps is compatible with the design resolution.

IV. SUMMARY AND OUTLOOK

The second prototype (CASIS1.1) of a VLSI front-end chip intended for the read-out of silicon calorimeters has been designed, produced and is being tested in the framework of the INFN R&D project CASIS2. The prototype features two front-end channels (which include a double-range CSA with a real-time network for feedback control, a CDS filter and an output buffer) and nine channels with fully differential, switched capacitor cyclic ADC, implemented around two alternative Diff. Opamp architectures.

Measurements on the front-end section have demonstrated a dynamic range of 52.6 pC, an ENC of 2280 e- rms + 8 e-/pF, a very good linearity and a power consumption of 2.8mW/channel.

Tests on the ADC channels are still under way at the time this paper is being written and they must be completed before we can assess the actual ADC performance (linearity, missing codes, etc.). From the preliminary results available at this time we can nonetheless conclude that:

1. The random device mismatch problem that affected the previous version of the ADC has been solved, since a fast functionality test performed on all chips (171 ADC channels) showed that 100% of the ADCs convert correctly and display the expected power consumption.
2. Preliminary indications are consistent with the expected 12-bit resolution.

On the basis of the results on this second prototype, we are confident to be able to design the final chip version (CASIS1.2) with 16 channels and one ADC per channel by 2008.

REFERENCES