PCI Test Adapter Card

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Preliminary

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This document provides hardware details for a proposed PCI based Test Adapter for BTeV

For electronic copies of this document access the web at URL:
http://www-ese.fnal.gov/ESEPROJ/BteV/TestStands/PCI_Test_Adapter.doc
http://www-ese.fnal.gov/ESEPROJ/BteV/TestStands/PCI_Test_Adapter.pdf

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1 PCI Test Adapter Card

The BTeV Test Stands are used to facilitate development and testing of the individual components of the entire system. The BTeV Test Stand will be a convenient and efficient way to perform component level debugging throughout the entire design and development stages. The test stands will all be built to identical specifications, yet contain the flexibility the user needs to customize their test stand to satisfy their own individual requirements. Additionally, during the development stage, the test stand can be used for software development and sub-system integration tests. Finally, during the production stage, the test stand will allow each individual component to be tested before it is introduced into the overall system.

The BTeV-Standard Test Stand will be equipped with a workstation, a standard PC, or an industrial PC. The computers will be selected to accept standard PCI-Based plug in cards. The PCI Test Adapter cards will have user programmable parts that provide designers the flexibility to interface with the various components of the overall system. The computer along with the PCI Test Adapter (known as PTA from here on out) will be used together with custom daughter cards that will interface the PTA with come subsystem or device under test allowing for a flexible platform to build small DAQ and test small detector subsystems. Figure 1 shows a picture of the PCI Test Adapter Card. Figure 2 shows a drawing of the PTA with its major components and features highlighted.

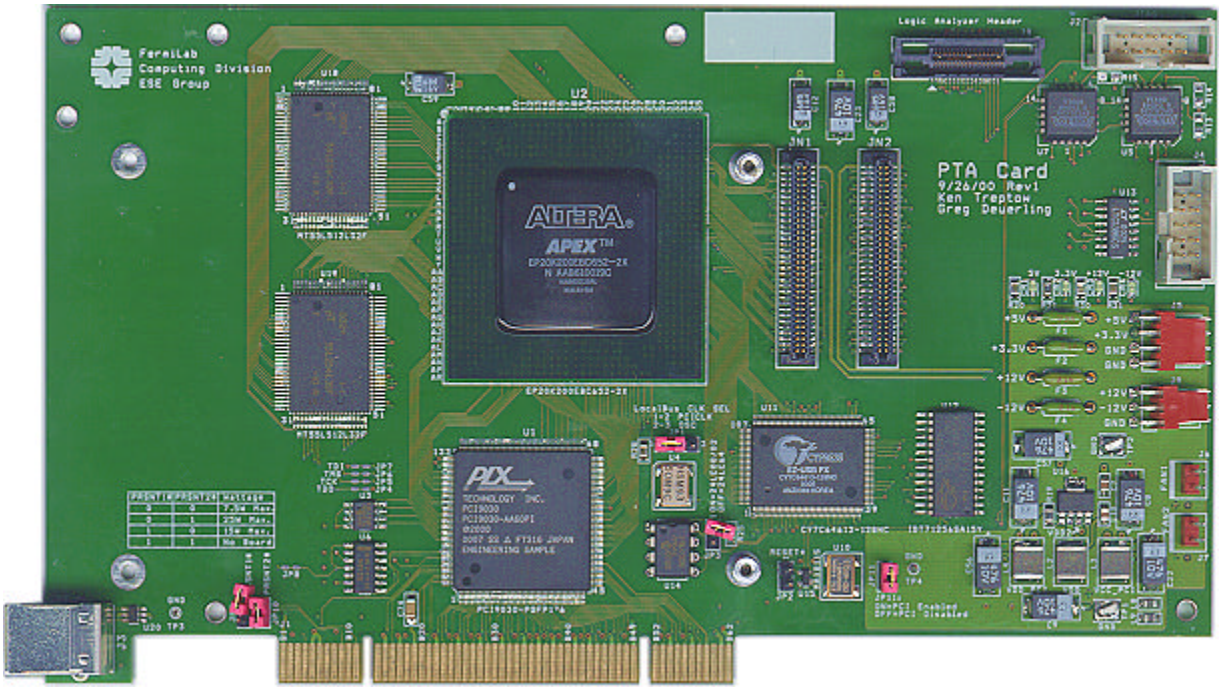


Figure 1

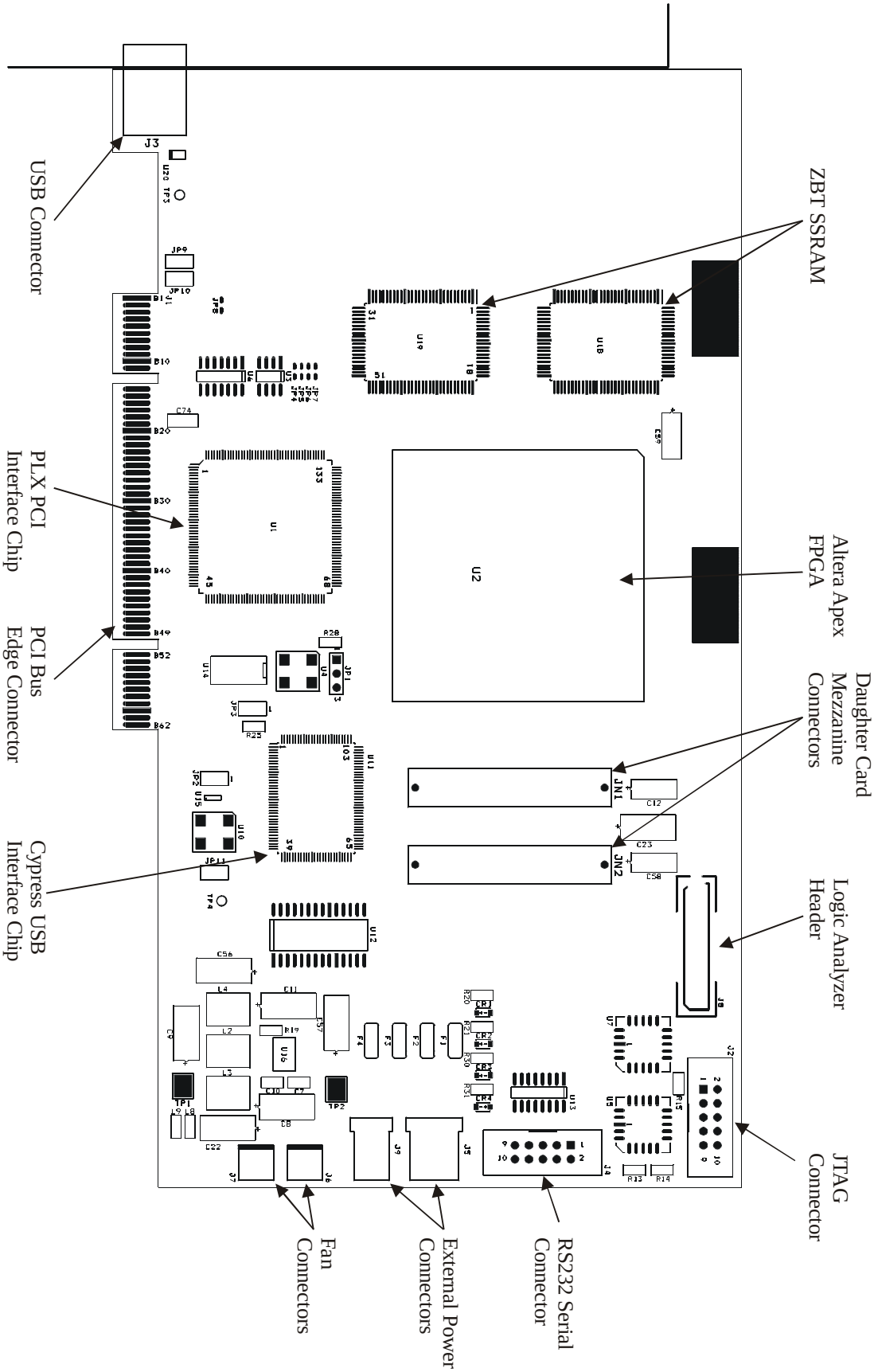

USB Connector
ZBT SSRAM
PLX PCI
Interface Chip
Altera Apex
FPGA
PCI Bus
Edge Connector
Daughter Card
Mezzanine
Connectors
Cypress USB
Interface Chip
Logic Analyzer
Header
JTAG
Connector
Fan
Connectors
External Power
Connectors
RS232 Serial
Connector

Figure 2

1.1 PCI Test Adapter Card Features

The PCI Test Adapter (PTA) card has the following features:

- FPGA controlling all functions for flexibility.
- PCI target interface (slave only).
- Two SRAM banks of 2 MB each.
- Daughter card interface for all links using IEEE 1386 Mezzanine connectors.
- JTAG interface.
- USB Interface

Figure 3 shows the block diagram of the PCI Test Adapter (PTA) card. For datasheets of the PTA components see the appendix.

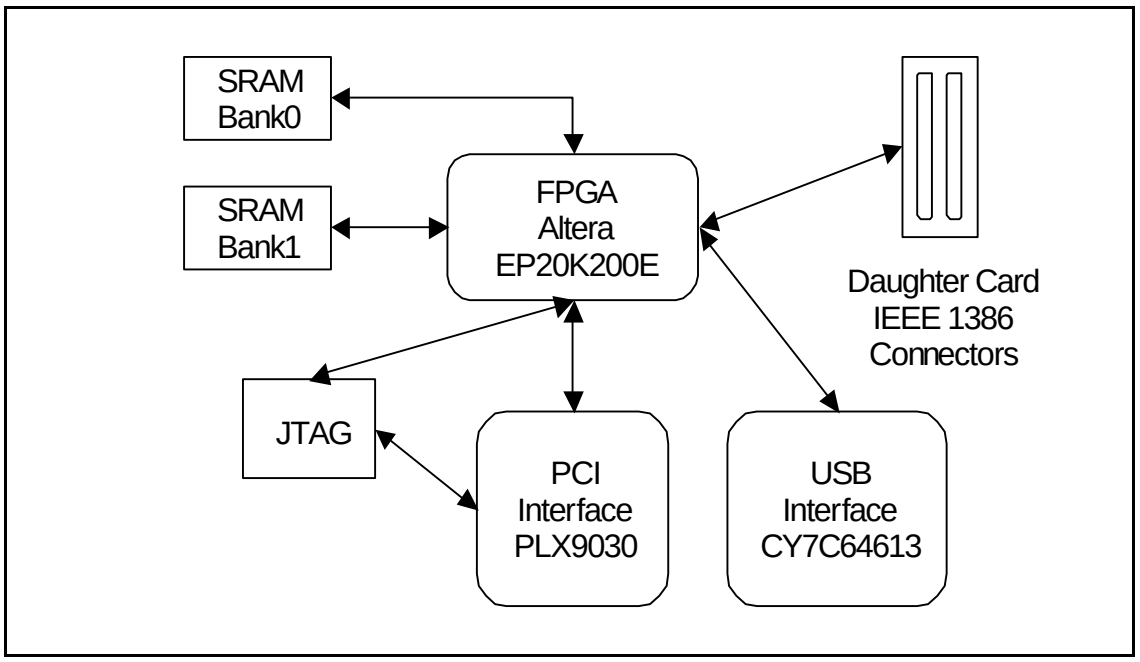


Figure 3

1.2 FPGA Board Controller

All board interfaces are connected to the Altera APEX EP20K200E FPGA to allow for maximum flexibility. The EP20K200E is a 652 pin BGA device that has a maximum of 526,000 system gates. If a device with a larger gate count is needed any one of the 652Pin BGA 20KE APEX chips will work. Currently the biggest device available is the EP20K1500E.

1.3 PCI Interface

The PCI interface is a PLX 9030 from PLX Technology. It is a 32Bit, 33MHz Slave interface chip with a local bus that can be run up to 60MHz connected to the Altera FPGA.

1.4 SRAM Interface

The current PTA design has two independent banks of Micron 256K x 32 ZBT SSRAM. The memory interface was designed to allow for larger ZBT memories that will be available in the future. Currently the 512K x 32 chips are sampling and will be out soon. The 1M x 32 chips are in the works and will be out sometime in late 2001 or early 2002.

1.5 Daughter Card Interface

The daughter card interface utilizes the mechanics defined in IEEE P1386/Draft 2.2, 22-Apr-00 (Draft Standard for a Common Mezzanine Card Family: CMC). The CMC connectors are connected directly to the Altera EP20K200E FPGA to allow for custom interface circuits for each different daughter card.

1.6 JTAG Interface

The JTAG interface allows for device configuration, boundary scan testing and PCB conductivity testing.

1.7 USB Interface

A USB interface using a Cypress CY7C64613 micro controller is included on the PTA. The USB chip is connected to the FPGA and is intended to control the PTA card when it is not installed in a PC.

2 Hardware Description

2.1 PLX PCI9030 PCI Target Interface

The PCI9030 target interface provides a data path between the PCI9030 and 33Mhz 32bit PCI system bus. When a computer with a PCI card installed is booted up the computer goes through a auto configuration cycle that reads a predefined header region from each installed PCI card. This region consists of fields that uniquely identifies the PCI card and allows the card to be generically controlled. The predefined header portion of the configuration space is divided into two parts. The first 16 bytes are defined the same for all types of devices. The remaining bytes can have different layouts depending on the base function that the PCI card supports

After the PCI card has been configured by the computer, software can be written to scan each slot to look for the PTA's Vendor and Device ID. The PTA card will have the following unique VendorID, DeviceID, SunsystemID, and SubsystemVendorID:

DeviceID	VendorID	Location
0x9030	0x10B5	0x00

SubsystemID	SubsystemVendorID	Location
0x0001	0xCE5E	0x2C

The VendorID of 0x10B5 identifies PLX as the manufacturer of the PCI target interface chip and the DeviceID of 0x9030 is the part number of the PCI target chip. The SubsystemVendorID of 0xCE5E identifies that the Computing Divisions ESE group designed this card and the SubSystemID of 0x0001 is the number used to identify the PTA card. For a complete memory map of the PCI configuration registers see the PCI9030 data sheet.

The PCI9030's registers are loaded at power up from a 2K bit serial EEPROM. This EEPROM holds the configuration information for all of the PCI9030's base address regions and local bus interface. The EEPROM also holds the PTA's serial number, PCB revision level, and the PCB modification level. The table below shows these details:

PTA Information Register			
31 - 24	23 - 16	15 - 0	EEPROM Address
PCB Mod Level	PCB Revision Level	PTA Serial Number	0xc0

2.2 PLX PCI9030 Local Bus

The local bus provides a data path between the PLX9030 and the Altera EP20K200E. The local bus clock can be anything up to 60MHz and is independent of the PCI bus clock. The PTA's local bus clock can be configured to run from the PCI clock, or an on board oscillator. JP1 on the PTA card selects which clock is used.

The PLX local bus interface uses a 32 bit multiplexed address/data bus. The PLX local bus is very versatile and configurable and has far to many features to describe here, so consult the PLX9030 data sheet for complete information. The PLX9030's local bus is broken into four base-address regions. These regions are configured at power up with a EEPROM that is connected to the PLX9030. The PTA's base address regions have been configured as follows:

Base Address Region	Function	Size
BAR2	PTA Configuration Registers	32K Byte
BAR3	ZBT SSRAM Bank0	1M Byte
BAR4	ZBT SSRAM Bank1	1M Byte
BAR5	Daughter Card Interface	64K Byte

All base address regions are configured for 32bit memory mapped word aligned addressing. The base address regions are assigned physical addresses at power up when the PC BIOS initializes the PCI bus.

2.3 ZBT SSRAM Interface

The PTA has 2 banks of Micron ZBT SSRAM. Each bank has its own address, data, and control lines so both banks can be accessed simultaneously. How the mezzanine card designer accesses the memory will differ from design to design. The default PTA configuration will allow access to the memory from the PCI bus and from the CMC daughter card interface. Bits in the ZBT SSRAM control register (BAR2, offset 0x08) determine who has control of the memory, PCI or mezzanine card. The PCI interface uses BAR3 and BAR4 of the PLX chip to access the two banks of memory. The mezzanine memory interface has several registers associated with it, a address pointer register, a limit register, and a status register. These registers are planned for memory control from the PTA daughter card that is running a data acquisition application. The address pointer register holds the address of the current memory access. The limit register is used as a programmable threshold that will set a bit in the memory status register when crossed. The status register shows that current status of both banks of memory, full, empty, and so on. Complete information on how to interface to a ZBT SSRAM can be found on the Micron website listed in the appendix.

2.4 Daughter Card Interface

The CMC daughter card interface has been designed with flexibility in mind. The Jn1 and Jn2 connectors (see figure 2 for location) have 72 signal pins which are connected directly to the Altera EP20K200E chip. These 72 pins can be configured as the engineer needs them and can

operate at various different logic levels. See the Altera APEX data sheet for complete information on the APEX's capabilities. The daughter card connectors has nine fixed purpose pins, CLK2, CLK2LK, CLK2FB, CLK4, TDI, TCK, TMS, TDO, and EEDATA.

The three CLK2 pins are connected to the EP20K200E's PLL2ClockLock/ClockBoost circuit. Of the two clocks on the daughter card connectors, CLK2 is the most configurable. If a daughter card design does not need to supply a clock to the PTA card or need the clock lock or boost pins the three signals can be used as I/O pins. CLK4 goes to a PLL but it has no feedback or clock lock pins. As with CLK2, if not needed CLK4 can be used as a I/O pin.

The four signals TDI, TCK, TMS, and TDO are used to drive a JTAG chain on a mezzanine card. These four signals are controlled via four bits in the PTA's configuration register (BAR2, Offset 0x00). In the IEEE 1398 mezzanine card specification these four pins are defined as BUSMODE pins. The BUSMODE pins were used to tell the motherboard if a mezzanine card was present and what protocols it supported. It was decided that JTAG was more useful than following the IEEE 1398 specification of the BUSMODE pins. The BUSMODE pins could easily be implemented if needed, but the JTAG pins would be lost.

The EEDATA pin is used by the PTA to access a Dallas Semiconductor 1-Wire EEPROM that will be on all PTA daughter cards. We will be using the Dallas DS2430A device. The EEPROM has three blocks, a unique 64bit factory serial number, a 256bit data EEPROM block, a one time programmable 64bit application register, and a 8bit status register. We will use the 64bit application register to store our own daughter card serial number, daughter card type, and PCB revision level. The first location in the EEPROM block will hold a PCB modification level number that will be incremented with each hardware modification to the PTA's PCB. At some time a system will be put in place for people outside of the ESE group to obtain the 8-Bit daughter card type number. The EEDATA pin is a bit in the PTA configuration register (BAR2, bit 0). For information on how to access the DS2430A device go to the Dallas website listed in the appendix. The table below shows the details of the factory serial number register and the application register:

64-Bit Factory Serial Number		
63 - 56	55 - 8	7-0
8-Bit CRC Code	48-Bit Serial Number	8-Bit Family Code (14H)

64-Bit Application Register			
63 - 32	31 - 24	23 - 16	15-0
X	8-Bit PCB Revision Level	8-Bit Card Type	16-Bit Serial Number

1st 8-Bits of EEPROM
7-0
8-Bit PCB MOD Level

Table 1 below shows the pin out of the Jn1 and Jn2 daughter card connectors. All signals on these connectors are connected directly to the Altera Apex chip. For the pin numbers of the corresponding pins on the Altera Apex chip see the PTA schematics or use Altera's Quartus software to see how the pins were assigned in the default PTA configuration.

Jn1			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
1	JN1_S0	2	-12V
3	Ground	4	JN1_S1
5	JN1_S2	6	JN1_S3
7	TDI	8	5V
9	JN1_S4	10	JN1_S5
11	Ground	12	JN1_S6
13	CLK2	14	Ground
15	Ground	16	CLK2LK
17	CLK2FB	18	5V
19	3.3V(I/O)	20	JN1_S7
21	JN1_S8	22	JN1_S9
23	JN1_S10	24	Ground
25	Ground	26	JN1_S11
27	JN1_S12	28	JN1_S13
29	JN1_S14	30	5V
31	3.3V(I/O)	32	JN1_S15
33	JN1_S16	34	Ground
35	Ground	36	JN1_S17
37	JN1_S18	38	5V
39	Ground	40	JN1_S19
41	JN1_S20	42	JN1_S21
43	JN1_S22	44	Ground
45	3.3V(I/O)	46	JN1_S23
47	JN1_S24	48	JN1_S25
49	JN1_S26	50	5V
51	Ground	52	JN1_S27
53	JN1_S28	54	JN1_S29
55	JN1_S30	56	Ground
57	3.3V(I/O)	58	JN1_S31
59	JN1_S32	60	JN1_S33
61	JN1_S34	62	5V
63	Ground	64	EEDATA

Jn2			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
1	12V	2	JN2_S0
3	JN2_S1	4	JN2_S2
5	JN2_S3	6	Ground
7	Ground	8	JN2_S4
9	JN2_S5	10	JN2_S6
11	TCK	12	3.3V
13	JN2_S7	14	TMS
15	3.3V	16	TDO
17	JN2_S8	18	Ground
19	JN2_S9	20	JN2_S10
21	Ground	22	JN2_S11
23	JN2_S12	24	3.3V
25	JN2_S13	26	JN2_S14
27	3.3V	28	JN2_S15
29	JN2_S16	30	Ground
31	JN2_S17	32	JN2_S18
33	Ground	34	JN2_S19
35	JN2_S20	36	3.3V
37	Ground	38	JN2_S21
39	JN2_S22	40	Ground
41	3.3V	42	JN2_S23
43	JN2_S24	44	Ground
45	JN2_S25	46	JN2_S26
47	Ground	48	JN2_S27
49	JN2_S28	50	3.3V
51	JN2_S29	52	JN2_S30
53	3.3V	54	JN2_S31
55	JN2_S32	56	Ground
57	JN2_S33	58	JN2_S34
59	Ground	60	JN2_S35
61	JN2_S36	62	3.3V
63	Ground	64	CLK4

= Programmable I/O = Fixed Purpose Pin = Power Pin = Ground Pin

Table 1

2.5 Logic Analyzer Header

The PTA has a single logic analyzer connector that is compatible with Hewlett Packard's 16500 series logic analyzers high density probe adapters. The header has 32 signal pins and 2 clock pins. All 34 signals go directly to the Altera EP20K200E and can be configured to monitor any thing within FPGA. See figure 2 for connector location.

2.6 PTA JTAG Interface

The PTA's JTAG interface chain consists of three devices, 2 EPC2 boot devices and a APEX EP20K200E. The chain can be accessed from the 10 pin JTAG connector (J2) or from the PCI bus via general purpose IO bits in the PLX PCI9030 PCI interface chip. The devices in the JTAG chain can be programmed and verified from either source. The device order in the PTA JTAG chain is shown in figure 4.

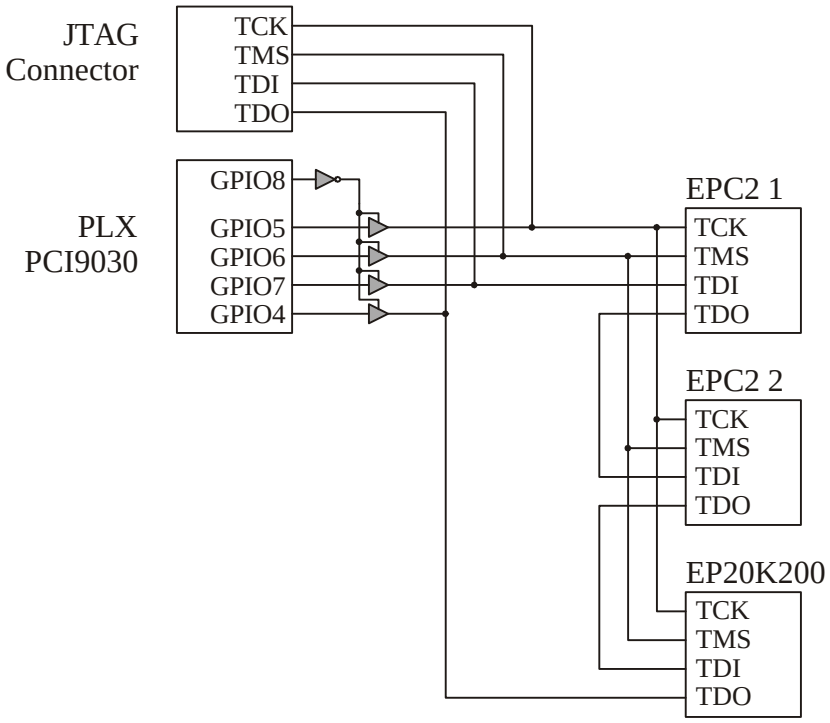
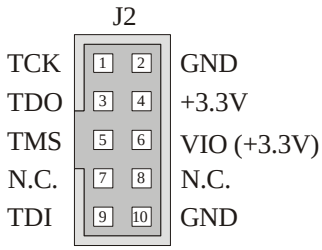


Figure 4

The JTAG connector uses a standard Altera ByteBlasterMV pinout. Since this is a low voltage card, only a ByteBlasterMV can be used. If a standard 5V ByteBlaster is used the parts in the JTAG chain could be damaged. The drawing below shows the ByteBlasterMV JTAG pinout:



As mentioned above, the PCI9030 can control the JTAG chain via 5 general purpose I/O pins. On power up the GPIO8 pin is tri-stated and will disable the PCI9030 from driving the JTAG chain. To enable the PCI9030 to drive the JTAG chain GPIO8 must be configured as a output, then GPIO8 must be cleared (zero) to get control of the JTAG chain. GPIO5-GPIO7 must be configured as outputs, and GPIO4 must be configured as a input. See section 6 in the PCI9030 data book for information on the PCI9030 registers used to control these 5 pins. The industry standard JTAG programming language is called JAM. Source code for a JAM player can be downloaded from Altera's web site (see appendix) and ported to work with the GPIO's on the PTA. The device programming files generated by Altera's Quartus need to be converted to JAM files before they can be used by the JAM player.

2.7 Mezzanine Card JTAG Interface

The Mezzanine JTAG interface will be used to program any JTAG compatible programmable logic devices that may be present on a mezzanine card. The TMS, TCK, TDI, and TDO signals are controlled via four bits in the PTA's control register (BAR2, Offset 0x00). As mentioned above in the PTA JTAG interface paragraph, a JAM player will be used to program and configure any logic devices.

2.8 PTA Option Jumpers

There are eleven option jumpers on the PTA.

JP1 – Selects the PLX local bus clock. Pins 1-2 (default) select the 33MHz PCI clock, pins 2-3 select a oscillator mounted on the PTA PCB.

JP2 – JP2 is a reset for the USB interface chip. If no jumper is on the USB chip runs as normal, if the jumper is "ON" the USB chip is held in reset.

JP3 – Selects what type of boot EEPROM is used on the USB chip. No jumper selects a 24LC64, if the jumper is installed a 24LC00/02 is selected. The initial PTA design uses a 24LC00/02 chip.

JP4 to JP8 – These jumpers are hardwired with traces on the PTA's PCB. These traces connect the USB chip to the JTAG chain so the 8051 micro controller in the USB chip can program the

Altera EP20K200E FPGA. If for some reason the USB chip is adversely affecting the JTAG chain we put in the option of removing it from the chain.

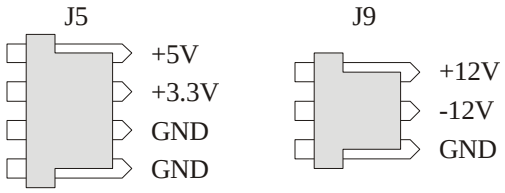
JP9 to JP10 – The PTA uses these two jumpers to tell the PCI controller on the PC motherboard its power requirements. The jumpers hook up to the PRSNT1# and PRSNT2# on the PCI bus and are part of the PCI 2.2 specification. The table below shows the four different settings:

PRSNT2# JP9	PRSNT1# JP10	Wattage
OFF	OFF	7.5W Max.
OFF	ON	15W Max.
ON	OFF	25W Max.
ON	ON	No Board

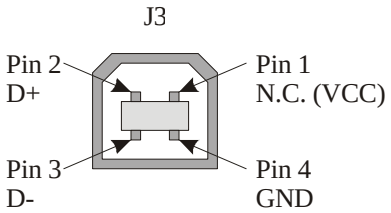
JP11 – Disables and enables the PLX9030 PCI chip. With jumper installed the PLX chip is enabled, when off the PLX chip is disabled. The PTA was designed to be able to function outside of a PC via a USB interface. When using the USB interface the PLX chip should be disabled.

2.9 Miscellaneous Connector Pin Outs

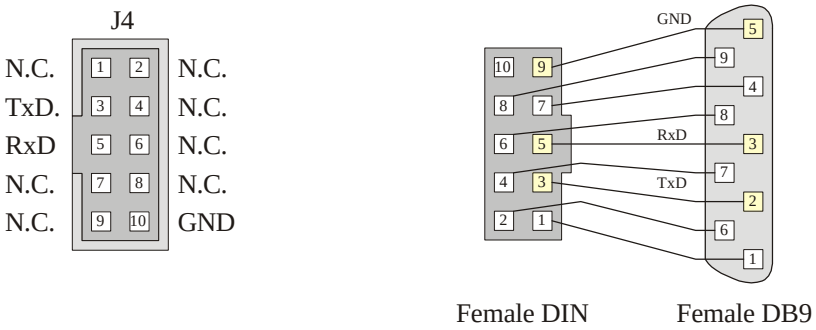
As mentioned in previous sections the PTA can be operated externally of a PC via a USB interface. Two connectors are provided to power the PTA from an external power supply. For normal operation all that is needed it +3.3V. The other voltages are not used by the PTA but are there for the daughter card interface to use. The figure below shows the pin out of the external power connectors J5 and J9:



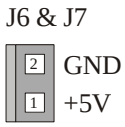
The PTA's USB port can be connected to any USB controller, PC, Mac, … The USB spec. allows a device to power it self from the VCC pin (pin 1) on the USB connector. The power requirements of the PTA will not allow this, pin 1 is not connected. The USB connector is pictured below:



The Cypress USB interface chip has a serial port that can be used when debugging software. To save space on the PTA card a 10 pin DIN connector was used instead of a DB9. The figure below shows the connector pin out and how to make a cable with a DB9 connector:



If a daughter card is running hot and needs additional cooling, two connectors are available for fans to be mounted to the PTA's PCB. The Sunon KDE0517PDB2-8 is a 70CFM 5V low profile fan that fit well on the PTA. The figure below shows the pinout of the fan connectors:



3 PTA Registers

In order to help the user to get started with the PTA card it comes with minimum firmware for the Altera Apex chip. Below we describe the features of this firmware.

3.1 PTA Configuration Register

This 32bit register is used to get information on the mezzanine card that is currently installed on the PTA. The read and write functions of this register are shown below:

BAR2, Offset 0x00 Read

31	30:20	19	18	17	16	15:2	1	0
CMCRESET	X	TMS	TCK	TDO	TDI	X	EEDIR	EEDATA

Bit0 – EEDATA: 1Wire bus data

This bit is used to read data from the 1-Wire EEPROM on the mezzanine card.

Bit1 – EEDIR: 1Wire data bus direction

This bit shows the current direction of the data on the 1-Wire bus. When cleared (zero), the bus is set for writing to the 1-Wire EEPROM. When set (one), the bus is set for reading.

Bits15:2 – Undefined

Bit16 – TDI

This bit monitors the current value of the JTAG serial data output pin. A read of this bit will show the data last written to it.

Bit17 – TDO

This bit connects to the JTAG serial data input pin. The bit monitors what is on the TDO pin coming from the programmable device. The TDO bit is read only.

Bit18 – TCK

This bit monitors the current value of the JTAG TCK clock pin. A read of this bit will show the data last written to it.

Bit19 – TMS

This bit monitors the current value of the JTAG TMS mode pin. A read of this bit will show the data last written to it.

Bits30:20 – Undefined

Bit31 – CMC Reset: CMC Mezzanine card reset

This bit shows the current state of the mezzanine card reset signal. When set (one), the mezzanine card is currently in a reset state.

BAR2, Offset 0x00 Write

31	30:20	19	18	17	16	15:2	1	0
CMC RESET	X	TMS	TCK	X	TDI	X	EEDIR	EEDATA

Bit0 – EEDATA: 1Wire bus data

This bit is used to write data to the 1-Wire EEPROM on the mezzanine card.

Bit1 – EEDIR: 1Wire data bus direction

This bit controls the direction of the data on the 1-Wire bus. When cleared (zero), the bus is set for writing to the 1-Wire EEPROM. When set (one), the bus is set for reading.

Bits15:2 – Undefined

Bit16 – TDI

This bit controls the state of the JTAG TDI serial data output pin. A read of this bit shows the last value written to it.

Bit17 – TDO

The TDO bit is read only, a write to this bit has no function.

Bit18 – TCK

This bit controls the state of the JTAG TCK clock output pin. A read of this bit shows the last value written to it.

Bit19 – TMS

This bit controls the state of the JTAG TMS mode output pin. A read of this bit shows the last value written to it.

Bit31 – CMC Reset: CMC Mezzanine card reset

When set (one), this bit will activate a 100ms reset to the mezzanine card. The bit will clear its self after the 100ms reset is terminated.

3.2 CMC Mezzanine Configuration/Status Register

This is a general purpose 32bit register that is used for mezzanine card configuration and mezzanine card status. The contents of this register will vary from each mezzanine card design. The mezzanine card designer will determine how this register will be used.

BAR2, Offset 0x04 Read/Write

31:0
CFG/STATUS

3.3 ZBT SSRAM Control Register

This register contains control bits for the two banks of ZBT SSRAM. The function of the control bits are listed below:

BAR2, Offset 0x08 Read/Write

31:4	3	2	1	0
X	B1CNTCLR	B1DIR	B0CNTCLR	B0DIR

Bit0 – B0DIR: Memory Bank0 Direction

This bit is used to select who has control of memory bank 0. If set (one), the mezzanine card has control of Bank0. If cleared (zero), the PTA has control of Bank0.

Bit1 – B0CNTCLR: Bank0 Address Counter Reset

This bit resets the address pointer register for Bank0. If set (one), the address counter is reset. If cleared, the counter will operate normally.

Bit2 – B1DIR: Memory Bank1 Direction

This bit is used to select who has control of memory bank 1. If set (one), the mezzanine card has control of Bank1. If cleared (zero), the PTA has control of Bank1.

Bit3 – B1CNTCLR: Bank1 Address Counter Reset

This bit resets the address pointer register for Bank1. If set (one), the address counter is reset. If cleared, the counter will operate normally.

Bits31:4 – Undefined

3.4 Bank0 Address Pointer

This register is an address pointer to Bank0 of the ZBT SRAM. The mezzanine card will use this pointer for its reads and writes from Bank0.

BAR2, Offset 0x0C Read/Write

31:0
Bank0 Address Pointer

3.5 Bank1 Address Pointer

This register is an address pointer to Bank1 of the ZBT SRAM. The mezzanine card will use this pointer for its reads and writes from Bank1.

BAR2, Offset 0x10 Read/Write

31:0
Bank1 Address Pointer

3.6 Bank0 Limit Register

This register is used as a programmable threshold that when crossed will set the B0LIMIT bit in the ZBT SSRAM Status register. The B0LIMIT bit is cleared when a zero is written to it.

BAR2, Offset 0x14 Read/Write

31:0
Bank0 Limit

3.7 Bank1 Limit Register

This register is used as a programmable threshold that when crossed will set the B1LIMIT bit in the ZBT SSRAM Status register. The B1LIMIT bit is cleared when a zero is written to it.

BAR2, Offset 0x18 Read/Write

31:0
Bank1 Limit

3.8 ZBT SSRAM Status Register

This register shows the status of both banks of memory.

BAR2, Offset 0x1C Read/Write

31:8	7	6	5	4	3	2	1	0
X	B1LIMIT	B1HFULL	B1FULL	B1EMPTY	B0LIMIT	B0HFULL	B0FULL	B0EMPTY

Bit0 – B0EMPTY: Memory Bank0 Empty

This bit is set (one) when the Bank0 address pointer is at location 0x00000000.

Bit1 – B0FULL: Memory Bank0 Full

This bit is set (one) when the Bank0 address pointer hits the last location in memory.

Bit2 – B0HFULL: Memory Bank0 Half Full

This bit is set (one) when the Bank0 address pointer crosses the half point in the memory.

Bit3 – B0LIMIT: Memory Bank0 Limit

This bit is set (one) when the programmable threshold in the Bank0 limit register has been reached.

Bit4 – B1EMPTY: Memory Bank1 Empty

This bit is set (one) when the Bank1 address pointer is at location 0x00000000.

Bit5 – B1FULL: Memory Bank1 Full

This bit is set (one) when the Bank1 address pointer hits the last location in memory.

Bit6 – B1HFULL: Memory Bank1 Half Full

This bit is set (one) when the Bank1 address pointer crosses the half point in the memory.

Bit7 – B1LIMIT: Memory Bank1 Limit

This bit is set (one) when the programmable threshold in the Bank1 limit register has been reached.

Bits31:8 – Undefined

4 Software

4.1 Drivers

We intend to use WinDriver from Jungo Ltd. to generate Windows PCI and USB drivers for Win9x, WinNT, and Win2000. They also have versions for Linux, VxWorks, and Solaris. This package generates C/C++ routines and DLL's that can be used to access the PTA from the PCI bus or a USB bus.

4.2 USB

We will be using the Keil DK51 C compiler for programming the 8051 uC in the Cypress USB controller.

4.3 JTAG

We will be porting the source code available on the JAM STAPLE web page to function with the two different JTAG chains on the PTA. See the Appendix for the JAM STAPLE web page link.

5 Power and Cooling Requirements

5.1 Power Requirements

5.1.1 PTA Power Requirements

With no mezzanine card installed, the PTA draws the following current:

- 3.3V 360ma
- 5.0V 40ma
- 12V 0ma
- -12V 0ma

5.1.2 Mezzanine Power Requirements

The total power consumption of the mezzanine card must not exceed 20 watts. This is a total of the wattage of all supplies on the PCI connector, +3.3V, +3.3Vaux, +5V, +VI/O, +12V, and -12V.

5.2 Cooling Requirements

The PTA requires no special cooling at this time. For proper cooling the PTA should be installed in a PC with the PC's case on. This will insure proper airflow inside the PC's case.

6 Appendix

6.1 Datasheet and software websites

I have listed below the links to all of the major components on the PTA. At the time of the writing of this document all links were functioning.

- Altera EP20K200 FPGA and EPC2 boot device datasheets, http://www.altera.com .
- JAM Player source code, http://www.jamisp.com .
- Cypress CY7C64613 USB chip datasheets, http://www.cypress.com .
- Dallas DS2430A 1-Wire EEPROM, http://www.dalsemi.com .
- Micron MT55L256L32F ZBT SSRAM datasheets, http://www.micron.com .
- PLX Technology PCI9030 target PCI interface datasheets, http://www.plxtech.com .
- Jungo Ltd. Windriver information, http://www.jungo.com .
- Keil DK51 8051 C compiler information, http://www.keil.com .
- IEEE P1386 Common Mezzanine Card Standard, http://www.tahoewayne.com .
- IEEE 1149.1 JTAG information, http://www.ieee.com .
- PCI Bus specification, http://www.pcisig.com .