Fermi National Accelerator Laboratory

PIXEL DETECTOR PROJECT

Programmable Mezzanine Card (PMC)

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Document Revision History

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0.0	2/26/01	B. Hall	Original
1.0	3/6/01	B. Hall	Changes per 3/2/01 review
1.1	3/12/01	B. Hall	Changed JTAG emulation pins from pins 57, 58, 60, and 61 on Jn2 to the BUSMODE pins on Jn1/Jn2.

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1 Introduction

This document describes the specifications and functionality of the Programmable Mezzanine Card (PMC). The PMC in intended work in conjunction with the PCI Test Adapter (PTA) card [1] to serve as a flexible platform for building small DAQ systems for testing detectors and subsystems. The PMC is designed around the Xilinx Virtex II FPGA which serves as an interface between the PTA card resources and the external subsystem/detector and miscellaneous inputs (see Figure 1). The Xilinx Virtex II FPGA features configurable inputs and outputs that support a wide variety of single ended and differential I/O signaling standards. TTL (5V or 3.3V), NIM and ECL interfaces are supported by level translator ICs assembled on the board. Expandability can be achieved by plugging in multiple PTA/PMC assemblies into available PCI slots in the host PC or using PCI extender crates.

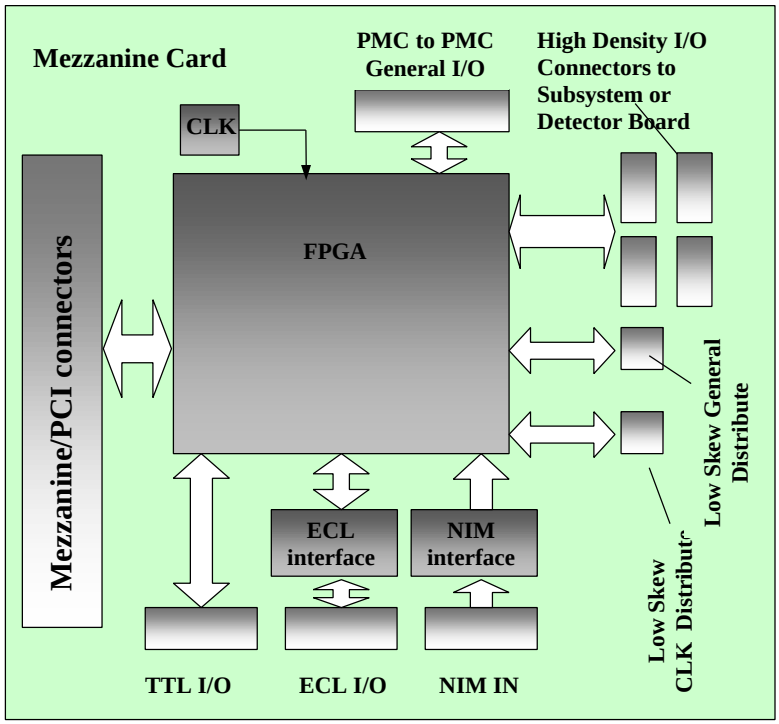

Figure 1. Functional Block Diagram of Programmable Mezzanine Card (PMC)

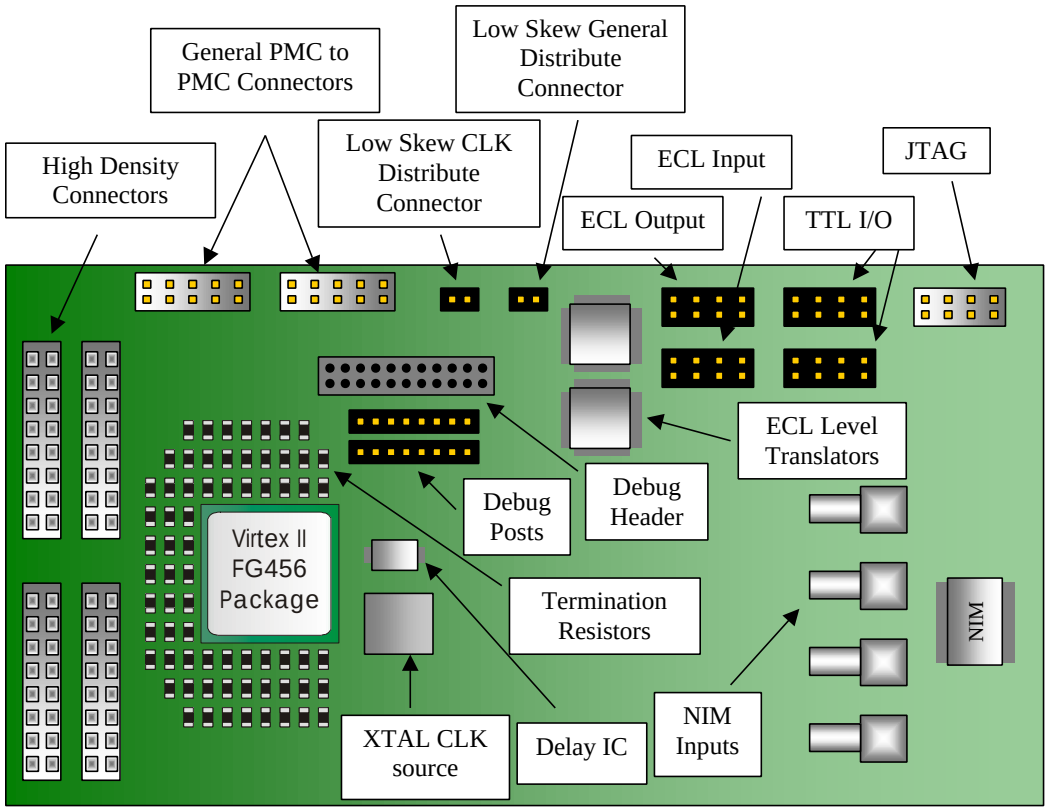

Figure 2. Diagram of key PMC components.

2 Circuitry and Connector Interfaces

This section describes some of the circuitry required in the PMC in order to satisfy its intended function. Figure 2 diagrams the key components in the PMC and a possible layout of the circuitry and connectors. The PTA Mezzanine card connector is on the bottom side of the board and is not shown in Figure 2.

2.1 PTA Card Interface

Table 1 shows the pin out description of the PTA/Mezzanine card interface connectors. This table is reproduced here from the PTA card specifications document [1]. A AMP part #AMP120527 64 position surface mount connector is used to make the physical connection.

Jn1			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
1	JN1_S0	2	-12V
3	Ground	4	JN1_S1
5	JN1_S2	6	JN1_S3
7	BUSMODE1#	8	5V
9	JN1_S4	10	JN1_S5
11	Ground	12	JN1_S6
13	CLK2	14	Ground
15	Ground	16	CLK2LK
17	CLK2FB	18	5V
19	3.3V(I/O)	20	JN1_S9
21	JN1_S10	22	JN1_S11
23	JN1_S12	24	Ground
25	Ground	26	JN1_S13
27	JN1_S14	28	JN1_S15
29	JN1_S16	30	5V
31	3.3V(I/O)	32	JN1_S17
33	JN1_S18	34	Ground
35	Ground	36	JN1_S19
37	JN1_S20	38	5V
39	Ground	40	JN1_S21
41	JN1_S22	42	JN1_S23
43	JN1_S24	44	Ground
45	3.3V(I/O)	46	JN1_S25
47	JN1_S26	48	JN1_S27
49	JN1_S28	50	5V
51	Ground	52	JN1_S29
53	JN1_S30	54	JN1_S31
55	JN1_S32	56	Ground
57	3.3V(I/O)	58	JN1_S33
59	JN1_S34	60	JN1_S35
61	JN1_S36	62	5V
63	Ground	64	EEDATA

Jn2			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
1	12V	2	JN2_S0
3	JN2_S1	4	JN2_S2
5	JN2_S3	6	Ground
7	Ground	8	JN2_S4
9	JN2_S5	10	JN2_S6
11	BUSMODE2#	12	3.3V
13	JN2_S7	14	BUSMODE3#
15	3.3V	16	BUSMODE4#
17	JN2_S8	18	Ground
19	JN2_S9	20	JN2_S10
21	Ground	22	JN2_S11
23	JN2_S12	24	3.3V
25	JN2_S13	26	JN2_S14
27	3.3V	28	JN2_S15
29	JN2_S16	30	Ground
31	JN2_S17	32	JN2_S18
33	Ground	34	JN2_S19
35	JN2_S20	36	3.3V
37	Ground	38	JN2_S21
39	JN2_S22	40	Ground
41	3.3V	42	JN2_S23
43	JN2_S24	44	Ground
45	JN2_S25	46	JN2_S26
47	Ground	48	JN2_S27
49	JN2_S28	50	3.3V
51	JN2_S29	52	JN2_S30
53	3.3V	54	JN2_S31
55	JN2_S32	56	Ground
57	JN2_S33	58	JN2_S34
59	Ground	60	JN2_S35
61	JN2_S36	62	3.3V
63	Ground	64	CLK4

= Programmable I/O = Fixed Purpose Pin = Power Pin = Ground Pin

Table 1. PTA card mezzanine connector pin assignment.

Virtex II 1000 FG456	
Available I/Os:	324
System Gates:	1M
SelectRAM bits:	720k
Digital Clock Managers (DCMs):	8

Table 2. Xilinx XC2V1000 FG456 features.

2.2 BUSMODE Connections

The four BUSMODE signals on the PTA mezzanine card connector are part of the IEEE P1386 CMC card specifications. For the PMC card, these pins will instead be used for JTAG emulation. See section 3.2 for further details.

2.3 Card Identification Number

A Dallas Semiconductor 1 wire serial memory provides each PMC a unique identification number. Use of this component is a requirement of the PTA specification. Refer to the PTA card specifications [1] and the Dallas Semiconductor web site for more information. The EEDATA pin (Pin 64) on the PTA Mezzanine card interface is reserved for connection to this device.

2.4 Virtex II FPGA

The heart of the PMC is a Xilinx Virtex II XC2V1000 FPGA in a FG456 package [2]. This device is electrically connected to all I/O connectors used to receive and transmit external signals as well as all the I/O on the PTA mezzanine card connector. The FPGA offers the user programmable flexibility in signal control as well as signaling level standards. Table 2 summarizes some of the key features of the XC2V1000 FPGA.

2.5 Clock Select and Low Skew Distribute

The main PMC FPGA clock can come from one of seven sources: Altera CLK2 from the PTA, Altera CLK4 from the PTA, local CLK from the on board XTAL, externally from a TTL input, externally from a NIM input, externally from a ECL input, or externally from the Low Skew Clock Distribution connector. Firmware in the FPGA is used to select the clock source.

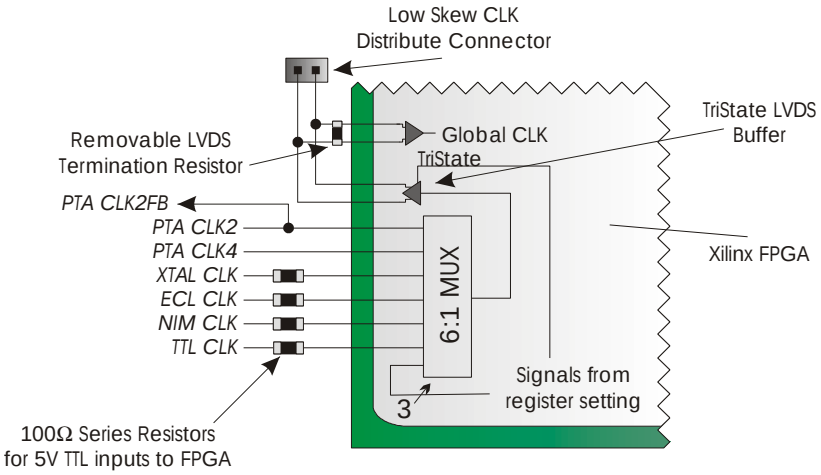

Figure 3. Clock select for low skew distribution and receiving

If a PMC is in a system with multiple PTA/PMC assemblies, one of the PMCs can be used as the master clock source for all other PTA/PMC assemblies. A CLK source is selected by a register in the FPGA (set by the user via software) and level translated to LVDS via the Xilinx Virtex II programmable I/O standards. The LVDS signal is then driven to the Low Skew Clock Distribution connector and a global clock input on the FPGA. The Low Skew Clock Distribution connector is used to distribute the LVDS version of the selected clock to other PMCs via a board to board multi drop cable.

If a PMC is to be configured to receive a CLK from the Low Skew Clock Distribution connector, a register in the receiving FPGA must tristate the LVDS output buffer shown in Figure 3.

The clock distribution scheme is low skew because the number of level translators the clock passes through before being received at each of the FPGAs' global clock input pins (on multiple PMCs) is the same. This technique will allow the clock to arrive with minimum phase shift from board to board.

2.6 General Signal Select and Low Skew Distribute

A second low skew distribution circuit similar to the low skew clock distribution circuit is on the PMC for distributing any signal from board to board with minimum skew. The general signal can come from one of five sources: Altera pin from the PTA, externally from a TTL input, externally from a NIM input, externally from a ECL input, or externally from the Low Skew General Distribution connector. Firmware in the FPGA is used to select the general signal source as shown in Figure 4.

If a PMC is to be configured to receive a general signal from the Low Skew General Distribution connector, a register in the receiving FPGA must tristate the LVDS output buffer shown in Figure 4.

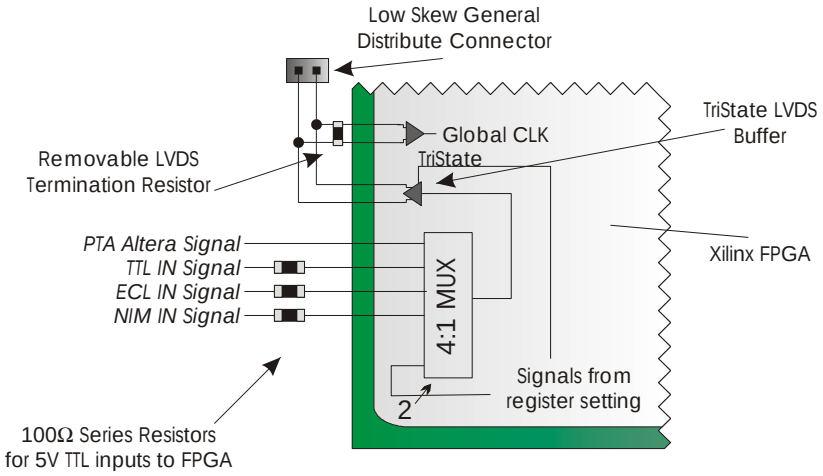

Figure 4. General signal select for low skew distribution and receiving.

The general signal distribution scheme is low skew because the number of level translators the general signal passes through before being received at each of the FPGAs' global clock input pins (on multiple PMCs) is the same. This technique will allow the general signal to arrive with minimum phase shift from board to board.

2.7 General Purpose TTL I/O

External sources can send or receive TTL signals to or from the PMC by connecting to available general purpose TTL I/O connectors. There are a total of 8 connectors available as shown in Figure 5. TTL IO1 and TTL IO2 go to the TTL CLK Select (see Figure 3) and TTL IN Signal select, respectively, (see Figure 4) as well as an FPGA I/O.

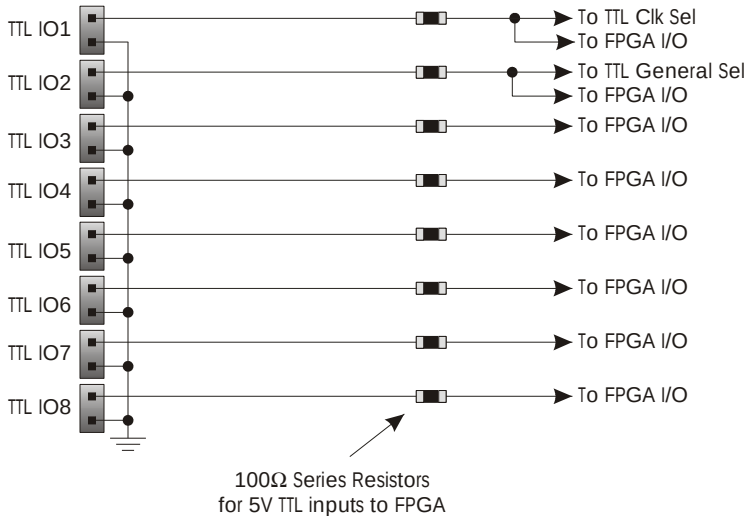

Figure 5. General purpose TTL I/O

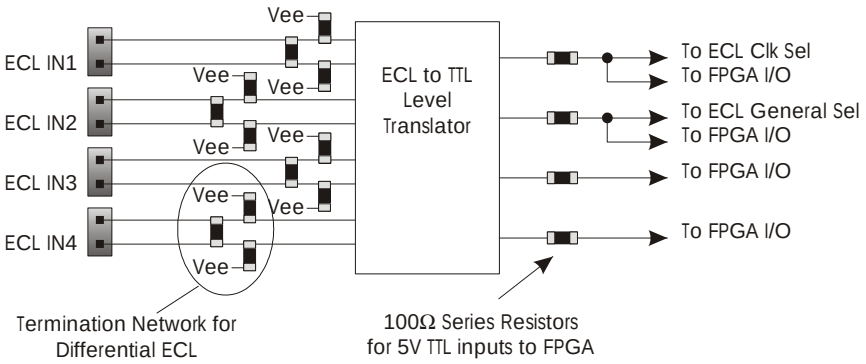

Figure 6. General purpose ECL inputs.

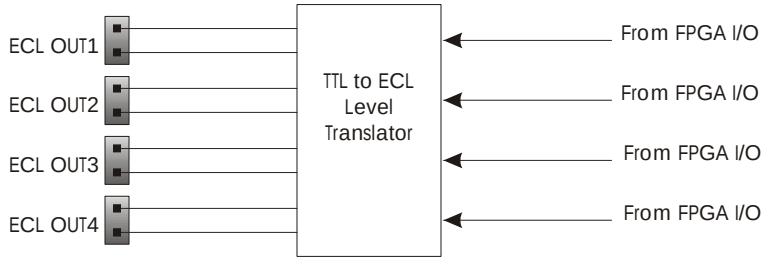

Figure 7. General purpose ECL outputs.

2.8 General Purpose ECL Inputs

Four general purpose ECL input connectors are available as shown in Figure 6. ECL IN1 and ECL IN2 go to the ECL CLK select (see Figure 3) and ECL IN Signal select (see Figure 4), respectively, as well as an FPGA I/O. The component that translates the ECL inputs to TTL levels is an On Semiconductor MC10125.

2.9 General Purpose ECL Outputs

Four general purpose ECL output connectors are available as shown in Figure 7. The four signal all come from a FPGA I/O pin. The component that translates the TTL levels from the Xilinx FPGA to ECL levels at the connectors is an On Semiconductor MC10124.

2.10 General Purpose NIM Inputs

Four general purpose NIM input connectors are available as shown in Figure 8. NIM IN1 and NIM IN2 go to the NIM CLK select (see Figure 3) and NIM IN Signal select (see Figure 4), respectively, as well as an FPGA I/O. The component that translates the NIM inputs to TTL is a MAX901.

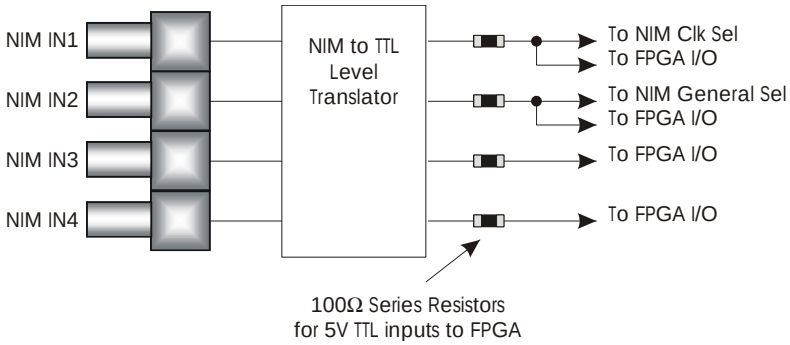

Figure 8. General purpose NIM inputs.

2.11 Delay Line

The PMC provides one 5 tap delay line for general signal delay requirements. A jumper is used to select the tap. The delay component is socketed to allow for easy replacement of delay components of differing values. The circuit used to tap the appropriate delay is shown in Figure 8. The delay component used is a Data Delay Devices series DDU83C. A few of the DDU83C devices available and their corresponding delays are shown in Table 3.

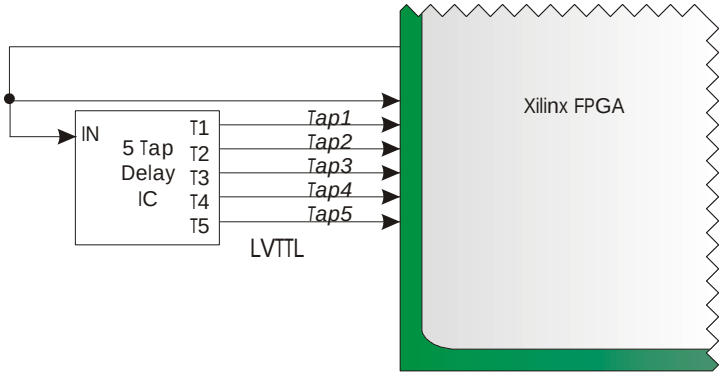

Figure 9. Delay circuit.

Part Number	Total Delay (ns)	Delay Per Tap (ns)
DDU8C3-5004	4 +/- 1.0	1.0 +/- 0.5
DDU8C3-5006	6 +/- 1.0	1.5 +/- 0.5
DDU8C3-5008	8 +/- 2.0	2.0 +/- 1.0
DDU8C3-5010	10 +/- 2.0	2.5 +/- 1.0
DDU8C3-5020	20 +/- 2.0	4.0 +/- 1.0
DDU8C3-5030	30 +/- 2.0	6.0 +/- 1.5
DDU8C3-5040	40 +/- 2.0	8.0 +/- 2.0

Table 3. Some of the available delay components and their corresponding delays.

2.12 General PMC to PMC Connector

Two 14 pin connectors are on the PMC for general board to board communication (see Figure 10). One connector is dedicated as an input connector and the other as an output connector. The signaling standard over this cable is intended to be differenial (LVDS, LVDSEXT, or LVPECL), however the user can also a single ended standard. There are 4 ground conductors and 10 signal conductors. This gives the user up to 5 differential signals or 10 single ended signals. Table 4 describes the pin out of both connectors.

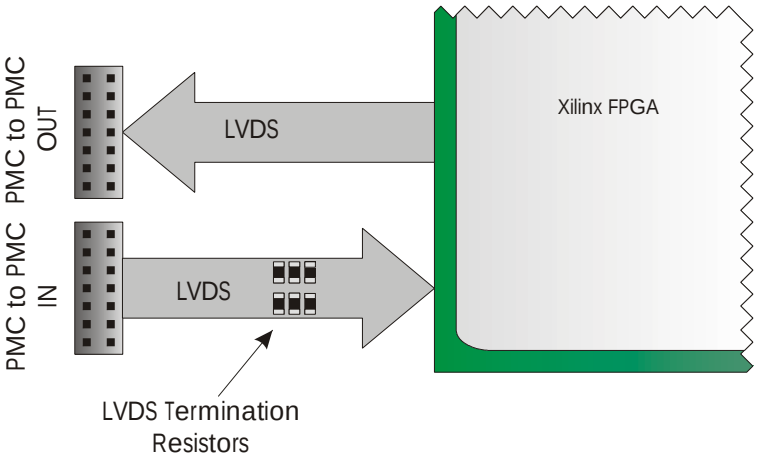

Figure 10. 14 pin PMC to PMC connectors.

Pin #	Description
1	GND
2	GND
3	FPGA I/O L*P
4	FPGA I/O L*N
5	FPGA I/O L*P
6	FPGA I/O L*N
7	FPGA I/O L*P
8	FPGA I/O L*N
9	FPGA I/O L*P
10	FPGA I/O L*N
11	FPGA I/O L*P
12	FPGA I/O L*N
13	GND
14	GND

Table 4. Pin assignment for general PMC to PMC connectors.

Available I/O Standards
LVTTL
LVCMOS (1.5V to 3.3V)
LVDS
LVDSEXT
LVPECL

Table 5. I/O standards available.

Differential I/O Standard	Output Swing (DV) w/ 100W Termination
LVDS	.350
LVDSEXT	1.2
LVPECL	.850 (Vcco = 3.3V)

Table 6. Differential I/O standards

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2.13 Prototype Area

The PMC has a small prototype area suitable for assembling a few additional components the user may need. A select number of FPGA I/O pins are connected to the prototype area consisting of through holes for mounting of components or posts.

2.14 Differential/Single Ended I/O Connectors

The PMC has four 50 pin SAMTEC FTS connectors that can be used to connect to a detector, subsystem or any other device or devices the user wishes to interface with. Of the 50 pins in each connector, 14 of them are connected to GND, 2 are connected to a PWR pad, and the remaining 34 are connected to a FPGA I/O (see Figure 11). With the four connectors this allows the user to utilize up to 136 single ended or 68 differential signals. The I/O signaling standards available in the Xilinx FPGA and the voltages associated with the differentials signaling standards are shown in Tables 5 and 6, respectively.

The user has the flexibility of independently programming each I/O pin to use any of the given I/O standards shown in Table 5. The only restriction the user has is that if differential signaling is to be used, the positive end of the signal must connect to and odd pin number on the connector and the negative end of the signal must connect to the adjacent even pin. Tables 7, 8, 9, and 10 detail the pin assignments. Note that signal names with a "_P" in them must map to an FPGA I/O pin with a Xilinx FPGA pin description name that contains "L*P". Signal names with a "_N" in them must map to an FPGA I/O pin with a FPGA pin description name that contains "L*N". See the Xilinx data book for the FG456 I/O pin description names.

A variable voltage regulator will set the Vcco of the FPGA I/O banks connecting to the SAMTEC connectors. This will allow the user to have control over the output voltage levels. Note that the LVDS and LVDSEXT differential I/Os described in Table 6 are specified to work at either Vcco = 3.3V or 2.5V.

Pins 7 and 8 on each of the connectors are routed to a global clock resource on the Xilinx FPGA. This allows the user to receive one clock signal from each of the connectors that are directly connected to the Xilinx FPGA internal global clock distribution network.
Pins 2 and 4 on each of the connectors are routed to a large pad on the PMC PCB which can be used to hand solder a power source or any other signal the user wishes to connect.

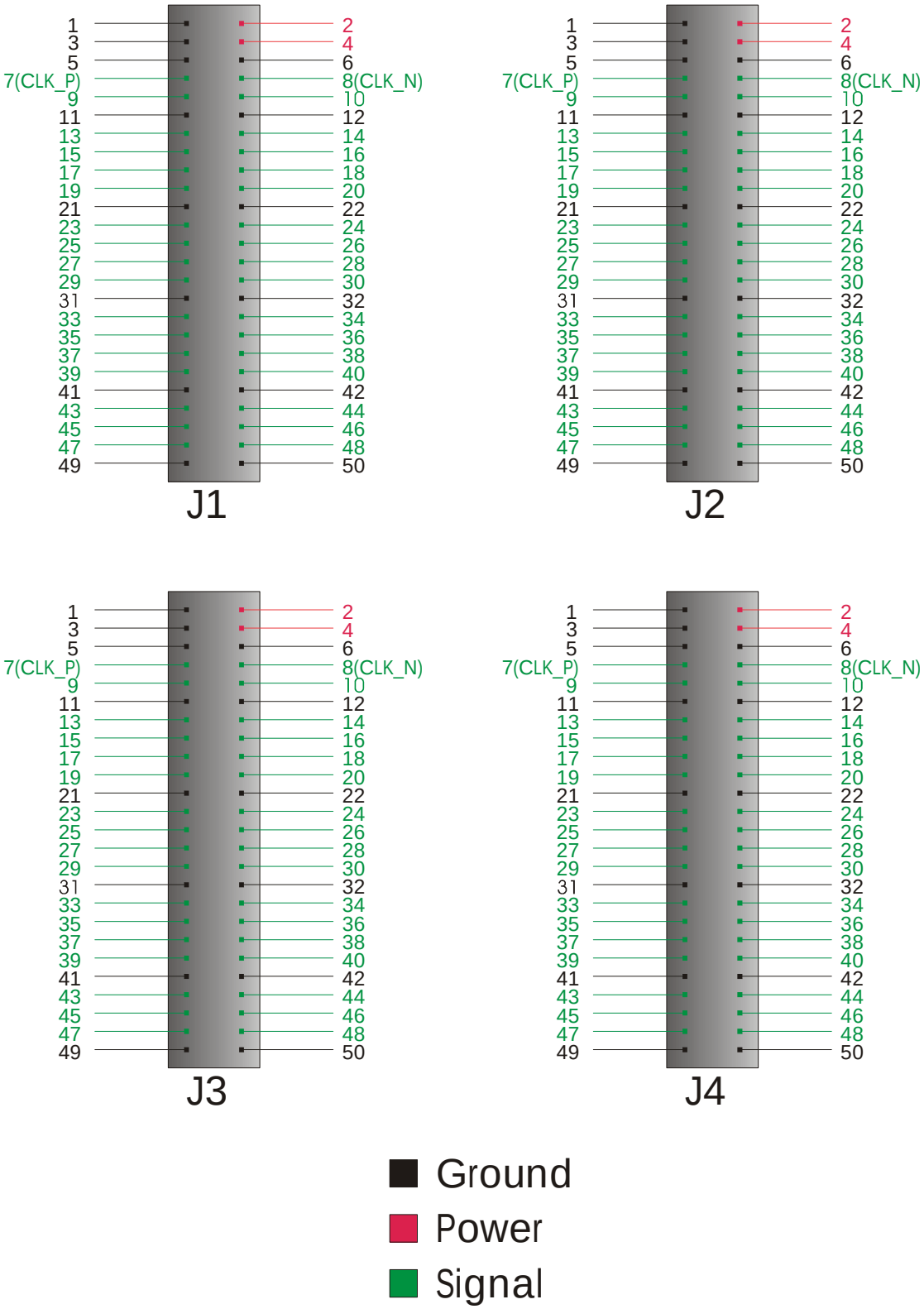

Figure 11. Pin function for SAMTEC connectors.

J1						
Pin #	**Signal Name**	**FPGA Pin**		**Pin #**	**Signal Name**	**FPGA Pin**
1	Ground	N/A		2	PWR1	N/A
3	Ground	N/A		4	PWR2	N/A
5	Ground	N/A		6	Ground	N/A
7	GPIO_A1_P_CLK	*TBD*		8	GPIO_A1_N_CLK	*TBD*
9	GPIO_A2_P	*TBD*		10	GPIO_A2_N	*TBD*
11	Ground	N/A		12	Ground	N/A
13	GPIO_A3_P	*TBD*		14	GPIO_A3_N	*TBD*
15	GPIO_A4_P	*TBD*		16	GPIO_A4_N	*TBD*
17	GPIO_A5_P	*TBD*		18	GPIO_A5_N	*TBD*
19	GPIO_A6_P	*TBD*		20	GPIO_A6_N	*TBD*
21	Ground	N/A		22	Ground	N/A
23	GPIO_A7_P	*TBD*		24	GPIO_A7_N	*TBD*
25	GPIO_A8_P	*TBD*		26	GPIO_A8_N	*TBD*
27	GPIO_A9_P	*TBD*		28	GPIO_A9_N	*TBD*
29	GPIO_A10_P	*TBD*		30	GPIO_A10_N	*TBD*
31	Ground	N/A		32	Ground	N/A
33	GPIO_A11_P	*TBD*		34	GPIO_A11_N	*TBD*
35	GPIO_A12_P	*TBD*		36	GPIO_A12_N	*TBD*
37	GPIO_A13_P	*TBD*		38	GPIO_A13_N	*TBD*
39	GPIO_A14_P	*TBD*		40	GPIO_A14_N	*TBD*
41	Ground	N/A		42	Ground	N/A
43	GPIO_A15_P	*TBD*		44	GPIO_A15_N	*TBD*
45	GPIO_A16_P	*TBD*		46	GPIO_A16_N	*TBD*
47	GPIO_A17_P	*TBD*		48	GPIO_A17_N	*TBD*
49	Ground	N/A		50	Ground	N/A

Table 7. J1 pin assignment.

J2						
Pin #	**Signal Name**	**FPGA Pin**		**Pin #**	**Signal Name**	**FPGA Pin**
1	Ground	N/A		2	PWR1	N/A
3	Ground	N/A		4	PWR2	N/A
5	Ground	N/A		6	Ground	N/A
7	GPIO_B1_P_CLK	*TBD*		8	GPIO_B1_N_CLK	*TBD*
9	GPIO_B2_P	*TBD*		10	GPIO_B2_N	*TBD*
11	Ground	N/A		12	Ground	N/A
13	GPIO_B3_P	*TBD*		14	GPIO_B3_N	*TBD*
15	GPIO_B4_P	*TBD*		16	GPIO_B4_N	*TBD*
17	GPIO_B5_P	*TBD*		18	GPIO_B5_N	*TBD*
19	GPIO_B6_P	*TBD*		20	GPIO_B6_N	*TBD*
21	Ground	N/A		22	Ground	N/A
23	GPIO_B7_P	*TBD*		24	GPIO_B7_N	*TBD*
25	GPIO_B8_P	*TBD*		26	GPIO_B8_N	*TBD*
27	GPIO_B9_P	*TBD*		28	GPIO_B9_N	*TBD*
29	GPIO_B10_P	*TBD*		30	GPIO_B10_N	*TBD*
31	Ground	N/A		32	Ground	N/A
33	GPIO_B11_P	*TBD*		34	GPIO_B11_N	*TBD*
35	GPIO_B12_P	*TBD*		36	GPIO_B12_N	*TBD*
37	GPIO_B13_P	*TBD*		38	GPIO_B13_N	*TBD*
39	GPIO_B14_P	*TBD*		40	GPIO_B14_N	*TBD*
41	Ground	N/A		42	Ground	N/A
43	GPIO_B15_P	*TBD*		44	GPIO_B15_N	*TBD*
45	GPIO_B16_P	*TBD*		46	GPIO_B16_N	*TBD*
47	GPIO_B17_P	*TBD*		48	GPIO_B17_N	*TBD*
49	Ground	N/A		50	Ground	N/A

Table 8. J2 pin assignment.

J3						
Pin #	**Signal Name**	**FPGA Pin**		**Pin #**	**Signal Name**	**FPGA Pin**
1	Ground	N/A		2	PWR1	N/A
3	Ground	N/A		4	PWR2	N/A
5	Ground	N/A		6	Ground	N/A
7	GPIO_C1_P_CLK	*TBD*		8	GPIO_C1_N_CLK	*TBD*
9	GPIO_C2_P	*TBD*		10	GPIO_C2_N	*TBD*
11	Ground	N/A		12	Ground	N/A
13	GPIO_C3_P	*TBD*		14	GPIO_C3_N	*TBD*
15	GPIO_C4_P	*TBD*		16	GPIO_C4_N	*TBD*
17	GPIO_C5_P	*TBD*		18	GPIO_C5_N	*TBD*
19	GPIO_C6_P	*TBD*		20	GPIO_C6_N	*TBD*
21	Ground	N/A		22	Ground	N/A
23	GPIO_C7_P	*TBD*		24	GPIO_C7_N	*TBD*
25	GPIO_C8_P	*TBD*		26	GPIO_C8_N	*TBD*
27	GPIO_C9_P	*TBD*		28	GPIO_C9_N	*TBD*
29	GPIO_C10_P	*TBD*		30	GPIO_C10_N	*TBD*
31	Ground	N/A		32	Ground	N/A
33	GPIO_C11_P	*TBD*		34	GPIO_C11_N	*TBD*
35	GPIO_C12_P	*TBD*		36	GPIO_C12_N	*TBD*
37	GPIO_C13_P	*TBD*		38	GPIO_C13_N	*TBD*
39	GPIO_C14_P	*TBD*		40	GPIO_C14_N	*TBD*
41	Ground	N/A		42	Ground	N/A
43	GPIO_C15_P	*TBD*		44	GPIO_C15_N	*TBD*
45	GPIO_C16_P	*TBD*		46	GPIO_C16_N	*TBD*
47	GPIO_C17_P	*TBD*		48	GPIO_C17_N	*TBD*
49	Ground	N/A		50	Ground	N/A

Table 9. J3 pin assignment.

J4						
Pin #	**Signal Name**	**FPGA Pin**		**Pin #**	**Signal Name**	**FPGA Pin**
1	Ground	N/A		2	PWR1	N/A
3	Ground	N/A		4	PWR2	N/A
5	Ground	N/A		6	Ground	N/A
7	GPIO_D1_P_CLK	*TBD*		8	GPIO_D1_N_CLK	*TBD*
9	GPIO_D2_P	*TBD*		10	GPIO_D2_N	*TBD*
11	Ground	N/A		12	Ground	N/A
13	GPIO_D3_P	*TBD*		14	GPIO_D3_N	*TBD*
15	GPIO_D4_P	*TBD*		16	GPIO_D4_N	*TBD*
17	GPIO_D5_P	*TBD*		18	GPIO_D5_N	*TBD*
19	GPIO_D6_P	*TBD*		20	GPIO_D6_N	*TBD*
21	Ground	N/A		22	Ground	N/A
23	GPIO_D7_P	*TBD*		24	GPIO_D7_N	*TBD*
25	GPIO_D8_P	*TBD*		26	GPIO_D8_N	*TBD*
27	GPIO_D9_P	*TBD*		28	GPIO_D9_N	*TBD*
29	GPIO_D10_P	*TBD*		30	GPIO_D10_N	*TBD*
31	Ground	N/A		32	Ground	N/A
33	GPIO_D11_P	*TBD*		34	GPIO_D11_N	*TBD*
35	GPIO_D12_P	*TBD*		36	GPIO_D12_N	*TBD*
37	GPIO_D13_P	*TBD*		38	GPIO_D13_N	*TBD*
39	GPIO_D14_P	*TBD*		40	GPIO_D14_N	*TBD*
41	Ground	N/A		42	Ground	N/A
43	GPIO_D15_P	*TBD*		44	GPIO_D15_N	*TBD*
45	GPIO_D16_P	*TBD*		46	GPIO_D16_N	*TBD*
47	GPIO_D17_P	*TBD*		48	GPIO_D17_N	*TBD*
49	Ground	N/A		50	Ground	N/A

Table 10. J4 pin assignment.

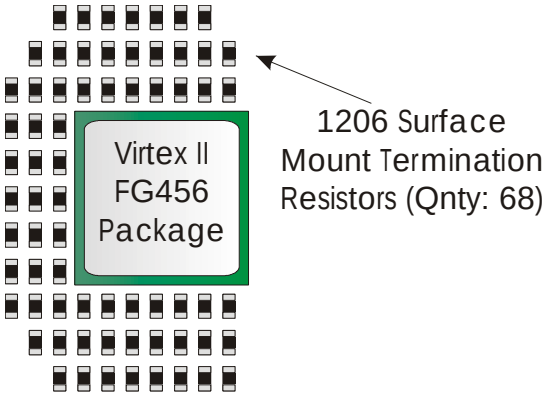

Figure 12. Location of termination resistors.

2.15 Termination Resistors for SAMTEC Connector Signals.

The user can configure the PMC to either receive or transmit differential, signal ended, or a combination of both, signals on the SAMTEC connectors. Because a mix of differential I/O and single ended I/O will be used, pads for individual 1206 series termination resistors are available for the user to install on any signal that is configured as a differential input (see Figure 12). There is a single pad set for each of possible differentials pair (68 total). An installed resistor offers a standard termination across the two differential inputs.

Silkscreen on the PCB allows for easy identification of which termination resistor applies which connector signal.

2.16 Indicator LEDs

LEDs on the PMC should be present to indicate the status of each of the required voltage levels. In addition, a number of surface mount LEDs of varying color should be connected to FPGA I/O pins for user defined control.

2.17 Reset Button

As single reset button will provide a power on reset.

2.18 Debug Header

A single 38 position connector will be used for connecting two HP logic analyzer pods for user debug. The 38 position connector is a AMP part # AMP2-767004-2. One pod (16 signals) should connect directly to FPGA I/O pins while the remaining 16 signals for the other pod should connect to posts on the PMC for user defined connections.

Supply	Value
5V TTL Level Tranlators	5V
ECL Level Translators	-5.2V
FPGA Vccaux	3.3V
FPGA Vcco Fixed Banks	3.3V
FPGA Variable Vcco Banks	1.5V - 3.3V
FPGA Vccint	1.5V

Table 11. Supply voltages required.

3 Power, Configuration, and Mechanical

3.1 Power and Voltage Regulators

The PTA card can provide full power to the PMC via the PTA Mezzanine card connector. Power comes from the PC power supply (or PCI extender crate supply). The PMC can also be powered externally for bench top testing and debug. Some of the voltages are available from the PTA Mezzanine card connector. However, some are not and they need to be generated by voltage regulators assembled on the Mezzanine card. Table 11 lists the voltages required in the PMC.

3.2 Xilinx Part Configuration

The Xilinx FPGA is configured via an on board EEPROM containing the configuration bit stream. The JTAG connector shown in Figure 13 is connected to the PTA card Altera I/O pins as described in Table 12. The configuration bit stream can be changed in system either with an external JTAG connection or through the PTA card JTAG emulation.

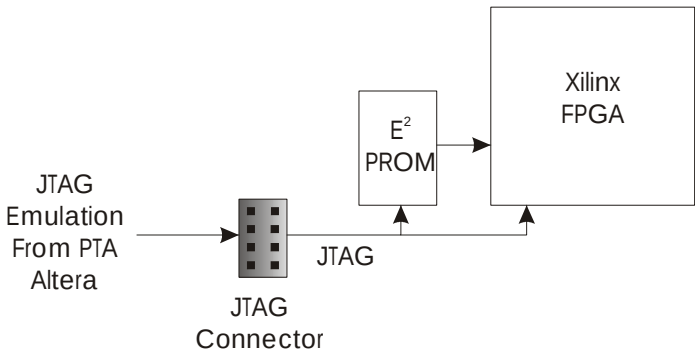

Figure 13. FPGA configuration.

PTA/Mezzanine Card Connector	JTAG Emulation
Jn1 pin 7 (BUSMODE1#)	TDI
Jn2 pin 11 (BUSMODE2#)	TCK
Jn2 pin 14 (BUSMODE3#)	TMS
Jn2 pin 16 (BUSMODE4#)	TDO

Table 12. Pin assignment for PTA JTAG emulation

3.3 5V Tolerant I/Os on Xilinx FPGA

Inputs on the Xilinx Virtex II are not inherently 5V tolerant. However 5V TTL signals from the level translators can drive LVTTL inputs on the FPGA if a 100Ω series resistor is used to prevent the FPGA I/O protection diodes from sinking too much current. Refer to Xilinx Tech Tip document VTT002 for further details [3]. The user must avoid driving 5V inputs directly to the SAMTEC connectors.

3.4 Mounting Holes

The PMC must have mounting holes for proper mezzanine mechanical support. Mounting holes are part of the PTA card mechanical specifications.

4 Expandability

Systems build around PTA/PMC assemblies can be expanded by using multiple PTA/PMC assemblies and available PCI slots on the host PC or PCI bus extenders. The PMC clock and general signal distribution techniques as well as the general purpose board to board connector can be used to transfer data and signals from board to board.

Figure 15 shows an example of a test DAQ system for a beam test built around three PTA/PMC assemblies. This system is shown controlling and reading six pixel modules (two modules for each assembly). A trigger arrives on the "master" PTA/PMC assembly and is distributed to the other PTA/PMC assemblies using the Low Skew General Distribute circuitry and a multidrop cable. A second multidrop cable is used to distribute a master clock signal using the Low Skew CLK Distribute circuitry and connectors to keep all three assemblies synchronized. A PCI interface interconnects the bus extender to a remote PC for configuration and data logging.

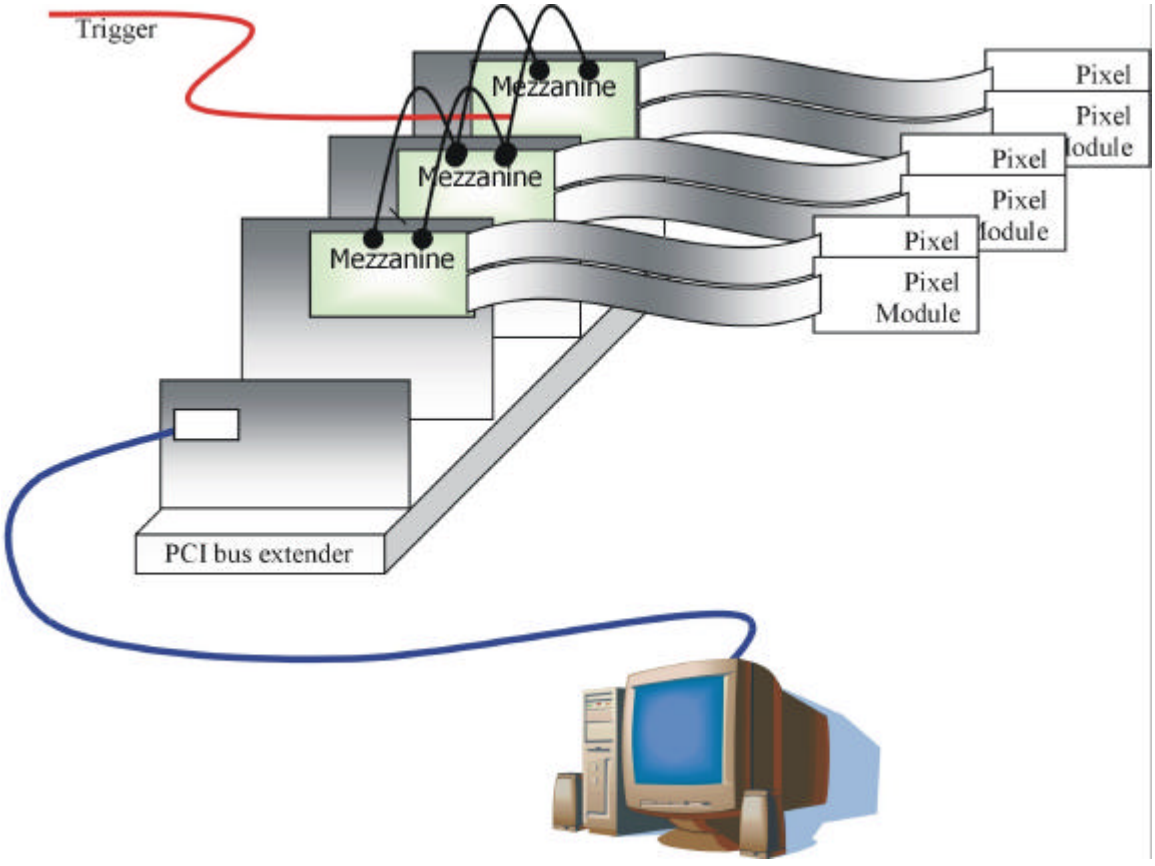

Figure 14. PTA based test stand.

5 References

[1] Deuerling, G, Treptow, K., “PCI Test Adapter Card”. Fermilab internal document. August 11, 2000.

[2] Xilinx, Inc. "Virtex-II Platform FPGA Handbook". Document DS031-1. January 25, 2001. Found at: http://www.xilinx.com/partinfo/databook.htm

[3] Xilinx, Inc. "5V Tolerant I/Os". Document VTT002. February 7, 2001. Found at: http://www.xilinx.com/products/virtex/techtopic/vtt002.pdf