FSSR2

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Introduction

The FSSR2 is the second release of the Fermilab Silicon Strip Readout Chip. The first release, simply called the FSSR, was a prototype version with many different analog front-end configurations to allow the various users to experiment with and ultimately chose the best front end for the final chip. The FSSR2 has been designed for the silicon strip detector of the BTeV experiment and includes a 3-bit FADC on every channel. The chip services 128 strips and provides address (12 bits), time (8 bits) and magnitude (3 bits) information for all hits. The data is serialized onto 1, 2, 4, or 6 output lines in a 24-bit output word (23 data bits plus 1 sync bit). The various bias lines required by the analog front end are all programmable through a slow, serial programming interface, though many of those biases can be overridden via external pads (also used for decoupling).

The FSSR2's readout architecture is a modified version of the FPIX architecture, which was developed for BTeV's pixel detector system and is also being used in the FPIX3 chip. The FSSR analog front-end was designed in cooperation with INFN in Italy. General descriptions of the FSSR analog front end and the readout architecture are beyond the scope of this paper but can be found in reference [1]. Herein only the pad frame and such information as will be needed to connect an FSSR to its board will be discussed.

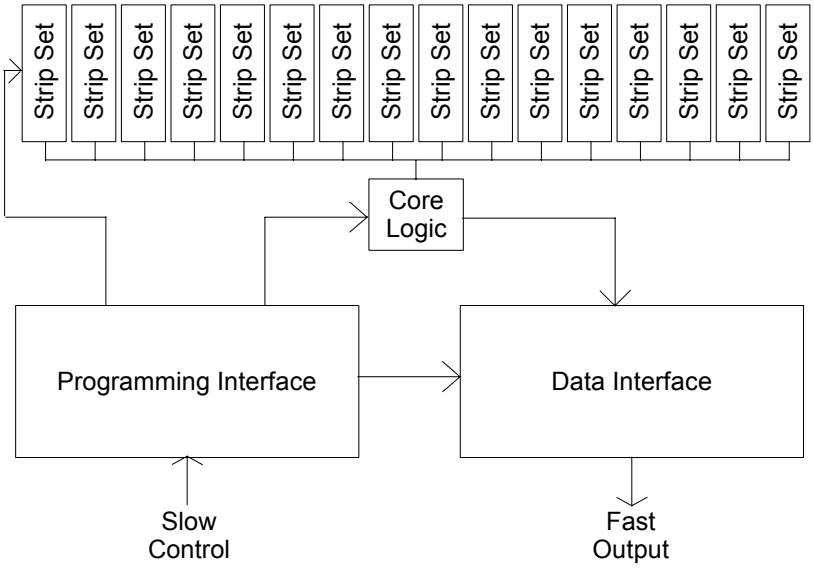


Figure 0: A block diagram of the FSSR2 Design

Block Diagram

Figure 1 shows a highly abstracted block diagram of the FSSR2 chip. In order for the readout architecture to handle the strip occupancy appropriately, the 128 strips are divided into 16 sets of 8 strips each. These "strip sets" are shown in Figure 2.

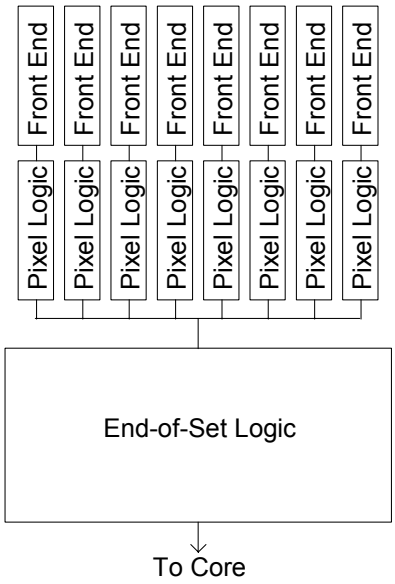
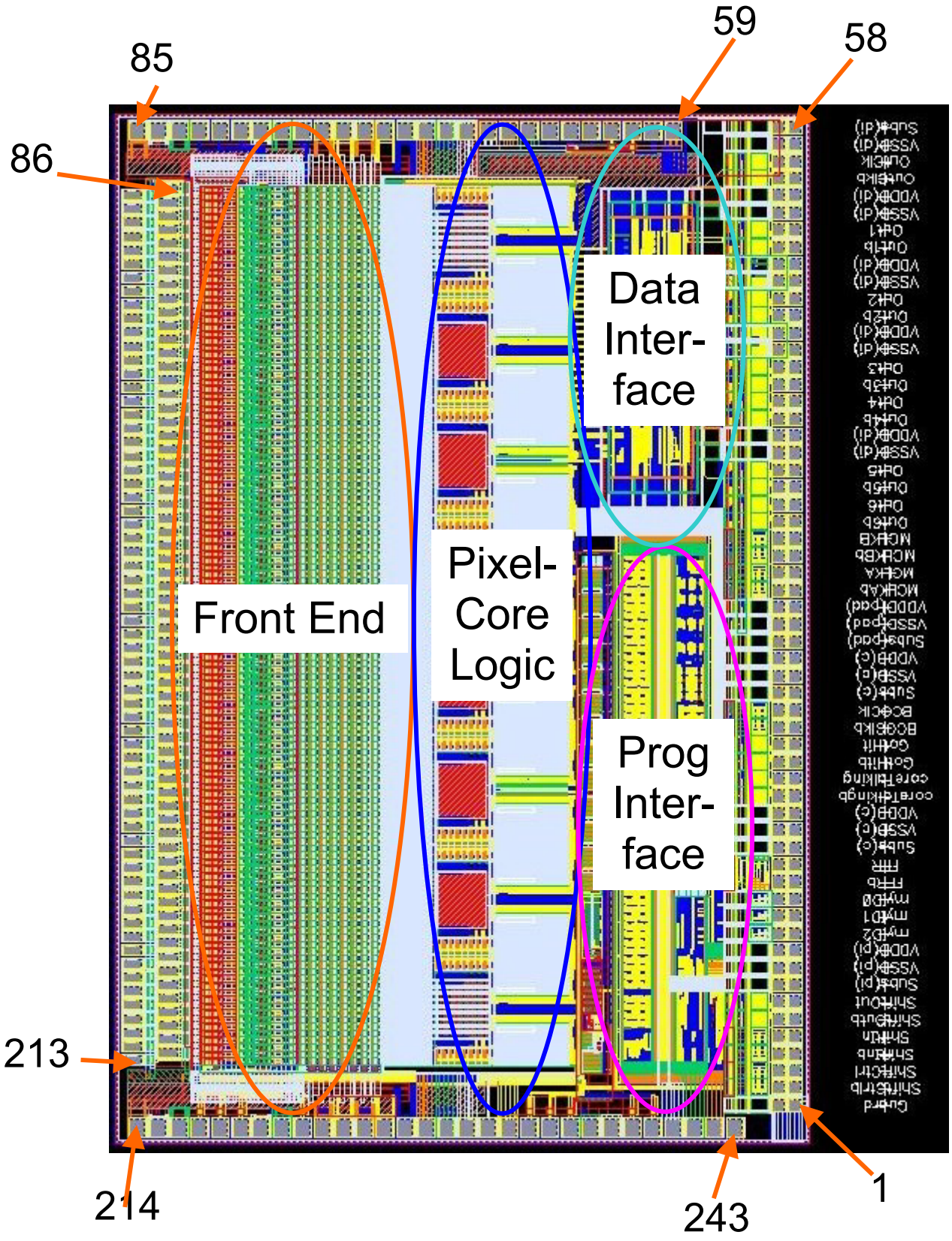


Figure 2: A block diagram of the Strip Set

A serialized slow control adjusts digital registers in the Programming interface. In turn, these digital registers directly control activity in the Data Interface (e.g. the number of active lines) and Control Logic (e.g. Send Data). Furthermore, via digital to analog converters, these digital registers in the Programming Interface control biases in the strip sets.

The data interface is given an external master clock (MClkA and MClkB) that sets the data output rate. Given the frequency of this master clock and the number of active lines requested by the user through the Programming Interface, the Data Interface generates a purely internal Read Clock used by the Core to output its data to the data interface. There is no FIFO in the data interface, and this scaling of the Read Clock ensures that data arrives at the data interface no faster than the data interface can output it.


85
59
58
86
Front End
Pixel-
Core
Logic
Data
Inter-
face
Prog
Inter-
face
213
214
243
1

Pads

Bottom – from left to right (see Figure 3)

No.	Name	Description	Y-position (mm)	X-position (mm)
1	Guard	Power - 0 volts	0.10382	0.2829
2	ShiftCtrlb	LVDS Input; when active (high), slow control is issuing command to programming interface	0.10382	0.4079
3	ShiftCtrl		0.10382	0.5329
4	ShiftInb	LVDS Input; slow control commands and data are input to the chip here	0.10382	0.6579
5	ShiftIn		0.10382	0.7829
6	ShiftOutb	Tri-statable LVDS output; when the programming interface outputs read requests, they come out here.	0.10382	0.9079
7	ShiftOut		0.10382	1.0329
8	Substrate (PI)	Power - 0 volts	0.10382	1.1579
9	VSSD (PI)	Power - 0 volts	0.10382	1.2829
10	VDDD (PI)	Power - 2.5 volts	0.10382	1.4079
11	MyID2	CMOS input (0 or 2.5 volts) This is the unique address of the chip. Esp. for the programming interface. NOTE: the chip id is 5 bits. Actual address is: (1 0 (MyID2) (MyID1) (MyID0))	0.10382	1.5329
12	MyID1		0.10382	1.6579
13	MyID0		0.10382	1.7829
14	MasterResetb	LVDS Input; Asynchronous system reset. Resets EVERYTHING in the chip including programming and hits.	0.10382	1.9079
15	MasterReset		0.10382	2.0329
16	Substrate (Core)	Power - 0 volts	0.10382	2.1579
17	VSSD (Core)	Power - 0 volts	0.10382	2.2829
18	VDDD (Core)	Power - 2.5 volts	0.10382	2.4079
19	coreTalkingb	LVDS output; diagnostic; Active when the core is driving data to the data Interface.	0.10382	2.5329
20	coreTalking		0.10382	2.6579
21	GotHitb	LVDS output; diagnostic; asynchronous indication that some strip has been hit	0.10382	2.7829
22	GotHit		0.10382	2.9079
23	BCOclkb	LVDS input; beam crossover clock; assumed to be 132ns	0.10382	3.0329
24	BCOclk		0.10382	3.1579
25	Substrate (Core)	Power - 0 volts	0.10382	3.2829
26	VSSD (Core)	Power - 0 volts	0.10382	3.4079
27	VDDD (Core)	Power - 2.5 volts	0.10382	3.5329
28	Substrate (Pads)	Power - 0 volts	0.10382	3.6579
29	VSSD (Pads)	Power - 0 volts	0.10382	3.7829
30	VDDD (Pads)	Power - 2.5 volts	0.10382	3.9079
31	MClkAb	LVDS input; output clock; 90 degrees out of phase with MClkB; assumed to be 70 MHz	0.10382	4.0329
32	MClkA		0.10382	4.1579
33	MClkBb	LVDS input; output clock; 90 degrees out of phase with MClkA; assumed to be 70 MHz	0.10382	4.2829
34	MClkB		0.10382	4.4079
35	Out6b	LVDS Output; 140 Mbit/sec chip output; active when ActLines set to 6	0.10382	4.5329
36	Out6		0.10382	4.6579
37	Out5b	LVDS Output; 140 Mbit/sec chip output; active when ActLines set to 6	0.10382	4.7829
38	Out5		0.10382	4.9079
39	VSSD (Pads)	Power - 0 volts	0.10382	5.0329
40	VDDD (Pads)	Power - 2.5 volts	0.10382	5.1579
41	Out4b	LVDS Output; 140 Mbit/sec chip output; active when ActLines set to 6 or 4	0.10382	5.2829
42	Out4		0.10382	5.4079
43	Out3b	LVDS Output; 140 Mbit/sec chip output; active when ActLines set to 6 or 4	0.10382	5.5329
44	Out3		0.10382	5.6579
45	VSSD (Pads)	Power - 0 volts	0.10382	5.7829
46	VDDD (Pads)	Power - 2.5 volts	0.10382	5.9079
47	Out2b	LVDS Output; 140 Mbit/sec chip output; active when	0.10382	6.0329

48	Out2	ActLines set to 6 or 4 or 2	0.10382	6.1579
49	VSSD (Pads)	Power - 0 volts	0.10382	6.2829
50	VDDD (Pads)	Power - 2.5 volts	0.10382	6.4079
51	Out1b	LVDS Output; 140 Mbit/sec chip output; always active	0.10382	6.5329
52	Out1		0.10382	6.6579
53	VSSD (Pads)	Power - 0 volts	0.10382	6.7829
54	VDDD (Pads)	Power - 2.5 volts	0.10382	6.9079
55	OutClkb	LVDS Output; Latch clock for the chip output; data is new and stable whenever outclk changes state.	0.10382	7.0329
56	OutClk		0.10382	7.1579
57	VSSD (Pads)	Power - 0 volts	0.10382	7.2829
58	Substrate (Pads)	Power - 0 volts	0.10382	7.4079

Right Side – from bottom to top (see Figure 3)

No.	Name	Description	Y-position (mm)	X-position (mm)
59	vssa	Power - 0 volts	0.98983	7.3821
60	TestBufBias	Test Structure – leave floating	1.13983	7.3821
61	InBufTest1	Test Structure – leave floating	1.28983	7.3821
62	InBufTest2	Test Structure – leave floating	1.43983	7.3821
63	OutBufTest3	Test Structure – leave floating	1.58983	7.3821
64	OutBufTest2	Test Structure – leave floating	1.73983	7.3821
65	OutBufTest1	Test Structure – leave floating	1.88983	7.3821
66	VDDA (test)	Test Structure – leave floating	2.03983	7.3821
67	Substrate (test)	Test Structure – leave floating	2.18983	7.3821
68	GNDA (test)	Test Structure – leave floating	2.33983	7.3821
69	Substrate (Core)	Power - 0 volts	2.48983	7.3821
70	VDDD (Core)	Power - 2.5 volts	2.63983	7.3821
71	VSSD (Core)	Power - 0 volts	2.78983	7.3821
72	VSSA	Power - 0 volts	2.93983	7.3821
73	VDD	Power - 2.5 volts	3.08983	7.3821
74	GND	Power - 0 volts	3.23983	7.3821
75	VDD	Power - 2.5 volts	3.38983	7.3821
76	GND	Power - 0 volts	3.53983	7.3821
77	DiscriBufOut	Diagnostic -Buffered output from discriminator	3.68983	7.3821
78	VDDA	Power - 2.5 volts	3.83983	7.3821
79	GNDA	Power - 0 volts	3.98983	7.3821
80	BlrBufOut	Diagnostic -Buffered output from baseline restorer	4.13983	7.3821
81	ShpBufOut	Diagnostic -Buffered output from Shaper	4.28983	7.3821
82	PrmpBufOut	Diagnostic -Buffered output from Preamp	4.43983	7.3821
83	VDDA	Power - 2.5 volts	4.58983	7.3821
84	GNDA	Power - 0 volts	4.73983	7.3821
85	VSSA	Power - 0 volts	4.88983	7.3821

Top – from right to left (see Figure 3)

No.	Name	Description	Y-position (mm)	X-position (mm)
86	In 128	Silicon Strip Detector Input	4.66988	6.9601
87	In 127	Silicon Strip Detector Input	4.92446	6.9101
88	In 126	Silicon Strip Detector Input	4.66988	6.8601
89	In 125	Silicon Strip Detector Input	4.92446	6.8101

90	In 124	Silicon Strip Detector Input	4.66988	6.7601
91	In 123	Silicon Strip Detector Input	4.92446	6.7101
92	In 122	Silicon Strip Detector Input	4.66988	6.6601
93	In 121	Silicon Strip Detector Input	4.92446	6.6101
94	In 120	Silicon Strip Detector Input	4.66988	6.5601
95	In 119	Silicon Strip Detector Input	4.92446	6.5101
96	In 118	Silicon Strip Detector Input	4.66988	6.4601
97	In 117	Silicon Strip Detector Input	4.92446	6.4101
98	In 116	Silicon Strip Detector Input	4.66988	6.3601
99	In 115	Silicon Strip Detector Input	4.92446	6.3101
100	In 114	Silicon Strip Detector Input	4.66988	6.2601
101	In 113	Silicon Strip Detector Input	4.92446	6.2101
102	In 112	Silicon Strip Detector Input	4.66988	6.1601
103	In 111	Silicon Strip Detector Input	4.92446	6.1101
104	In 110	Silicon Strip Detector Input	4.66988	6.0601
105	In 109	Silicon Strip Detector Input	4.92446	6.0101
106	In 108	Silicon Strip Detector Input	4.66988	5.9601
107	In 107	Silicon Strip Detector Input	4.92446	5.9101
108	In 106	Silicon Strip Detector Input	4.66988	5.8601
109	In 105	Silicon Strip Detector Input	4.92446	5.8101
110	In 104	Silicon Strip Detector Input	4.66988	5.7601
111	In 103	Silicon Strip Detector Input	4.92446	5.7101
112	In 102	Silicon Strip Detector Input	4.66988	5.6601
113	In 101	Silicon Strip Detector Input	4.92446	5.6101
114	In 100	Silicon Strip Detector Input	4.66988	5.5601
115	In 99	Silicon Strip Detector Input	4.92446	5.5101
116	In 98	Silicon Strip Detector Input	4.66988	5.4601
117	In 97	Silicon Strip Detector Input	4.92446	5.4101
118	In 96	Silicon Strip Detector Input	4.66988	5.3601
119	In 95	Silicon Strip Detector Input	4.92446	5.3101
120	In 94	Silicon Strip Detector Input	4.66988	5.2601
121	In 93	Silicon Strip Detector Input	4.92446	5.2101
122	In 92	Silicon Strip Detector Input	4.66988	5.1601
123	In 91	Silicon Strip Detector Input	4.92446	5.1101
124	In 90	Silicon Strip Detector Input	4.66988	5.0601
125	In 89	Silicon Strip Detector Input	4.92446	5.0101
126	In 88	Silicon Strip Detector Input	4.66988	4.9601
127	In 87	Silicon Strip Detector Input	4.92446	4.9101
128	In 86	Silicon Strip Detector Input	4.66988	4.8601
129	In 85	Silicon Strip Detector Input	4.92446	4.8101
130	In 84	Silicon Strip Detector Input	4.66988	4.7601
131	In 83	Silicon Strip Detector Input	4.92446	4.7101
132	In 82	Silicon Strip Detector Input	4.66988	4.6601
133	In 81	Silicon Strip Detector Input	4.92446	4.6101
134	In 80	Silicon Strip Detector Input	4.66988	4.5601
135	In 79	Silicon Strip Detector Input	4.92446	4.5101
136	In 78	Silicon Strip Detector Input	4.66988	4.4601
137	In 77	Silicon Strip Detector Input	4.92446	4.4101
138	In 76	Silicon Strip Detector Input	4.66988	4.3601
139	In 75	Silicon Strip Detector Input	4.92446	4.3101
140	In 74	Silicon Strip Detector Input	4.66988	4.2601
141	In 73	Silicon Strip Detector Input	4.92446	4.2101
142	In 72	Silicon Strip Detector Input	4.66988	4.1601

143	In 71	Silicon Strip Detector Input	4.92446	4.1101
144	In 70	Silicon Strip Detector Input	4.66988	4.0601
145	In 69	Silicon Strip Detector Input	4.92446	4.0101
146	In 68	Silicon Strip Detector Input	4.66988	3.9601
147	In 67	Silicon Strip Detector Input	4.92446	3.9101
148	In 66	Silicon Strip Detector Input	4.66988	3.8601
149	In 65	Silicon Strip Detector Input	4.92446	3.8101
150	In 64	Silicon Strip Detector Input	4.66988	3.7601
151	In 63	Silicon Strip Detector Input	4.92446	3.7101
152	In 62	Silicon Strip Detector Input	4.66988	3.6601
153	In 61	Silicon Strip Detector Input	4.92446	3.6101
154	In 60	Silicon Strip Detector Input	4.66988	3.5601
155	In 59	Silicon Strip Detector Input	4.92446	3.5101
156	In 58	Silicon Strip Detector Input	4.66988	3.4601
157	In 57	Silicon Strip Detector Input	4.92446	3.4101
158	In 56	Silicon Strip Detector Input	4.66988	3.3601
159	In 55	Silicon Strip Detector Input	4.92446	3.3101
160	In 54	Silicon Strip Detector Input	4.66988	3.2601
161	In 53	Silicon Strip Detector Input	4.92446	3.2101
162	In 52	Silicon Strip Detector Input	4.66988	3.1601
163	In 51	Silicon Strip Detector Input	4.92446	3.1101
164	In 50	Silicon Strip Detector Input	4.66988	3.0601
165	In 49	Silicon Strip Detector Input	4.92446	3.0101
166	In 48	Silicon Strip Detector Input	4.66988	2.9601
167	In 47	Silicon Strip Detector Input	4.92446	2.9101
168	In 46	Silicon Strip Detector Input	4.66988	2.8601
169	In 45	Silicon Strip Detector Input	4.92446	2.8101
170	In 44	Silicon Strip Detector Input	4.66988	2.7601
171	In 43	Silicon Strip Detector Input	4.92446	2.7101
172	In 42	Silicon Strip Detector Input	4.66988	2.6601
173	In 41	Silicon Strip Detector Input	4.92446	2.6101
174	In 40	Silicon Strip Detector Input	4.66988	2.5601
175	In 39	Silicon Strip Detector Input	4.92446	2.5101
176	In 38	Silicon Strip Detector Input	4.66988	2.4601
177	In 37	Silicon Strip Detector Input	4.92446	2.4101
178	In 36	Silicon Strip Detector Input	4.66988	2.3601
179	In 35	Silicon Strip Detector Input	4.92446	2.3101
180	In 34	Silicon Strip Detector Input	4.66988	2.2601
181	In 33	Silicon Strip Detector Input	4.92446	2.2101
182	In 32	Silicon Strip Detector Input	4.66988	2.1601
183	In 31	Silicon Strip Detector Input	4.92446	2.1101
184	In 30	Silicon Strip Detector Input	4.66988	2.0601
185	In 29	Silicon Strip Detector Input	4.92446	2.0101
186	In 28	Silicon Strip Detector Input	4.66988	1.9601
187	In 27	Silicon Strip Detector Input	4.92446	1.9101
188	In 26	Silicon Strip Detector Input	4.66988	1.8601
189	In 25	Silicon Strip Detector Input	4.92446	1.8101
190	In 24	Silicon Strip Detector Input	4.66988	1.7601
191	In 23	Silicon Strip Detector Input	4.92446	1.7101
192	In 22	Silicon Strip Detector Input	4.66988	1.6601
193	In 21	Silicon Strip Detector Input	4.92446	1.6101
194	In 20	Silicon Strip Detector Input	4.66988	1.5601
195	In 19	Silicon Strip Detector Input	4.92446	1.5101

196	In 18	Silicon Strip Detector Input	4.66988	1.4601
197	In 17	Silicon Strip Detector Input	4.92446	1.4101
198	In 16	Silicon Strip Detector Input	4.66988	1.3601
199	In 15	Silicon Strip Detector Input	4.92446	1.3101
200	In 14	Silicon Strip Detector Input	4.66988	1.2601
201	In 13	Silicon Strip Detector Input	4.92446	1.2101
202	In 12	Silicon Strip Detector Input	4.66988	1.1601
203	In 11	Silicon Strip Detector Input	4.92446	1.1101
204	In 10	Silicon Strip Detector Input	4.66988	1.0601
205	In 9	Silicon Strip Detector Input	4.92446	1.0101
206	In 8	Silicon Strip Detector Input	4.66988	0.9601
207	In 7	Silicon Strip Detector Input	4.92446	0.9101
208	In 6	Silicon Strip Detector Input	4.66988	0.8601
209	In 5	Silicon Strip Detector Input	4.92446	0.8101
210	In 4	Silicon Strip Detector Input	4.66988	0.7601
211	In 3	Silicon Strip Detector Input	4.92446	0.7101
212	In 2	Silicon Strip Detector Input	4.66988	0.6601
213	In 1	Silicon Strip Detector Input	4.92446	0.6101

Left Side – from top to bottom (see Figure 3)

No.	Name	Description	Y-position (mm)	X-position (mm)
214	VSSA	Power - 0 volts	4.88983	0.117
215	GNDA	Power - 0 volts	4.73983	0.117
216	VDDA	Power - 2.5 volts	4.58983	0.117
217	IntVbn1	Programmable Voltage; Decouple	4.43983	0.117
218	ShpVbp2	Programmable Voltage; Decouple	4.28983	0.117
219	ShpVbp1	Programmable Voltage; Decouple	4.13983	0.117
220	GNDA	Power - 0 volts	3.98983	0.117
221	VDDA	Power - 2.5 volts	3.83983	0.117
222	BlrVbp1	Programmable Voltage; Decouple	3.68983	0.117
223	GND	Power - 0 volts	3.53983	0.117
224	VDD	Power - 2.5 volts	3.38983	0.117
225	GND	Power - 0 volts	3.23983	0.117
226	VDD	Power - 2.5 volts	3.08983	0.117
227	VSSA	Power - 0 volts	2.93983	0.117
228	VSSD (Core)	Power - 0 volts	2.78983	0.117
229	VDDD (Core)	Power - 2.5 volts	2.63983	0.117
230	Substrate (Core)	Power - 0 volts	2.48983	0.117
231	PlsrOut	Diagnostic	2.33983	0.117
232	VSSA	Power - 0 volts	2.18983	0.117
233	PlsrCommon	Programmable Voltage; Decouple	2.03983	0.117
234	Vref	Programmable Voltage; Decouple	1.88983	0.117
235	VbbpMaster	Programmable Voltage; Decouple	1.73983	0.117
236	VDDA_B	Power - 2.5 volts	1.58983	0.117
237	GNDA_B	Power - 0 volts	1.43983	0.117
238	DisVtp<0>	Programmable Voltage; Decouple	1.28983	0.117
239	DisVtn	Programmable Voltage; Decouple	1.13983	0.117
240	Substrate (PI)	Power - 0 volts	0.98983	0.117
241	VDDD (PI)	Power - 2.5 volts	0.83983	0.117
242	VSSD (PI)	Power - 0 volts	0.68983	0.117
243	Substrate	Power - 0 volts	0.53983	0.117

Some notes on power supplies

This chip was designed with the assumption that it would sit on or near a two power planes, one 2.5±0.25 volt and the other 0±0.25 volt. There is no need to separate analog power and analog ground from digital power and digital ground. That is done on the chip. From the board designers' point of view, there is no difference between, for example, VDDD (PI) and VDDD (Core). However, it has also been assumed by that chip designers that all power supplies will be very well decoupled and that that decoupling will be done as close as possible to the chip. If the chip is not adequately decoupled, then it should be assumed that the chip will not work.

A quick note on resetting

Simply put, this chip must be reset in order to work properly. Until the chip has been reset, it should be assumed that the data coming out of the chip is garbage. The reset can be either a Master Reset or a programmed Smart Core Reset. Users of the chip should not be fooled by the robust natures of the data interface and the programming interface. They have been designed to be "self starting". The Core is another matter. It is theoretically possible – however unlikely it may be - that the Core could be powered on and it will appear as if it already has data to transmit. This, of course, would be nonsense attributable to the unpredictable starting value of positive feedback-based CMOS registers. Therefore, the FSSR2 must be reset before it can be expected to produce reliable, reproducible data.

Default Values

After a Master Reset, the registers in the Programming Interface have the following values.

No.	Register	Default	Notes
1	Pulser Data	0	
2	Pulser Control	0	
3	Integrator Vbn	139	Rarely changed
4	Shaper Vbp2	116	
5	Shaper Vbp1	121	
6	Base-line Restorer Vbp1	80	
7	Discriminator Vtn	FF	
8	Discriminator Vtp<0>	0	
9	Discriminator Vtp<1>	0	
10	Discriminator Vtp<2>	0	
11	Discriminator Vtp<3>	0	
12	Discriminator Vtp<4>	0	
13	Discriminator Vtp<5>	0	
14	Discriminator Vtp<6>	0	
15	Discriminator Vtp<7>	0	
16	Active Lines	0	0= 1 Line, 1= 2 Lines, 2= 4 Lines, 3= 6 Lines
17	Kill Select	N/A	
18	Inject Select	N/A	
19	Send Data	0	0= Send No Data 1= Send Data
20	Reject Hits	1	0= Accept Hits 1= Reject Hits
24	Smart Programming Reset	N/A	
27	Digital Control Register	0	
28	Smart Core Reset	N/A	Default Command = Reset Hits Reset Command = Reset BCO Counter Set Command = Reset Hits and BCO Counter
30	Acquire BCO Number	0	

The Digital Control Register is simply a programmable set of values rolled into one register to save on address space. The 8-bit register defaults to 0, and its individual bits are as follows:

No.	Bit	Default	Notes
0	Shaper Select Low	0	
1	Shaper Select High	0	
2	Feedback Cap Select	0	
3	Disable BLR	0	0= BLR enabled, 1= BLR disabled
4	Mod 255	0	0= Mod 159, 1= Mod 255
5	Unused	0	
6	Unused	0	
7	Unused	0	

With the Feedback Cap Select set to 0, the preamp gain is 1.626 $\mu V/e^-$. With the Feedback Cap Select set to 1, the preamp gain is 1.084 $\mu V/e^-$. There is an additional gain of 10 between the output of the preamp and the output of the shaper.

The two Shaper Select bits set the shaping time. The approximate shaping times are as follows:

Shaper Select High	Shaper Select Low	Approximate Shaping Time
0	0	65ns
0	1	85ns
1	0	100ns
1	1	125ns

References

[1] R. Yarema, J. Hoff, A. Mekkaoui, M Manghisoni, V. Re, *et al*, “Fermilab Silicon Strip Readout Chip for BTeV”, FERMILAB-PUB-04-260-E, presented at the IEEE Nuclear Science Symposium, Rome, Italy, 2005. To be published in IEEE Trans. Nucl. Sci. Date: TBD.