Brevissima introduzione all’elettronica analogica (transistor, etc. ...)

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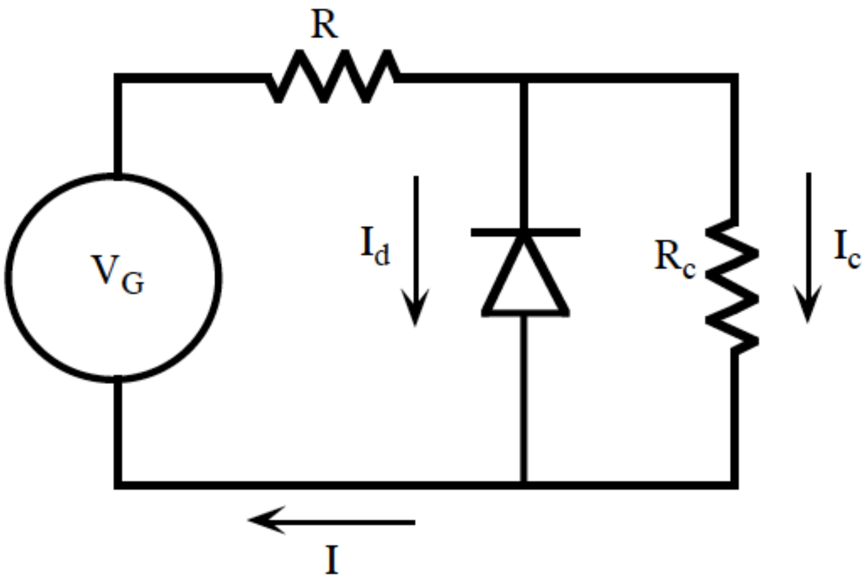
Corso di Metodi di Trattamento dei Segnali

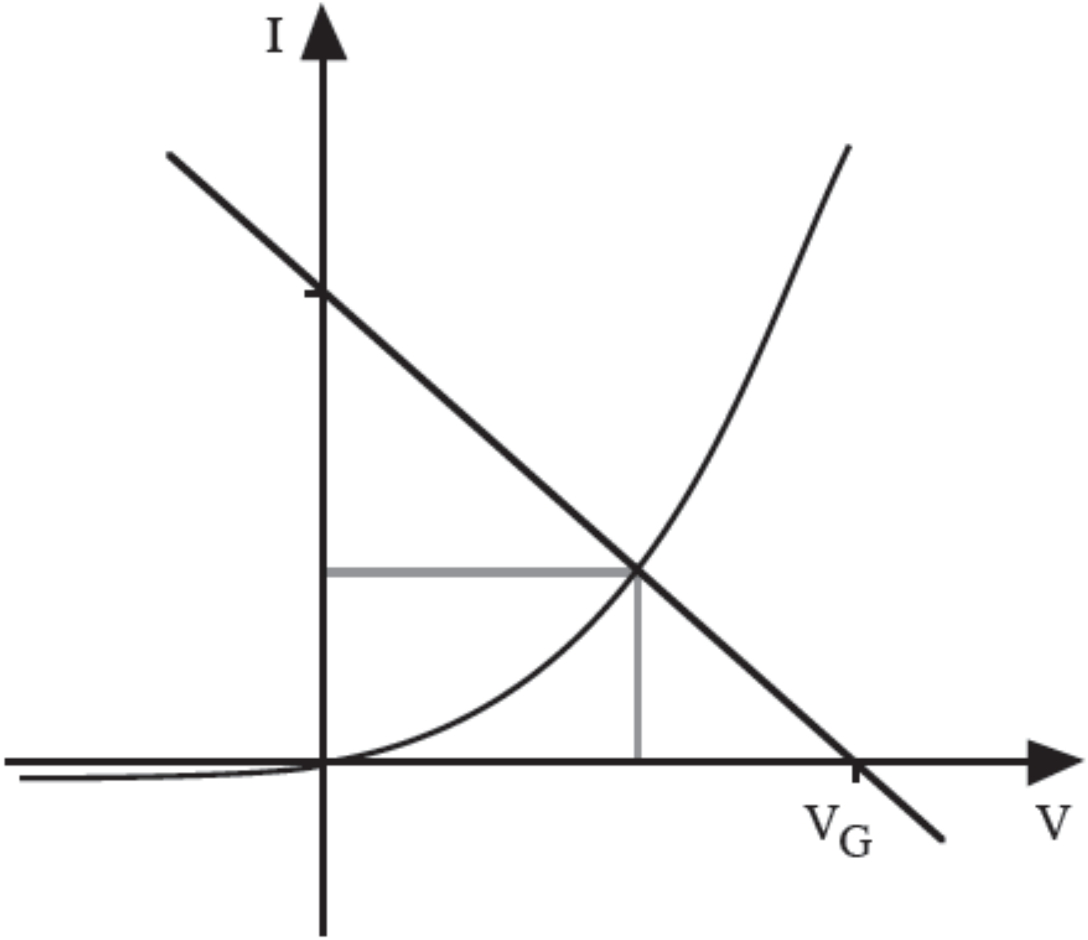
A. A. 2016-17

Soluzione di problemi non lineari in elettronica: il metodo della retta di carico



$$\begin{cases} V_G = IR + V_d \\ V_d = I_c R_c \\ I = I_d + I_c \\ V_d = V_d(I_d) \end{cases}$$

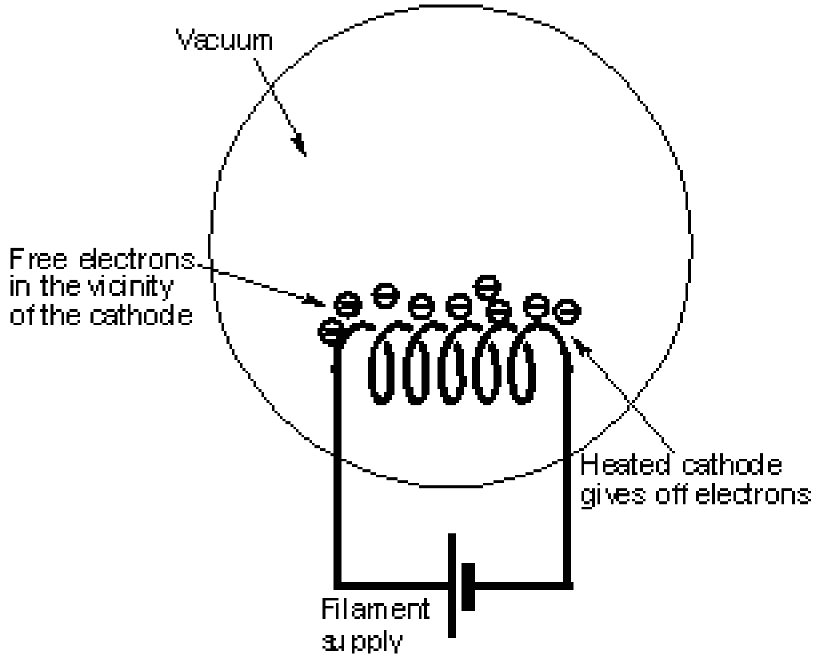
$$
\begin{cases}
V_G = I_d R + V_d \left(1 + \dfrac{R}{R_c} \right) \\
V_d = V_d(I_d)
\end{cases}
$$

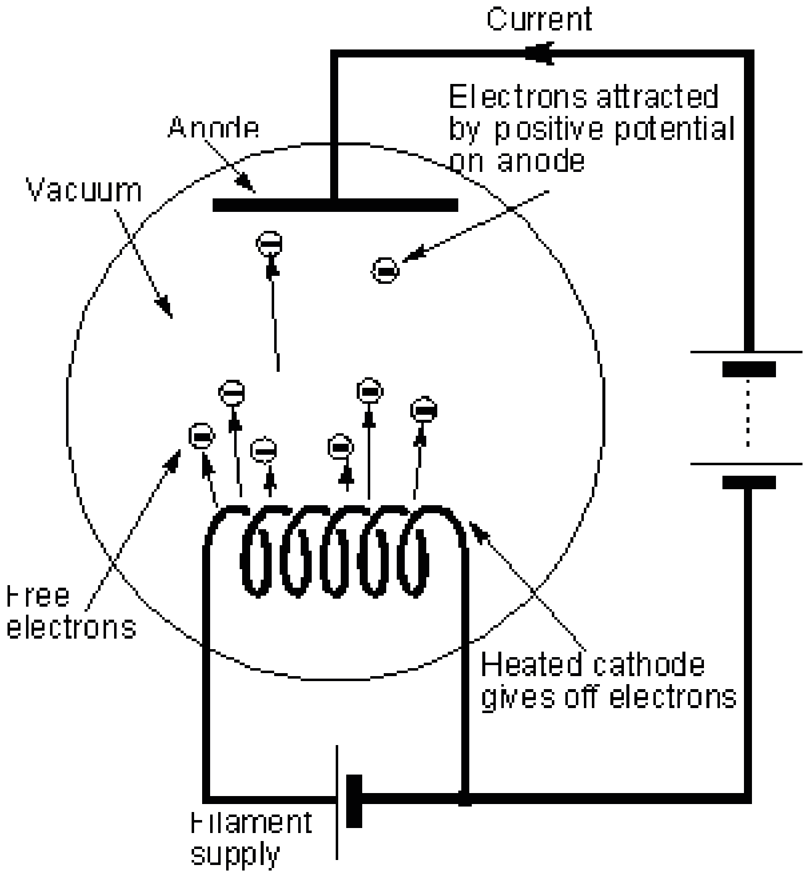


Gli inventori del transistor bipolare (premi Nobel nel 1956): da sinistra; e John Bardeen, William P. Shockley, e Walter H. Brattain (il primo ha vinto un secondo premio Nobel nel 1972 insieme a Cooper e Schrieffer per la teoria della superconduttività).

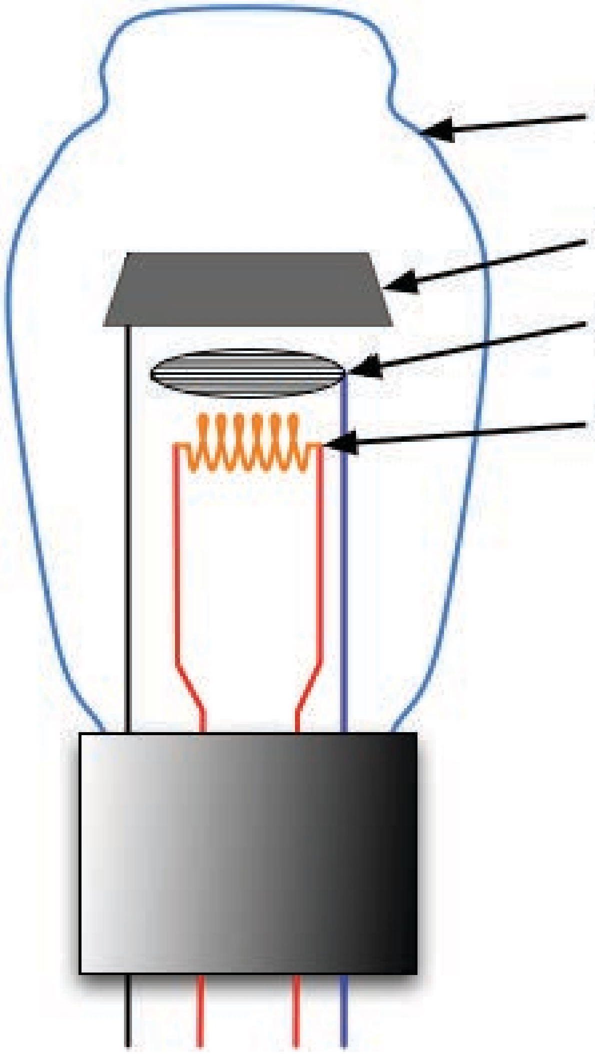

microelectronics group
Lucent Technologies
Bell Labs Innovations
A replica of the first transistor, invented at Bell Labs, December 23, 1947
50 Years and Counting...

Diodo a vuoto





Triodo



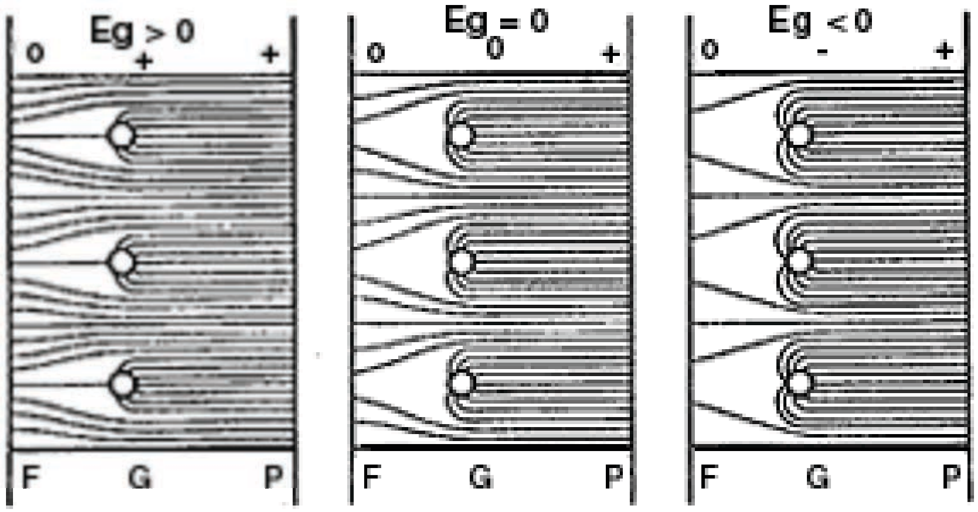
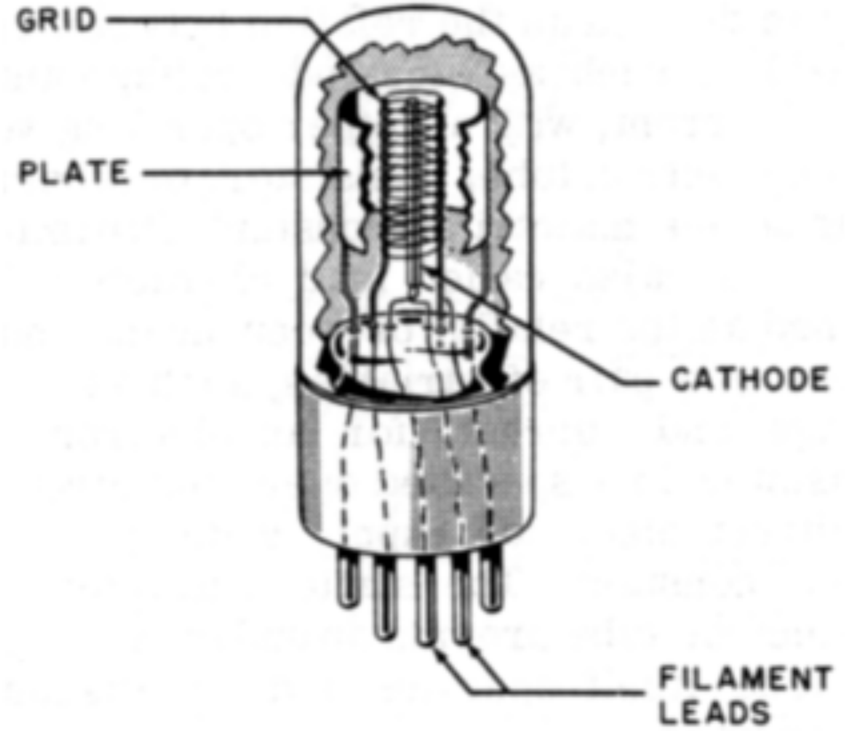
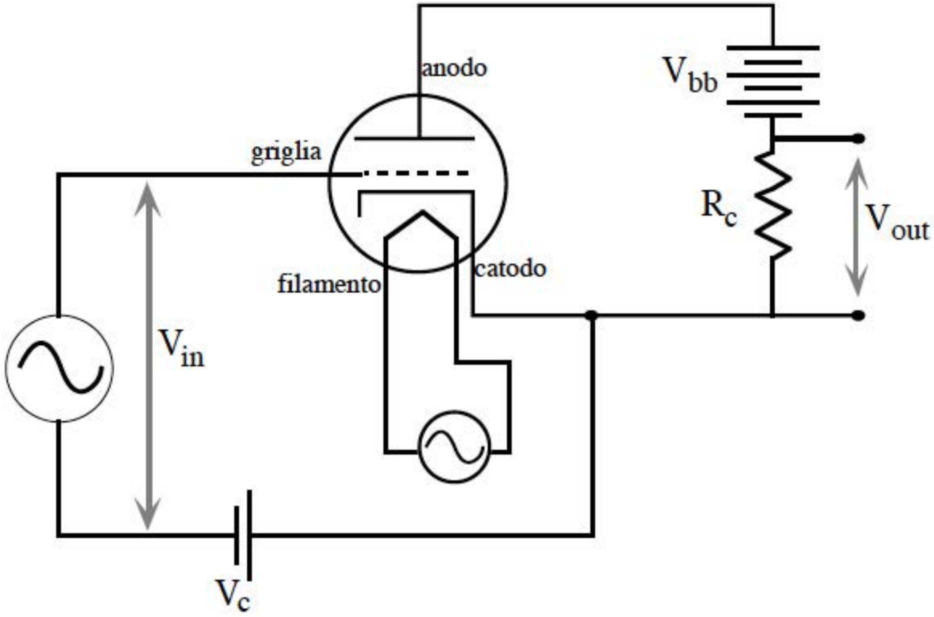
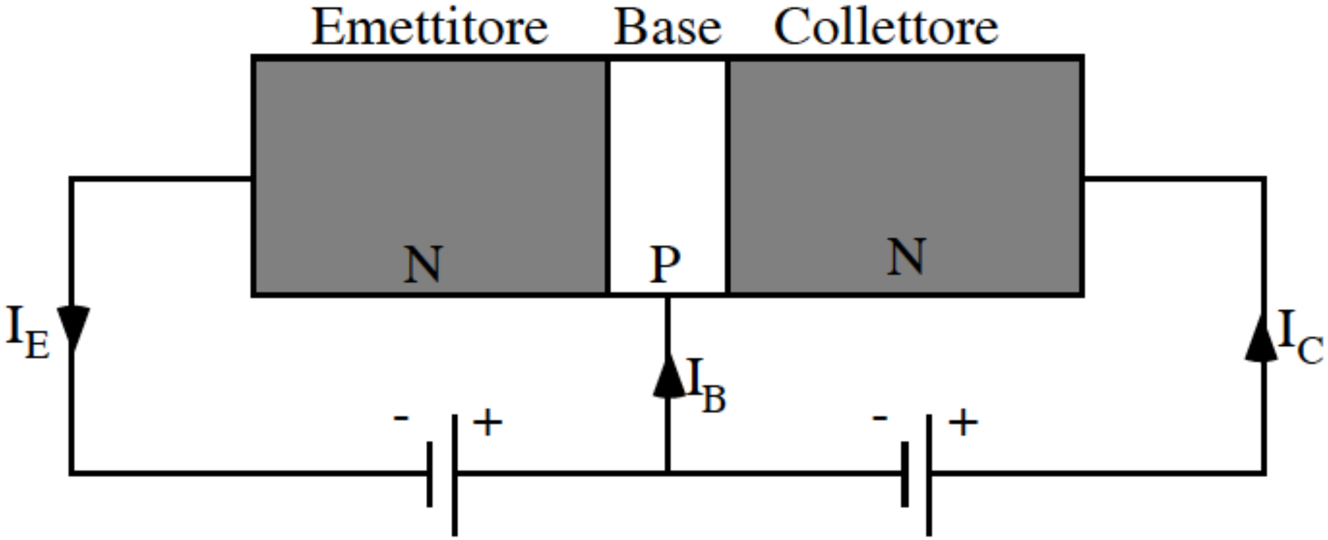


Figure 4 - Shows how changing the voltage on the grid of a triode controls the current through the tube.

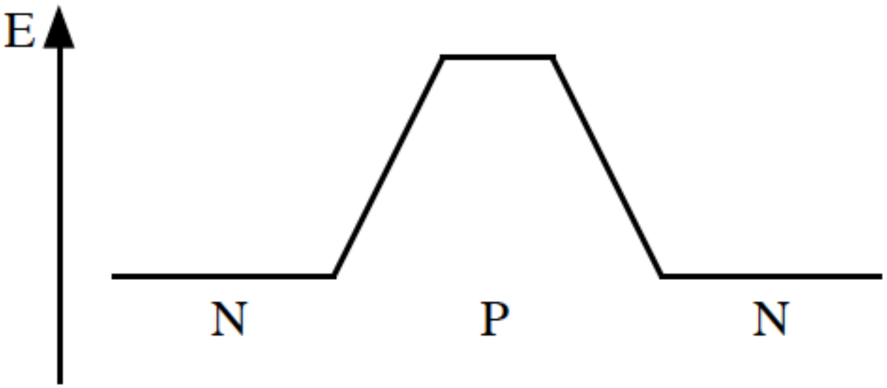

GRID
PLATE
CATHODE
FILAMENT LEADS

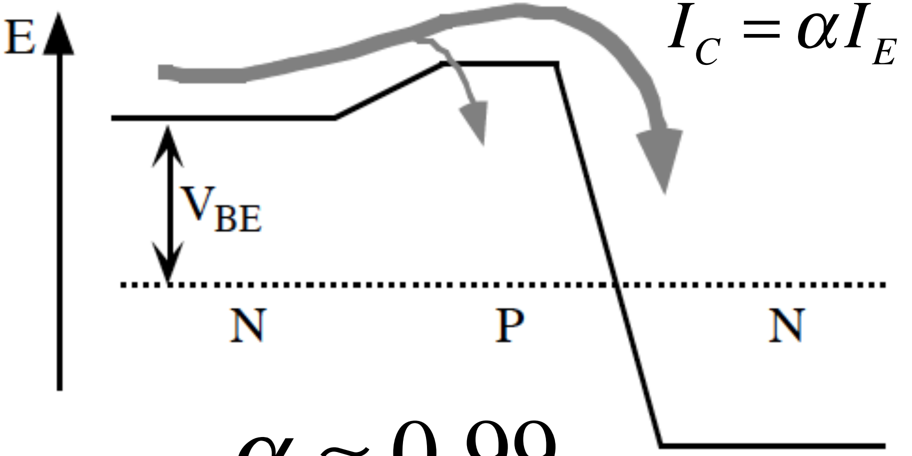

anodo
V_{bb}
griglia
R_c
V_{out}
filamento
catodo
V_{in}
V_c


VALVO
VALVO
EZ80
MADE IN HOLLAND



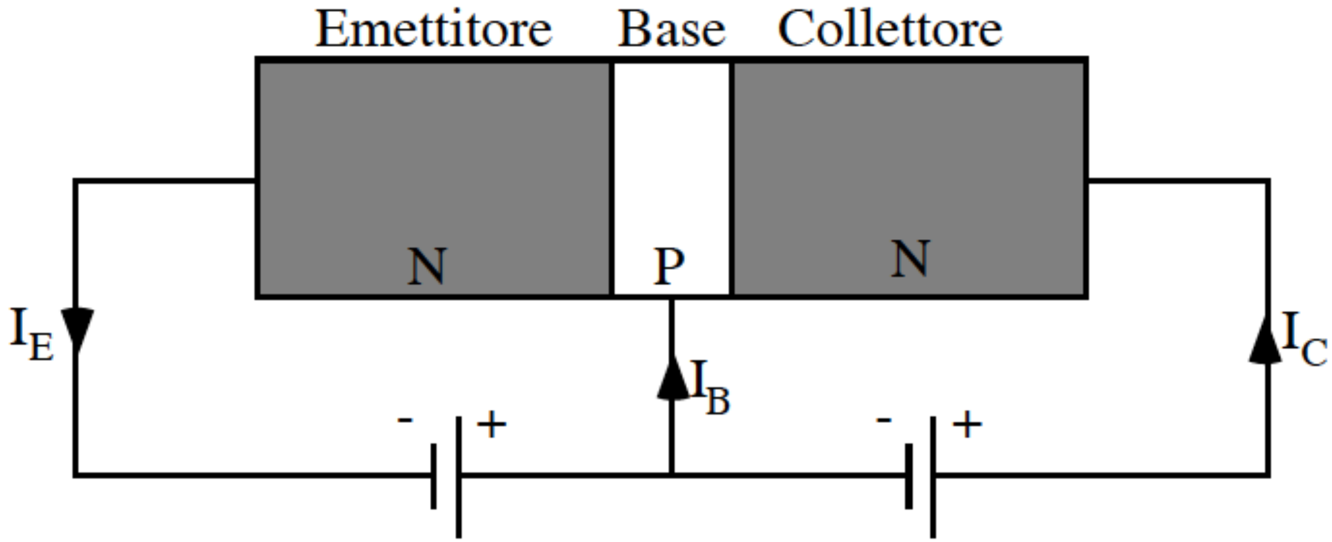
Buona parte della corrente di emettitore va nel collettore





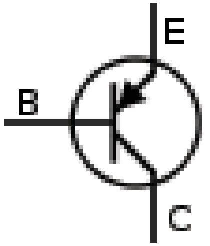
$$I_C = \alpha I_E$$

$$\alpha \approx 0.99$$

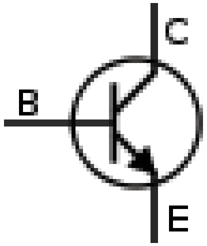


$$I_E = I_B + I_C \quad \text{e inoltre} \quad I_C = \alpha I_E$$

$$\Rightarrow \quad I_E = \frac{1}{1-\alpha} I_B \quad \text{e} \quad I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B$$



transistor bipolare
PNP

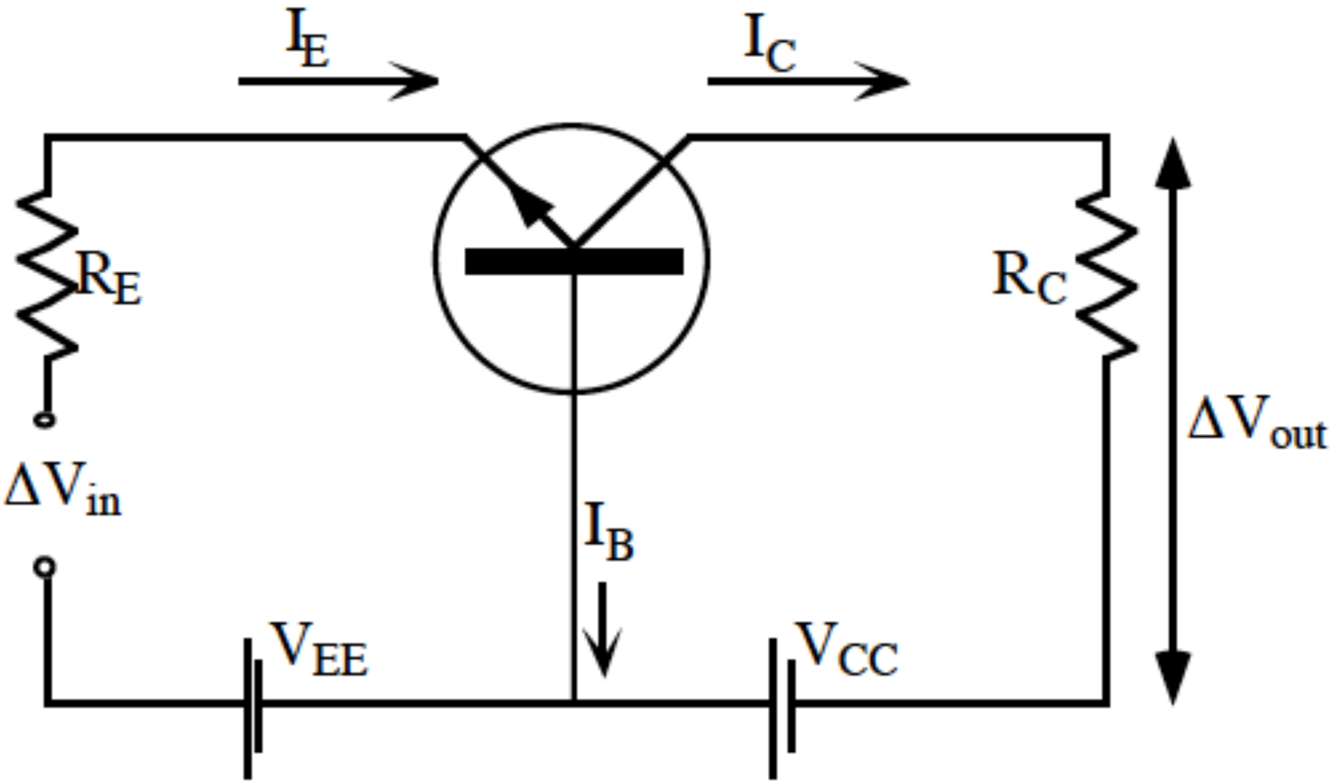


transistor bipolare
NPN

Le regole basilari del funzionamento dei transistor *npn* sono le seguenti:

1. Il collettore deve essere "più positivo" dell'emettitore
2. Le giunzioni base-emettitore e base collettore sono due diodi (e quindi $V_B \approx V_E + 0.6$ Volt)
3. I_B, I_C, I_E hanno dei valori massimi che non possono superare, pena la distruzione del transistor
4. $I_C = \frac{\alpha}{1-\alpha} I_B = \beta I_B$

Configurazione a base comune

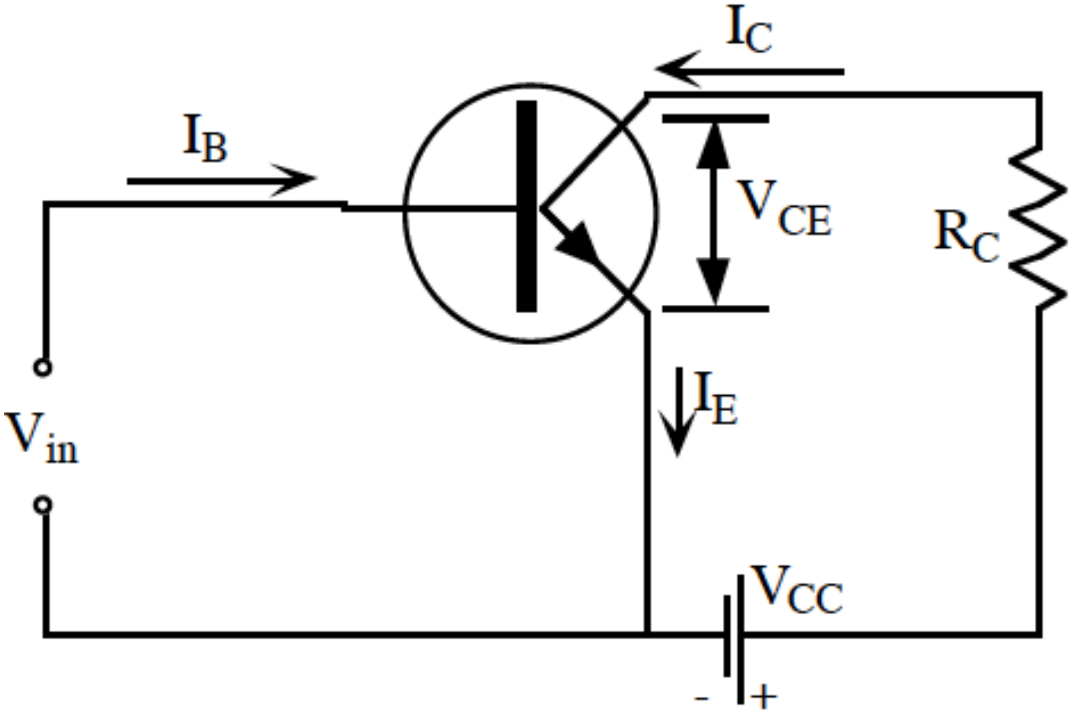


$$\Delta V_{in} + V_{EE} = R_E I_E + V_{BE}$$
$$V_{out} = R_C I_C$$
$$R_C I_C - V_{BC} = V_{CC}$$
$$I_C = I_E - I_B = \alpha I_E$$

$$\Delta I_C = \alpha \Delta I_E = \alpha \frac{\Delta V_{in}}{R_E}$$

$$\Delta V_{out} = R_C \Delta I_C = \alpha \frac{R_C}{R_E} \Delta V_{in}$$

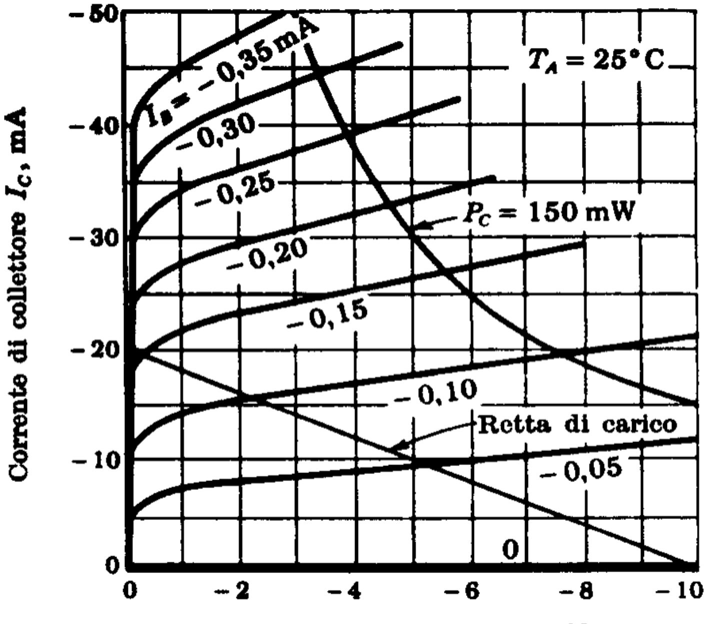
Configurazione a emettitore comune e curve caratteristiche



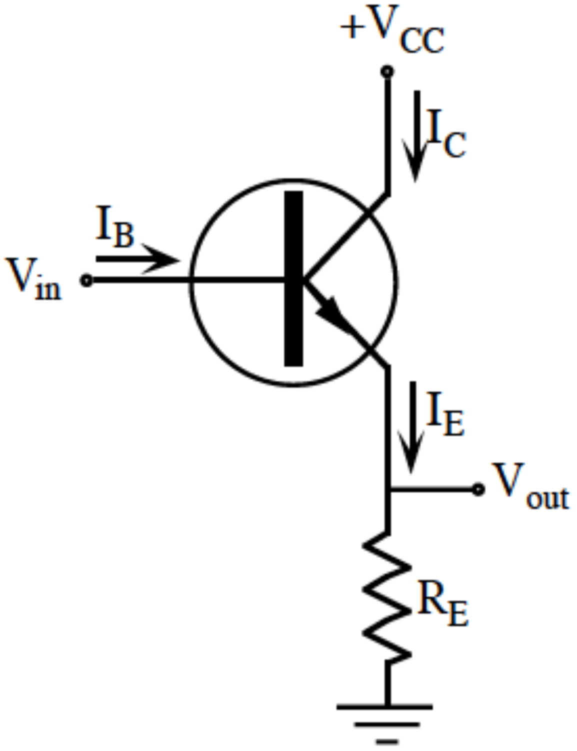
$$V_{CC} = V_{CE} + I_C R_C$$

$$I_C = I_C\left(I_B, V_{CE}\right)$$

soluzione con il metodo della retta di carico



Emitter follower



$$V_{in} - V_{out} = V_{BE} \approx 0.6V$$

$$I_E = I_B + I_C = (1+\beta) I_B$$

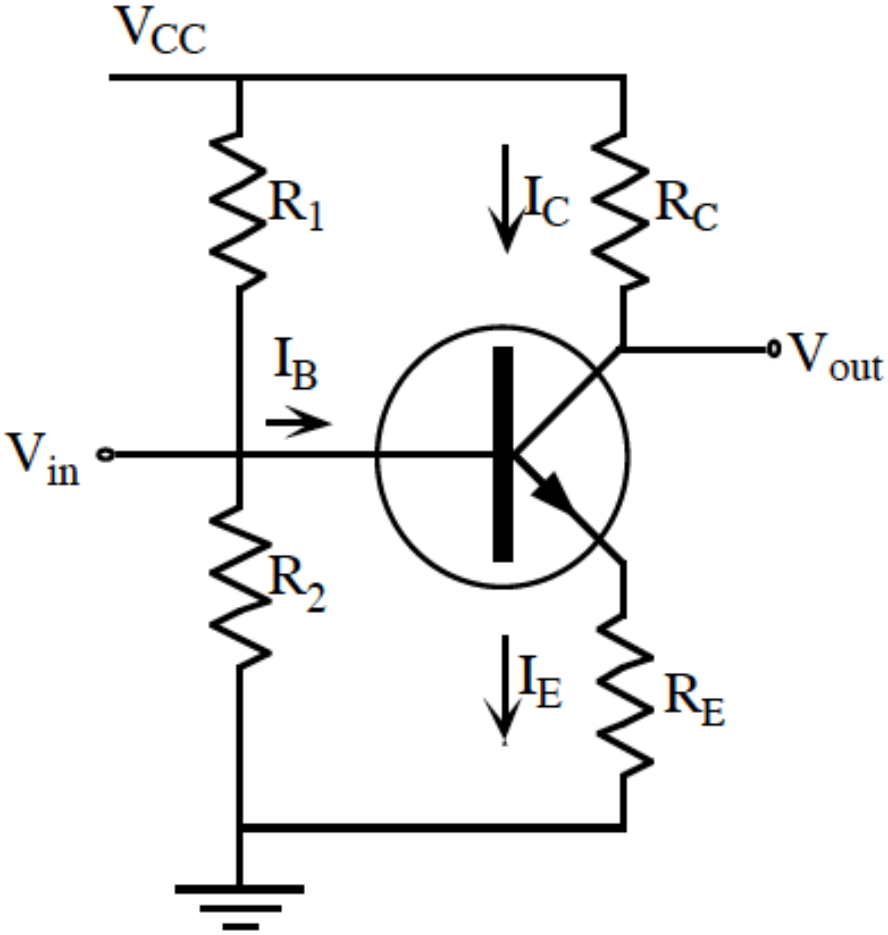
$$\Delta V_{in} \approx \Delta V_{out}$$

$$\Delta I_E = (1+\beta) \Delta I_B$$

$$Z_{in} = \frac{\Delta V_{in}}{\Delta I_B} \approx (1+\beta) \frac{\Delta V_{out}}{\Delta I_E} = (1+\beta) Z_{out}$$

applicazioni: adattamento di impedenza, aumento della potenza del segnale

Amplificatore ad emettitore comune



$$V_{out} = V_C = V_{CC} - I_C R_C$$

$$\Delta V_{in} = \Delta V_B \approx \Delta V_E$$

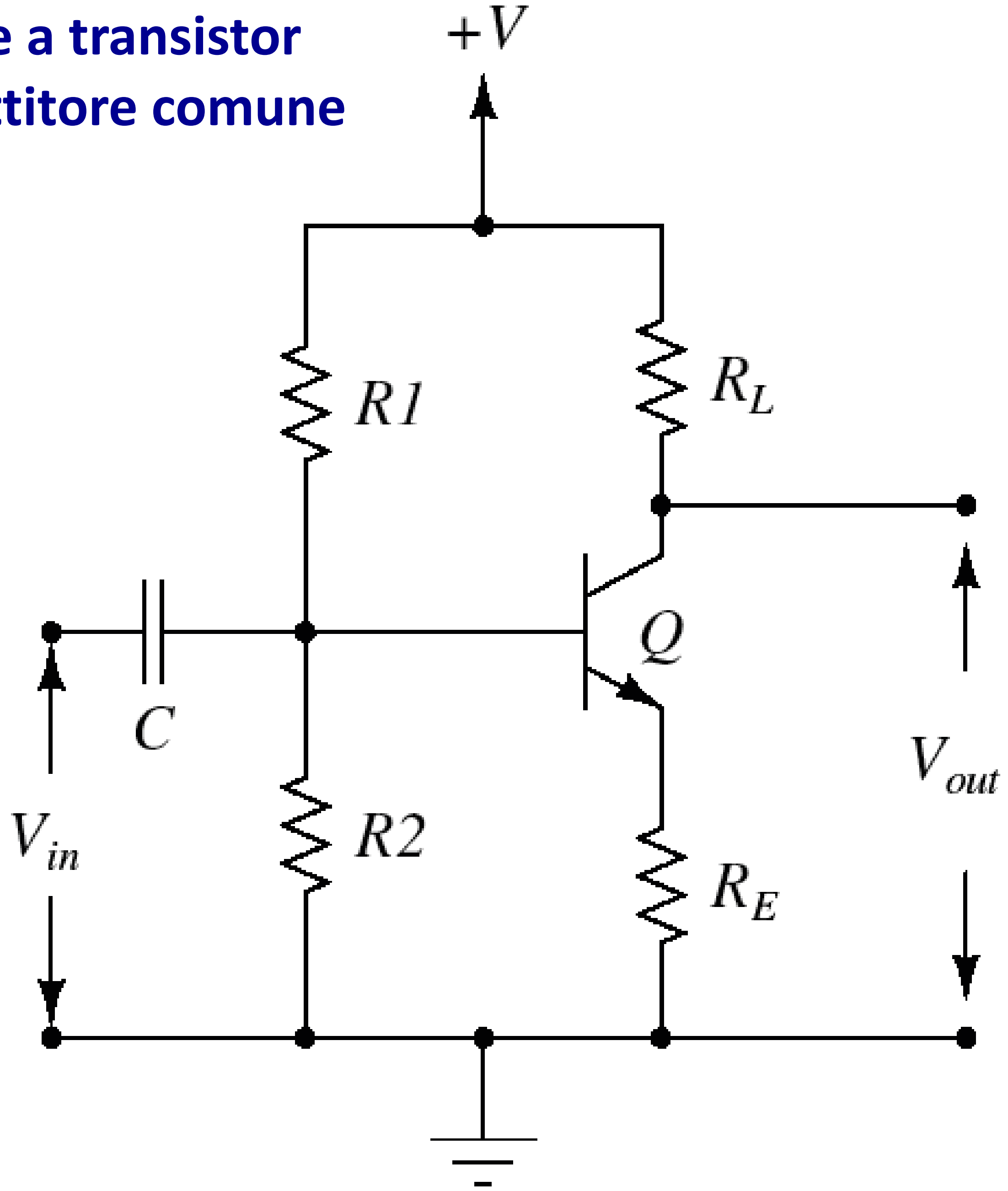
$$\Delta V_E = R_E \Delta I_E \approx R_E \Delta I_C$$

$$\Delta V_{out} = \Delta V_C = -R_C \Delta I_C$$

$$G = \frac{\Delta V_{out}}{\Delta V_{in}} \approx -\frac{R_C}{R_E}$$

amplificatore invertente!

Progetto di un amplificatore a transistor nella configurazione a emettitore comune con un transistor 2N3904



NPN switching transistor 2N3904

FEATURES

- Low current (max. 200 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- High-speed switching.

DESCRIPTION

NPN switching transistor in a TO-92; SOT54 plastic package. PNP complement: 2N3906.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter

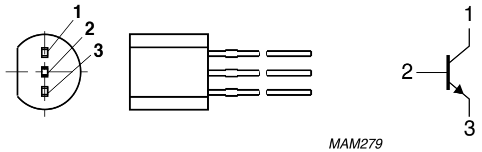


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

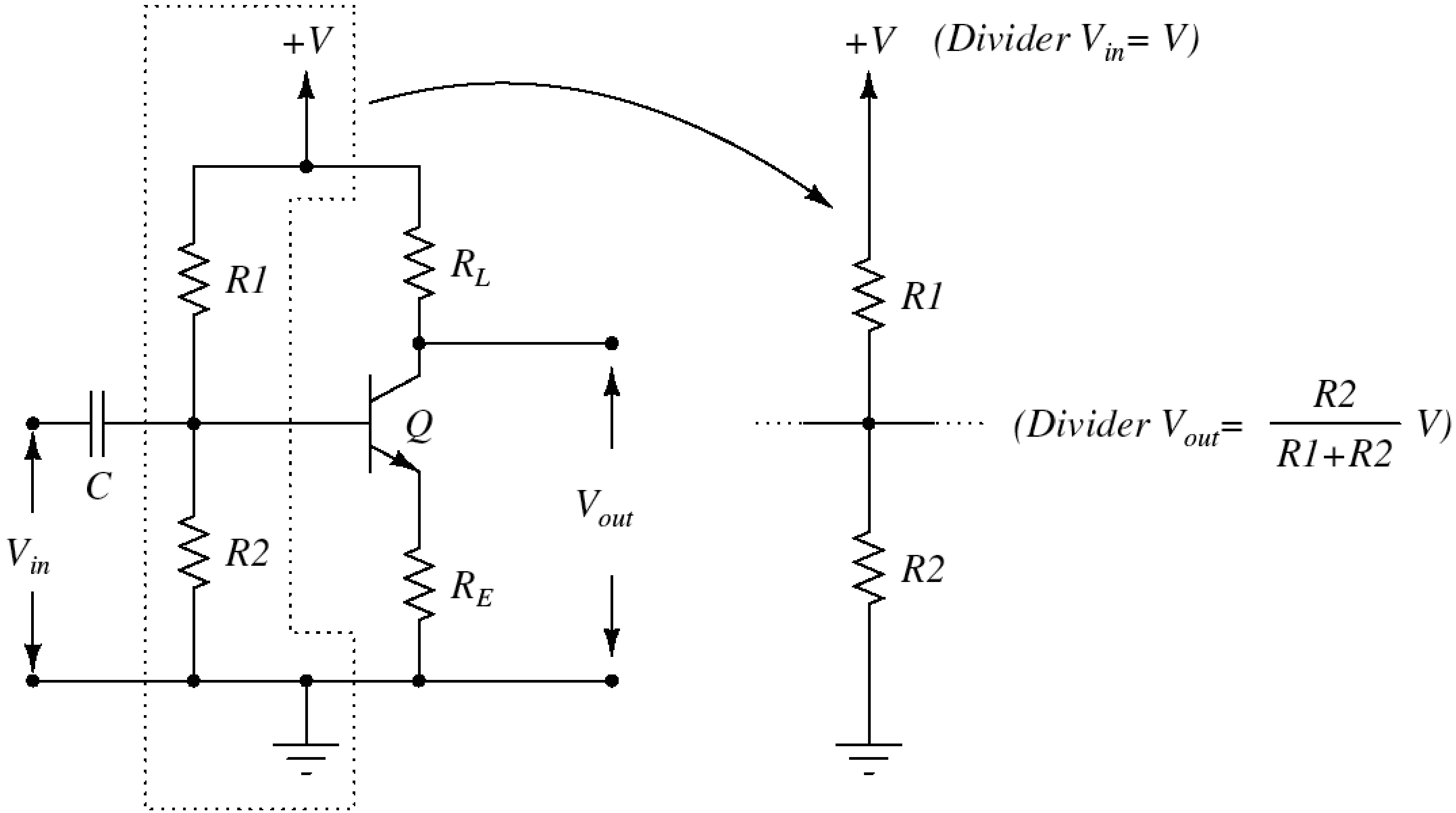
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	200	mA
I_{CM}	peak collector current		–	300	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \le 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

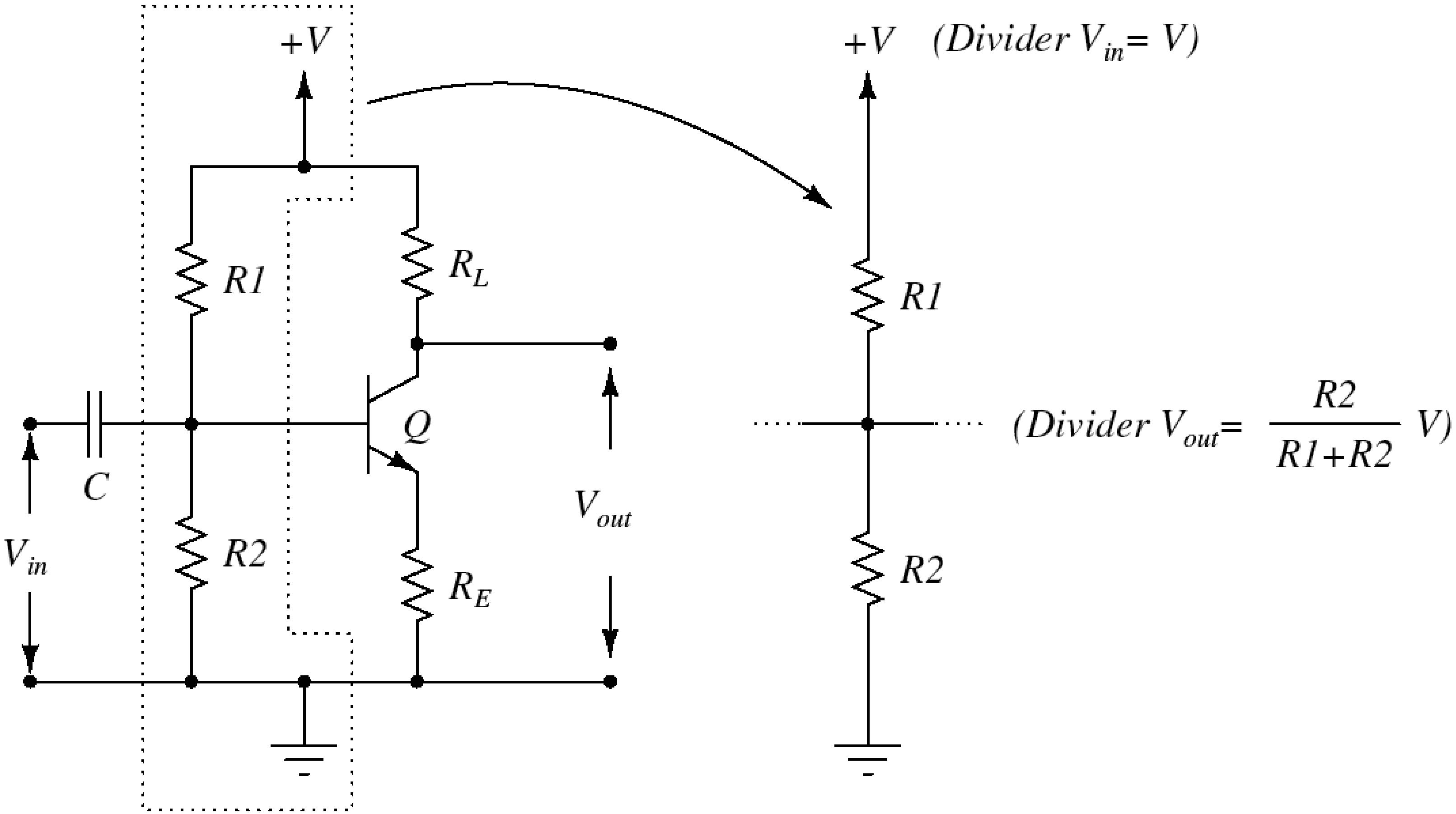
Note

1. Transistor mounted on an FR4 printed-circuit board.



Nel circuito possiamo isolare una parte (segnata nel tratteggio) che rappresenta un partitore che costituisce la rete di polarizzazione della base: la scelta delle resistenze del partitore seleziona il punto di lavoro dell'amplificatore.

In modo del tutto analogo le resistenze R_L, R_E e il transistor costituiscono una specie di partitore con una resistenza variabile (il transistor): la conseguenza è che la tensione di uscita può variare tra 0V e la tensione di alimentazione +*V*.



$$\Delta V_{in} = \Delta V_B \approx \Delta V_E = R_E \Delta I_E \approx R_E \Delta I_C$$

$$\Delta V_{out} = \Delta V_C = -R_L \Delta I_C$$

$$G = \frac{\Delta V_{out}}{\Delta V_{in}} \approx -\left(\frac{R_L}{R_E} \right)$$

Definizione dei parametri del circuito

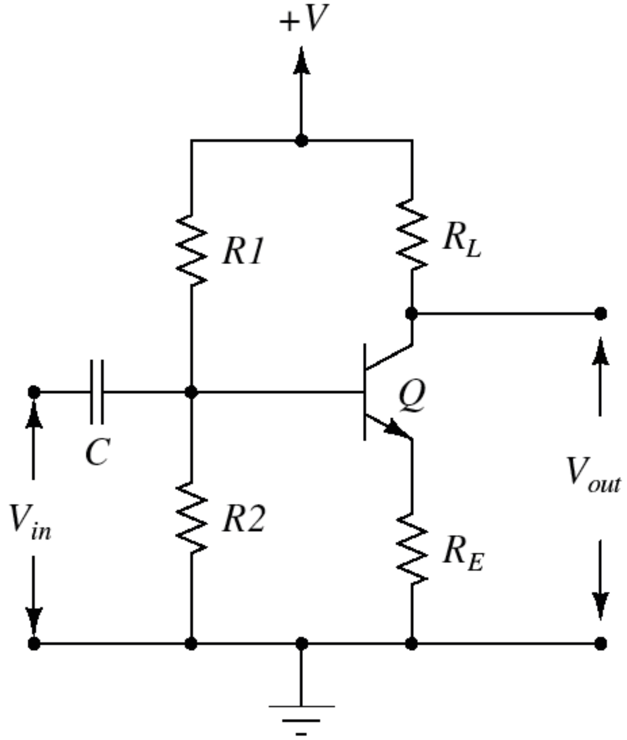
- la prima scelta l’abbiamo già fatta: abbiamo preso una configurazione di amplificatore a emettitore comune.

- a questo punto scegliamo la tensione di alimentazione: come si è visto questo determina l’escursione massima in tensione del segnale amplificato. Questa scelta dipende da molti fattori, tra cui il tipo di alimentatore disponibile e le caratteristiche dei transistor che abbiamo a disposizione: in pratica si tratta sempre di una tensione dell’ordine della decina di volt.
  Noi scegliamo una tensione di 10V che è compatibile con la tensione massima emettitore-collettore di questo transistor (40V) ed è facile da ottenere con gli alimentatori normalmente disponibili in laboratorio.

- **scegliamo ora la corrente quiescente della maglia di uscita.** Questa corrente viene determinata a partire dalle caratteristiche del transistor. In questo caso la corrente di collettore massima accettabile è di 200 mA, mentre la dissipazione termica in condizioni ordinarie è di 0.5 W circa. Così con una tensione (massima) emettitore-collettore di 10V si ottiene la dissipazione (massima) di 0.5W con una corrente di 50 mA.

Questo sta all'interno del limite di 200 mA, ma è una corrente piuttosto alta se prendiamo delle resistenze di polarizzazione dell'ordine del kOhm (non possiamo prendere delle resistenze troppo piccole se non vogliamo che un carico tra quelli ordinariamente disponibili modifichi eccessivamente la rete di polarizzazione del transistor). Infatti la dissipazione di potenza su 1 kOhm diventa in questo caso 2.5 W, una potenza piuttosto elevata, che comporta l'utilizzo di componenti meccanicamente piuttosto grandi.

Se vogliamo utilizzare le normali resistenze da 1/4 W o da 1/2 W, dobbiamo abbassare la corrente: prendiamo un valore più piccolo, $I_C = 4$ mA. Con questa corrente il "partitore" di uscita si comporta in modo che la resistenza equivalente totale abbia 10V/4mA = 2.5 kOhm. La tensione quiescente di uscita viene posta allora a V/2 (=5V) se si prende R_L = 2.5 kOhm /2 = 1.25 kOhm.



È buona pratica prendere la resistenza di emettitore grande almeno $R_L/10$: qui noi prendiamo $R_E=R_L/3$, vale a dire $R_E \approx$ 417 Ohm. Questo significa che l'amplificatore ha guadagno G=3 e che la tensione di emettitore è

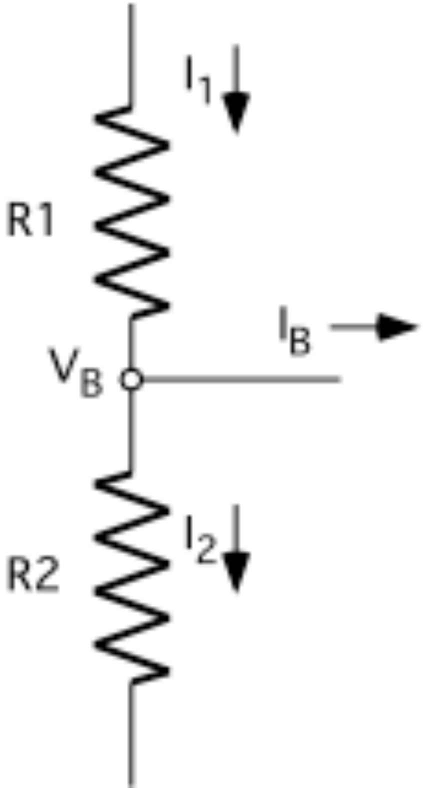
$$V_E \approx 417\Omega \cdot 4\mathrm{mA} \approx 1.7V$$

e la tensione di base è circa 0.6V più alta, vale a dire circa $V_B \approx$ 2.3V.

- per completare la scelta delle resistenze dobbiamo determinare i valori delle resistenze R1 e R2: per farlo in modo corretto dovremmo conoscere l’esatto valore di *beta* del nostro transistor, ma dal datasheet si trova che esso varia tipicamente tra 70 e 300, e per questo noi prendiamo il valore *beta* = 100.

Questo vuol dire che la corrente di base è 100 volte più piccola della corrente di collettore, e quindi vale 40µA.

La figura mostra come si divide la corrente nel partitore di ingresso; devono valere quindi le seguenti equazioni:



$$I_1 = I_2 + I_B$$

$$I_1 R_1 = V - V_B$$

$$I_2 R_2 = V_B$$

$$I_1 = \frac{V_B}{R_2} + I_B$$

$$I_1 = \frac{V - V_B}{R_1}$$

$$I_2 = \frac{V_B}{R_2}$$

Il sistema non si può risolvere per trovare le correnti e le resistenze a meno che non si imponga una condizione aggiuntiva. Adesso però si può notare che la corrente nella resistenza R_2 deve essere molto maggiore della corrente di base, in modo che un cambiamento della corrente di base non influenzi il comportamento della rete: prendiamo dunque $I_2 = 10\, I_B$, allora

$$I_1 = \frac{V_B}{R_2} + I_B$$

$$I_1 = \frac{V - V_B}{R_1}$$

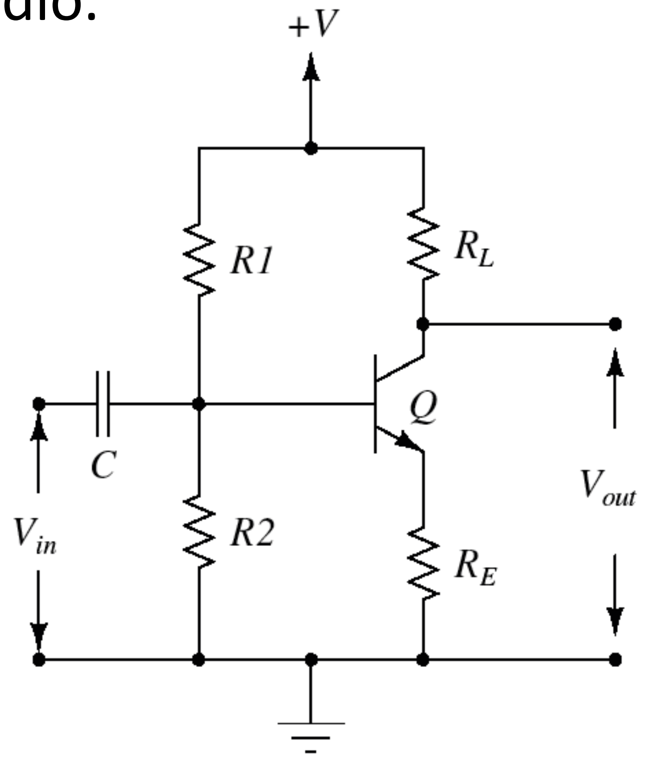
$$I_2 = \frac{V_B}{R_2}$$

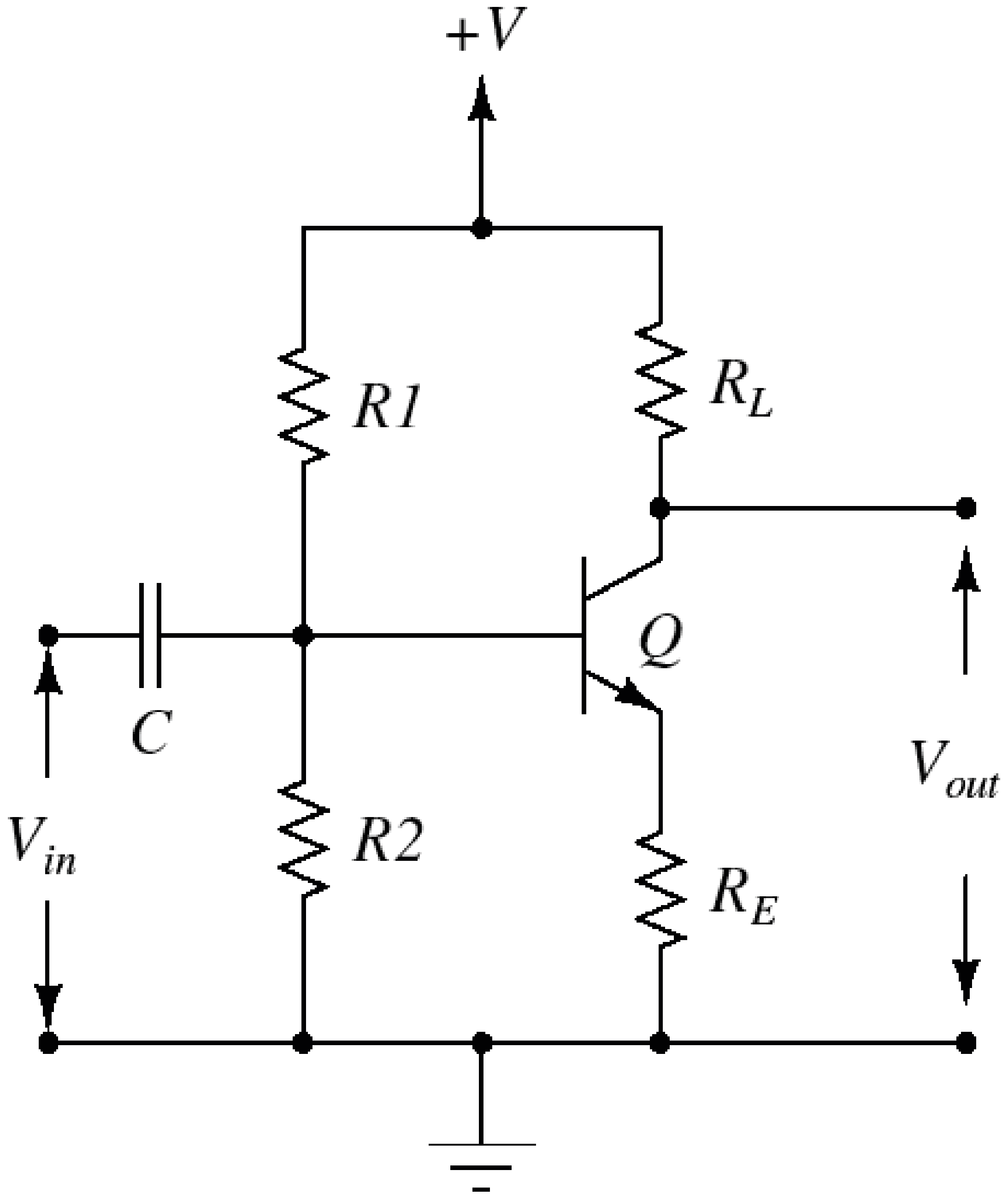
$$\Rightarrow$$

$$\frac{V_B}{R_2} \approx \frac{2.3V}{R_2} \approx 0.4mA; \quad R_2 \approx 5.75k\Omega$$

$$I_1 \approx 0.44mA \approx \frac{V - V_B}{R_1} = \frac{10V - 2.3V}{R_1} = \frac{7.7V}{R_1}; \quad R_1 \approx 17.5k\Omega$$

- la scelta del condensatore di disaccoppiamento dipende dalla resistenza R2 (che mette a terra il segnale in ingresso): insieme il condensatore e R2 costituiscono un filtro RC passa alto con una frequenza di taglio $1/R_2C$; ad esempio, se si prende un comune condensatore (non polarizzato) da 4.7 μF si ottiene una frequenza di taglio di 12 Hz; questa frequenza è adeguata per un amplificatore audio.





R_1 = 18 kΩ

R_2 = 6 kΩ

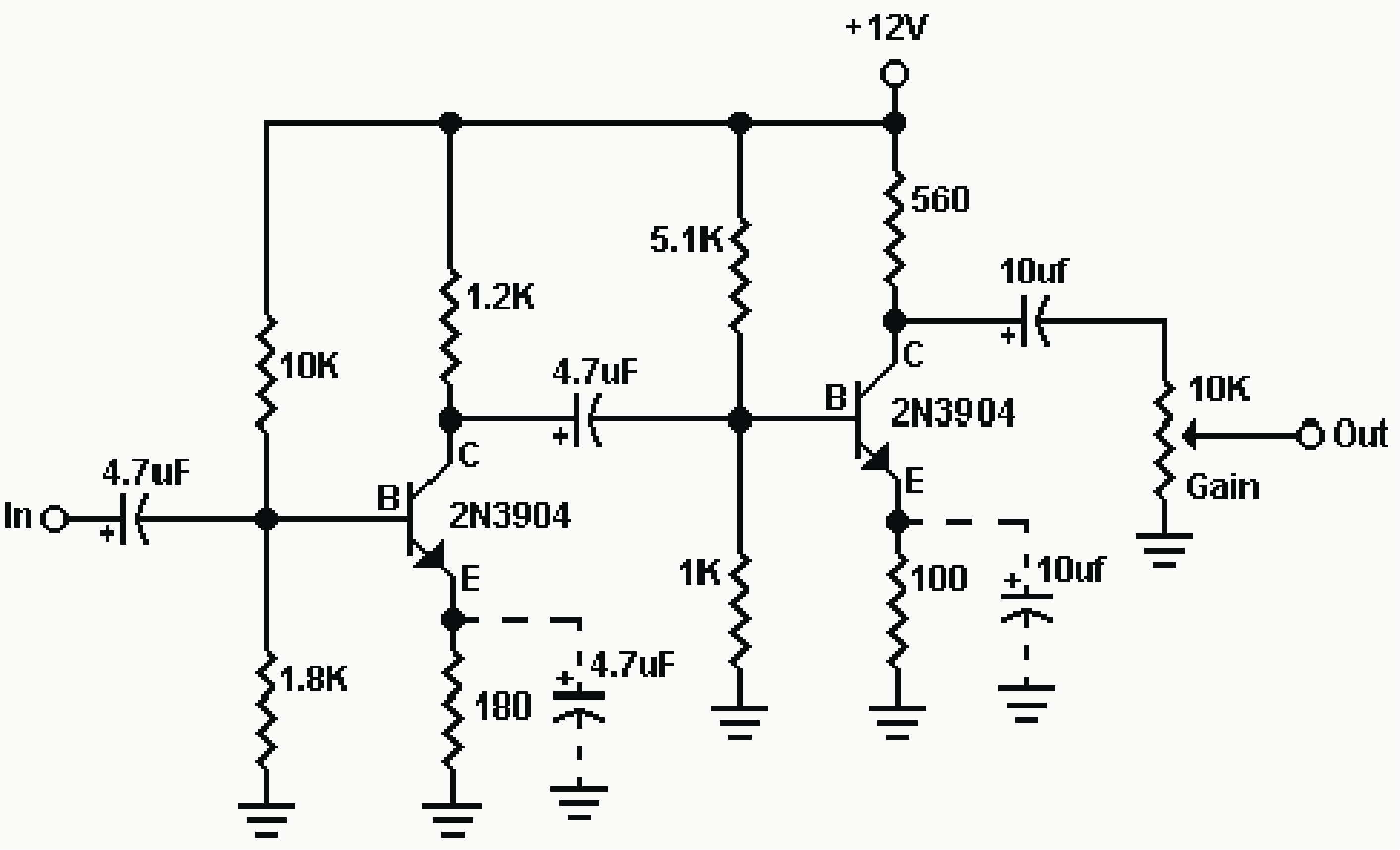
R_L = 1.25 kΩ

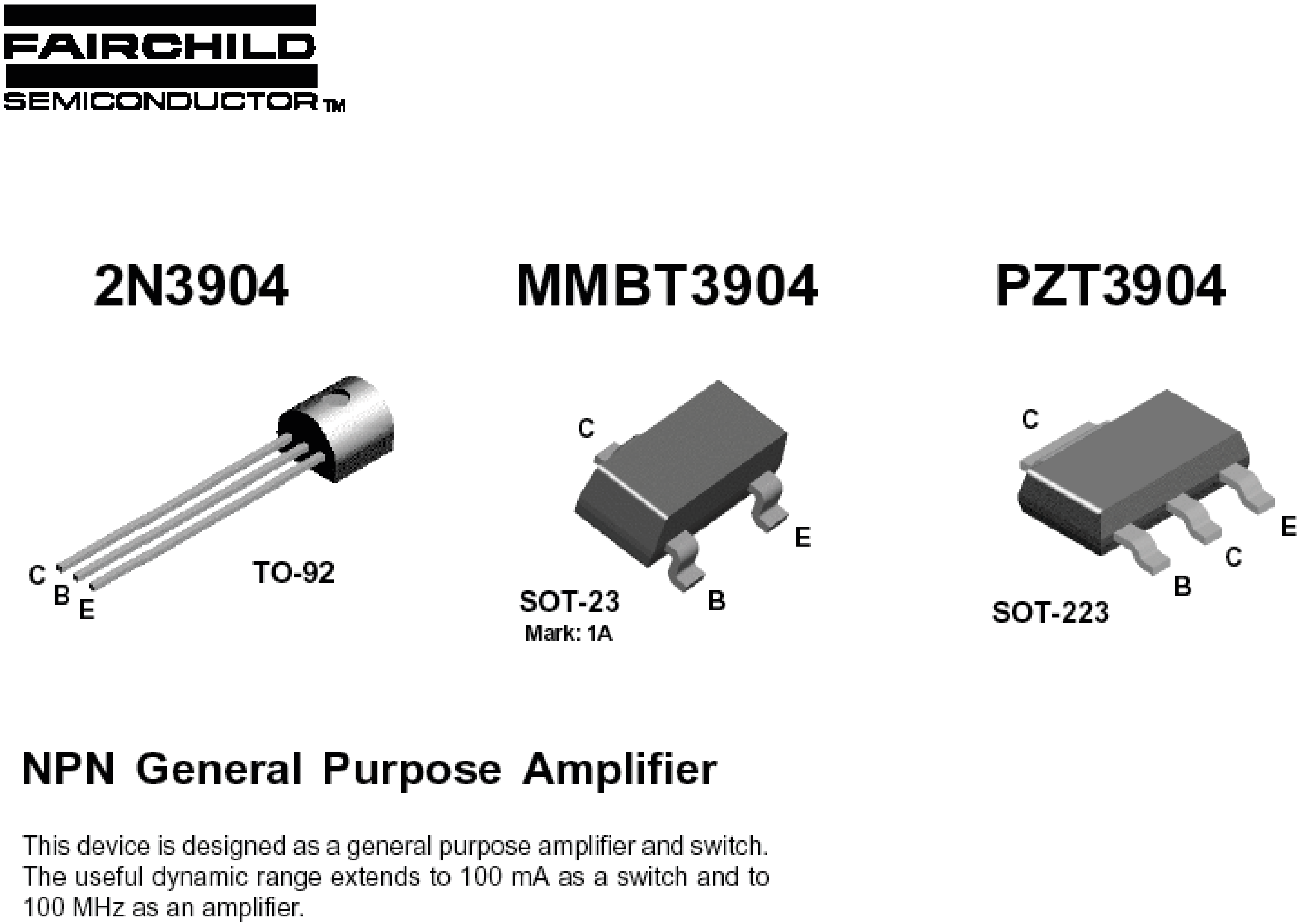
R_E = 420 Ω

C = 4.7 µF

Q = 2N3904

L'amplificazione non è elevata e potrebbe essere necessario aggiungere degli ulteriori stadi di amplificazione, come nella figura seguente, simile al circuito che abbiamo discusso, che mostra due emitter follower in cascata





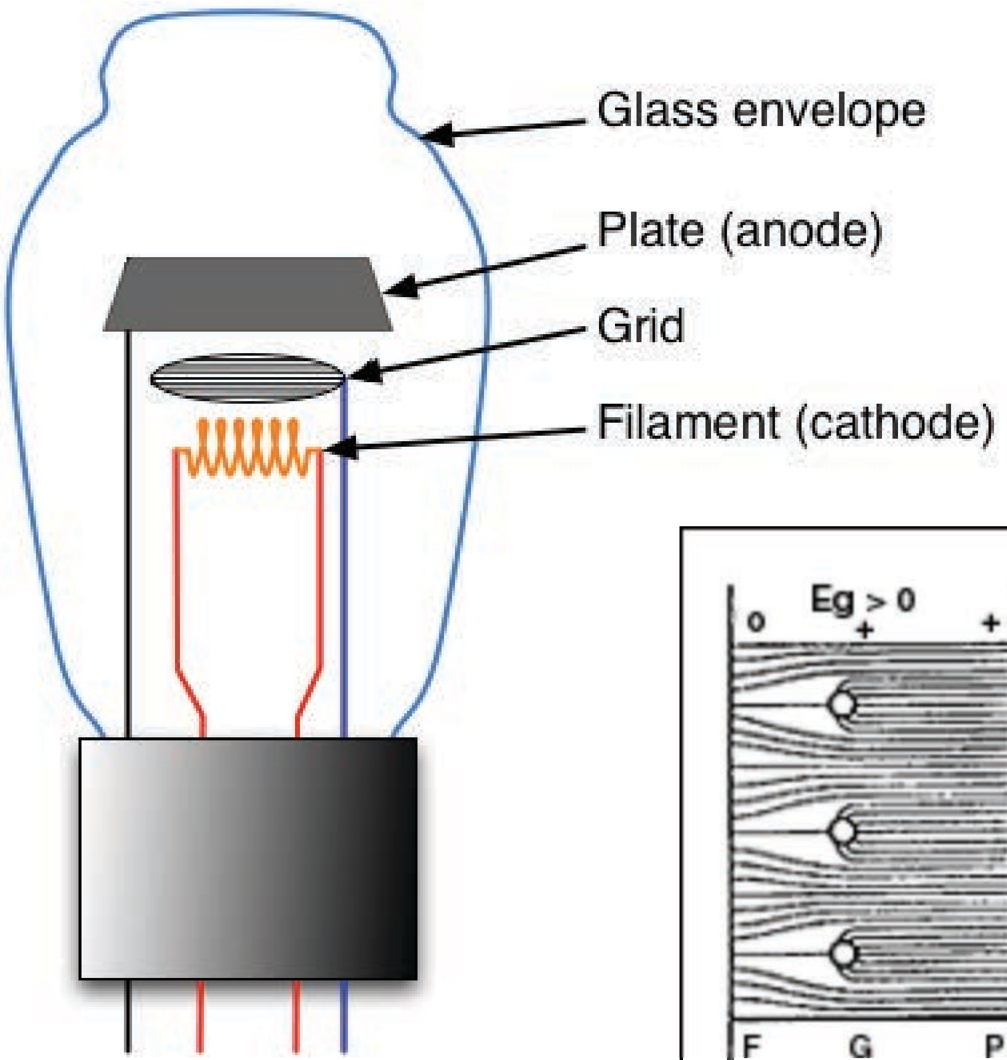
FAIRCHILD SEMICONDUCTOR™

2N3904 **MMBT3904** **PZT3904**

NPN General Purpose Amplifier

This device is designed as a general purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.

Triodo



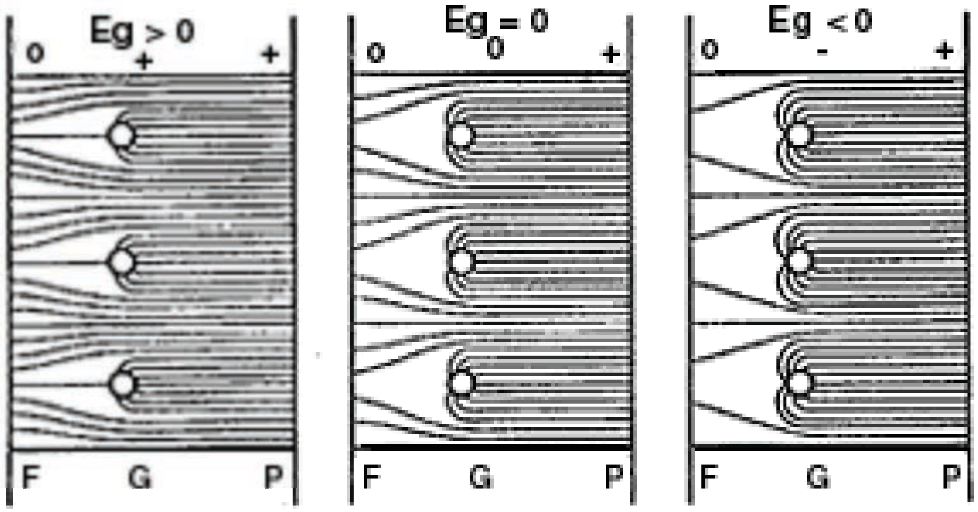
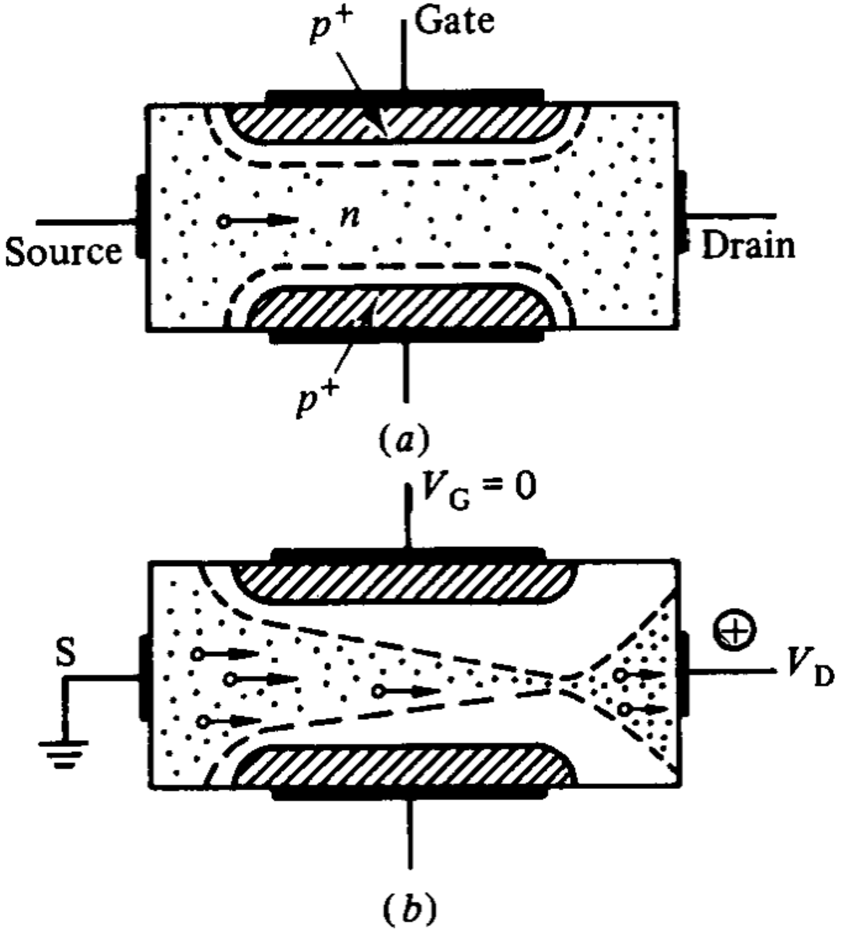
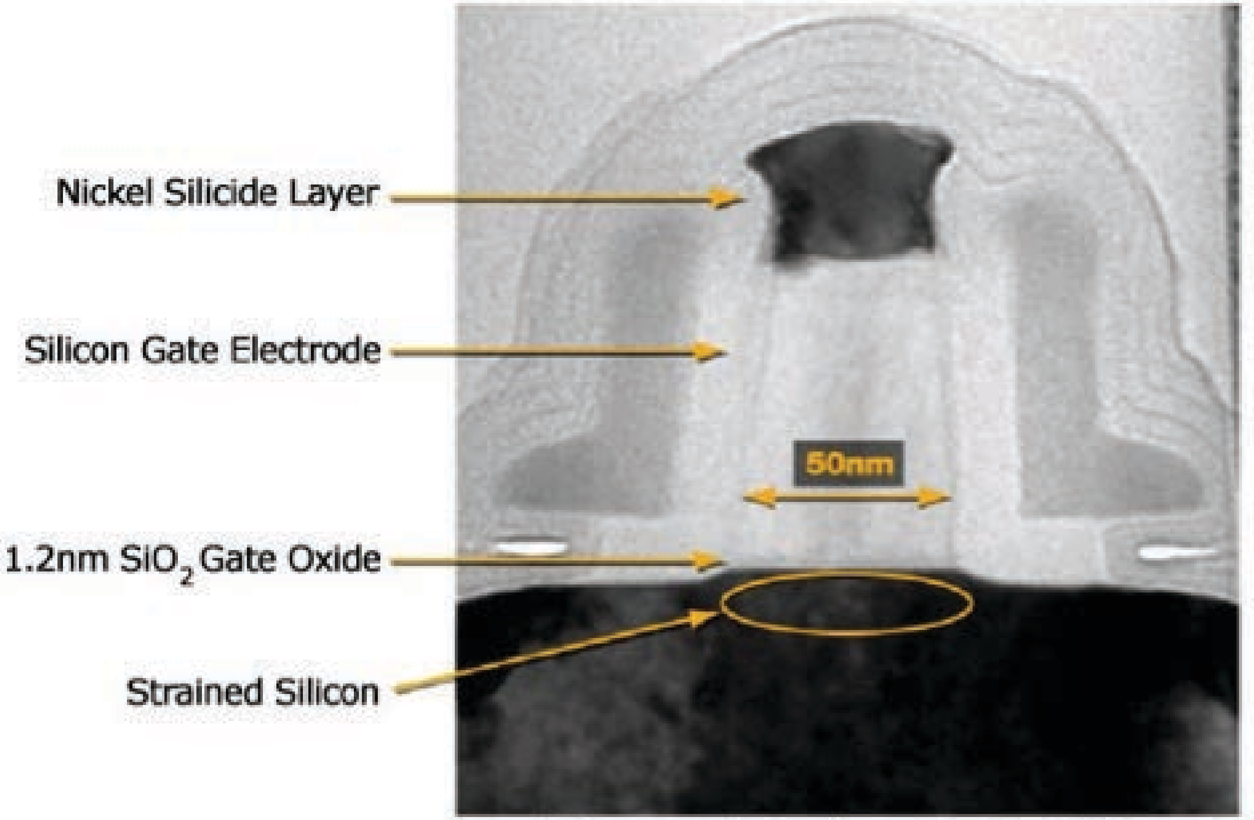


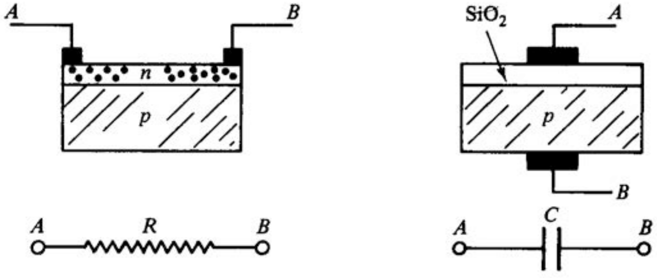
Figure 4 - Shows how changing the voltage on the grid of a triode controls the current through the tube.

I transistor a effetto di campo (FET)

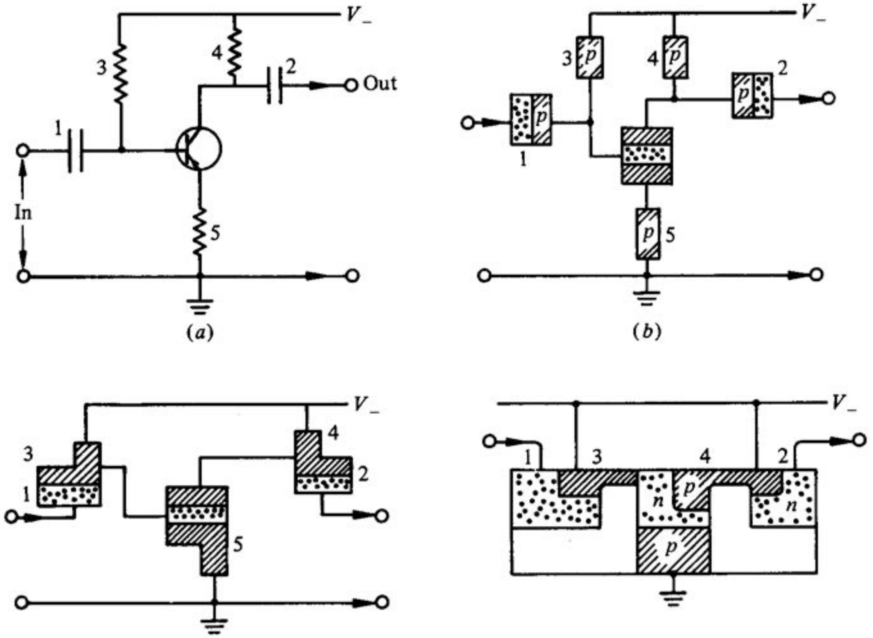




50nm transistor dimension is ~2000x smaller than diameter of human hair

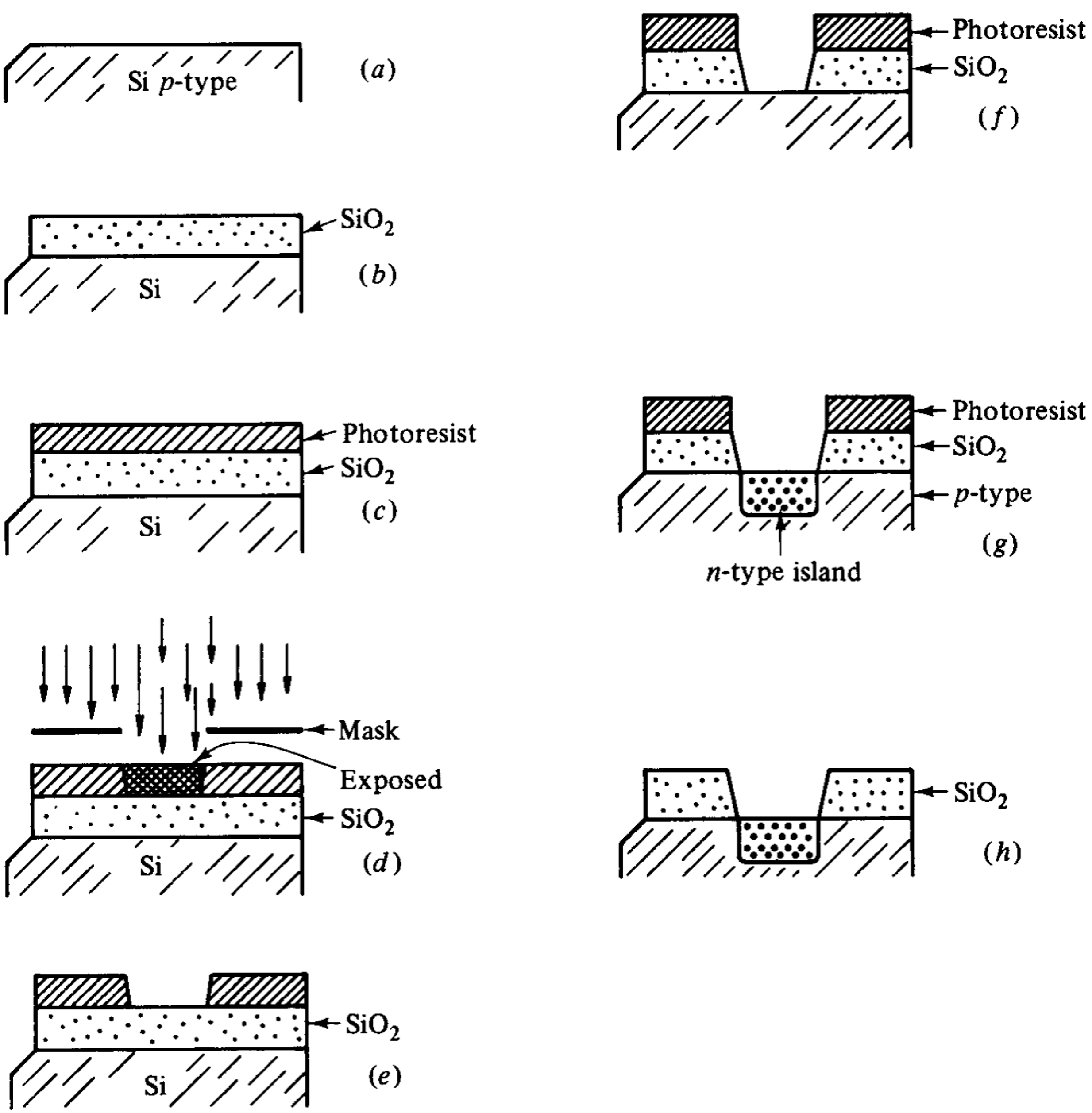

A
B
n
p
SiO$_2$
A
p
B
A
R
B
A
C
B

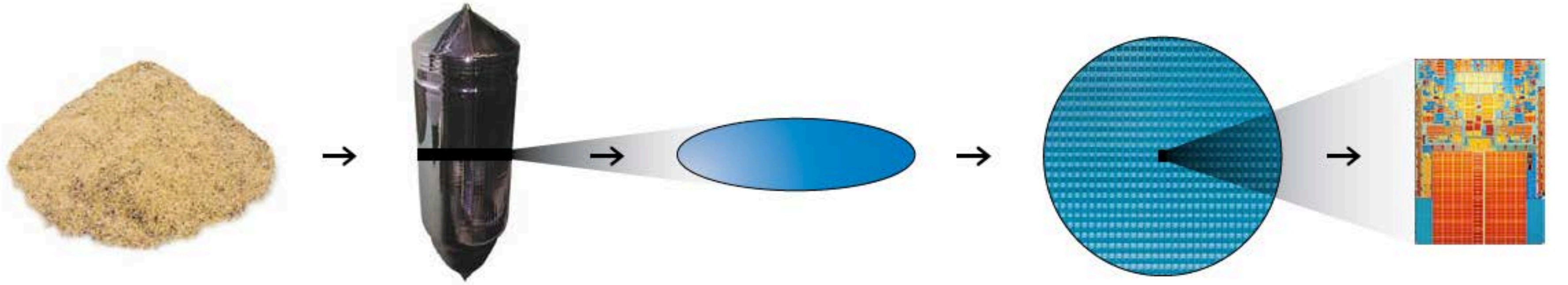
(a) (b)


V$_-$
3
4
2
Out
1
In
5
V$_-$
3
p
4
p
2
p
p
1
p
5
V$_-$
3
4
2
1
5
V$_-$
1
3
4
2
n
p
n
p

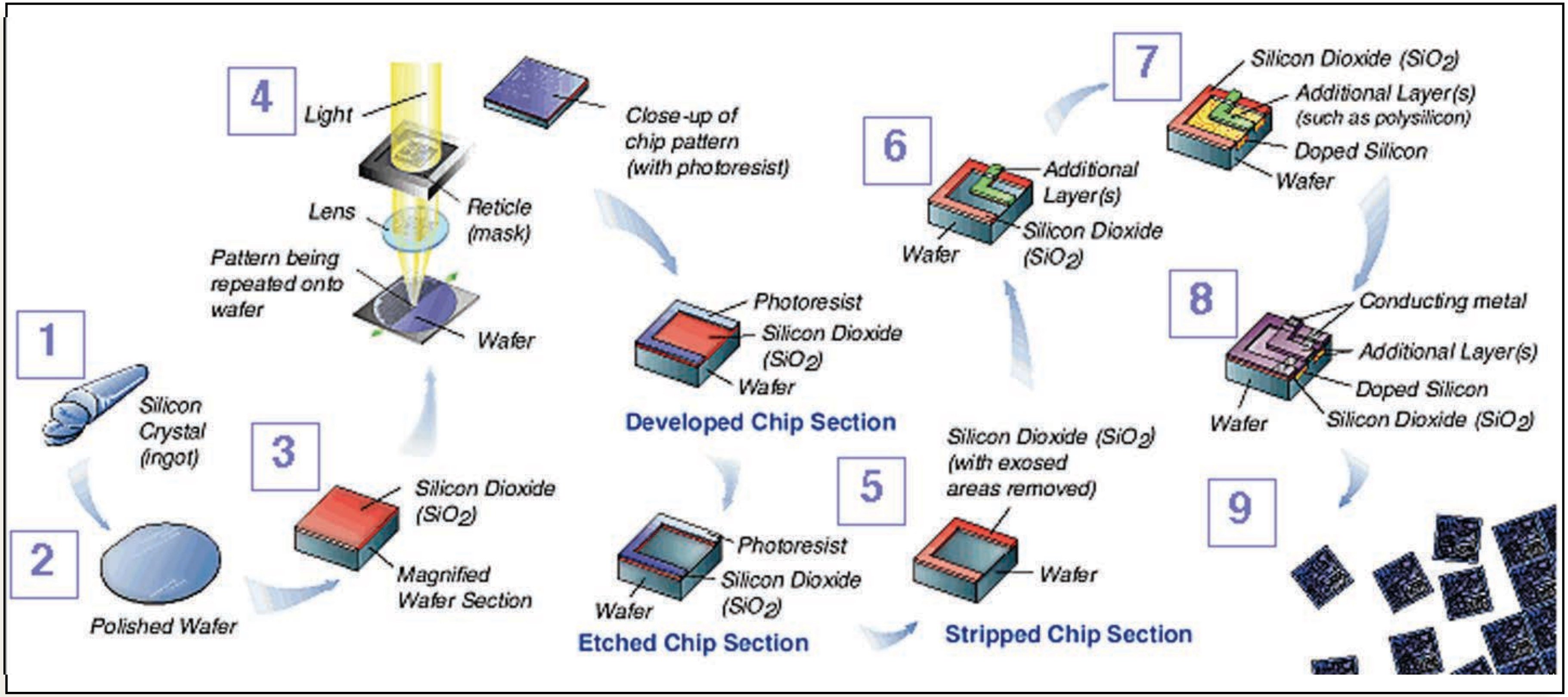
(a) (b)

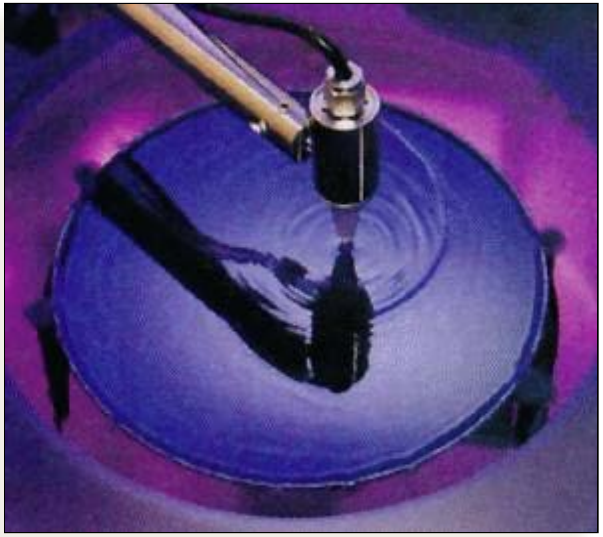
(c) (d)


Si p-type
(a)
SiO2
Si
(b)
Photoresist
SiO2
Si
(c)
Mask
Exposed
SiO2
Si
(d)
SiO2
Si
(e)
Photoresist
SiO2
(f)
Photoresist
SiO2
p-type
n-type island
(g)
SiO2
(h)

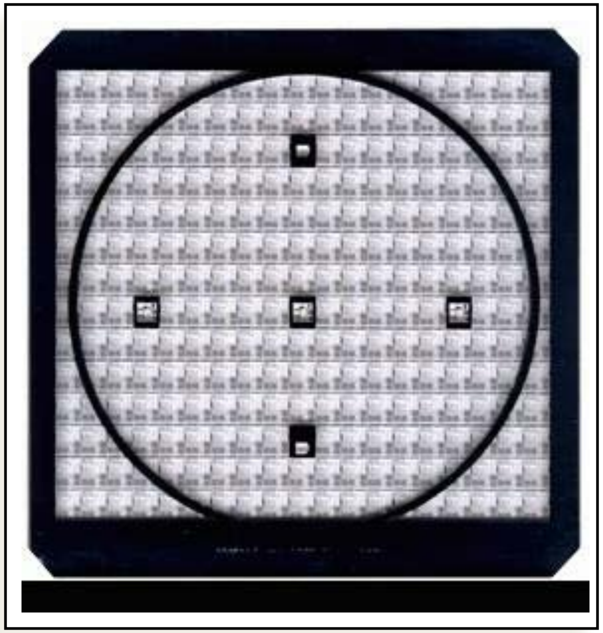


Sand → Purified silicon ingot → Wafer sliced from ingot and polished → Processed wafer → Completed die from finished wafer

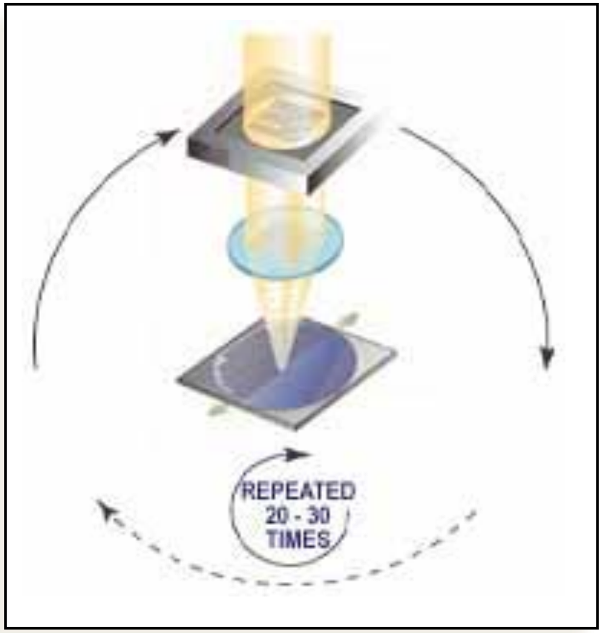




Il fotoresist viene depositato sul wafer



La maschera da proiettare

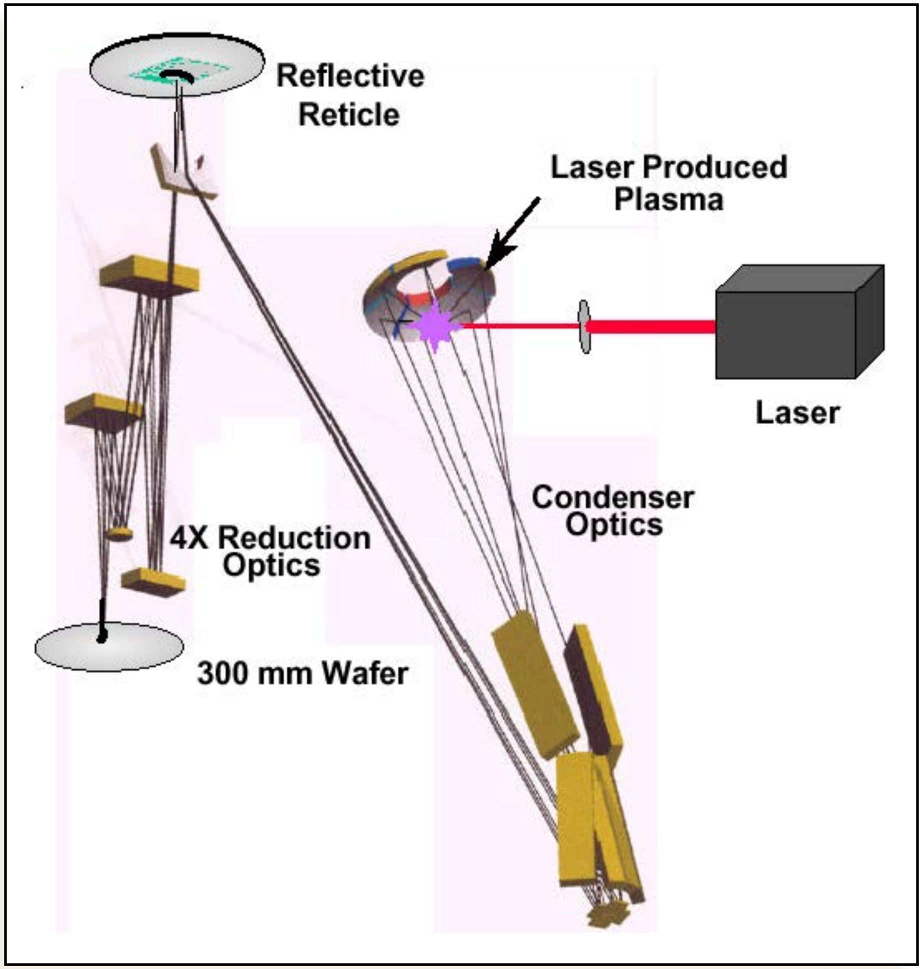


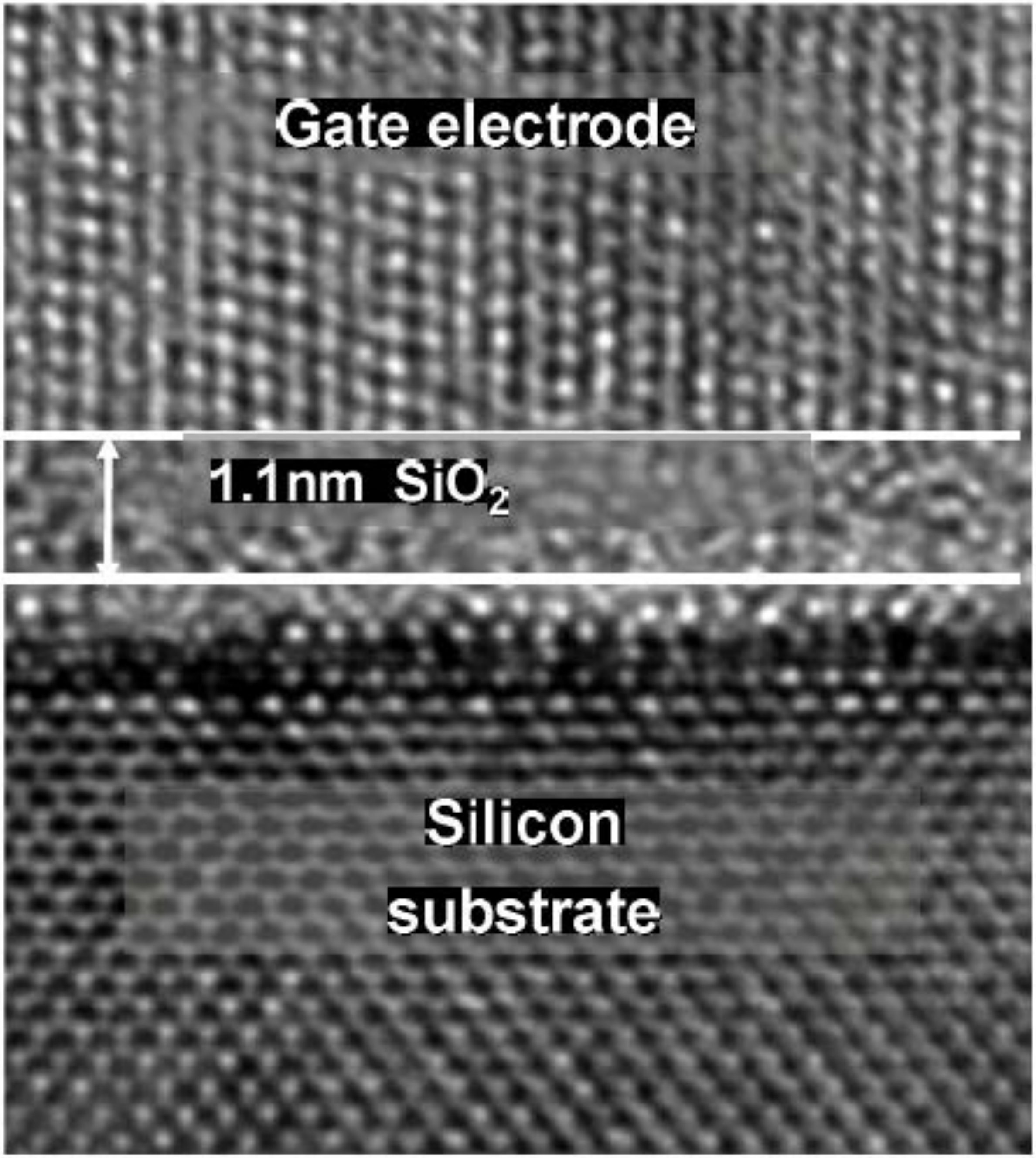
Proiezione della maschera

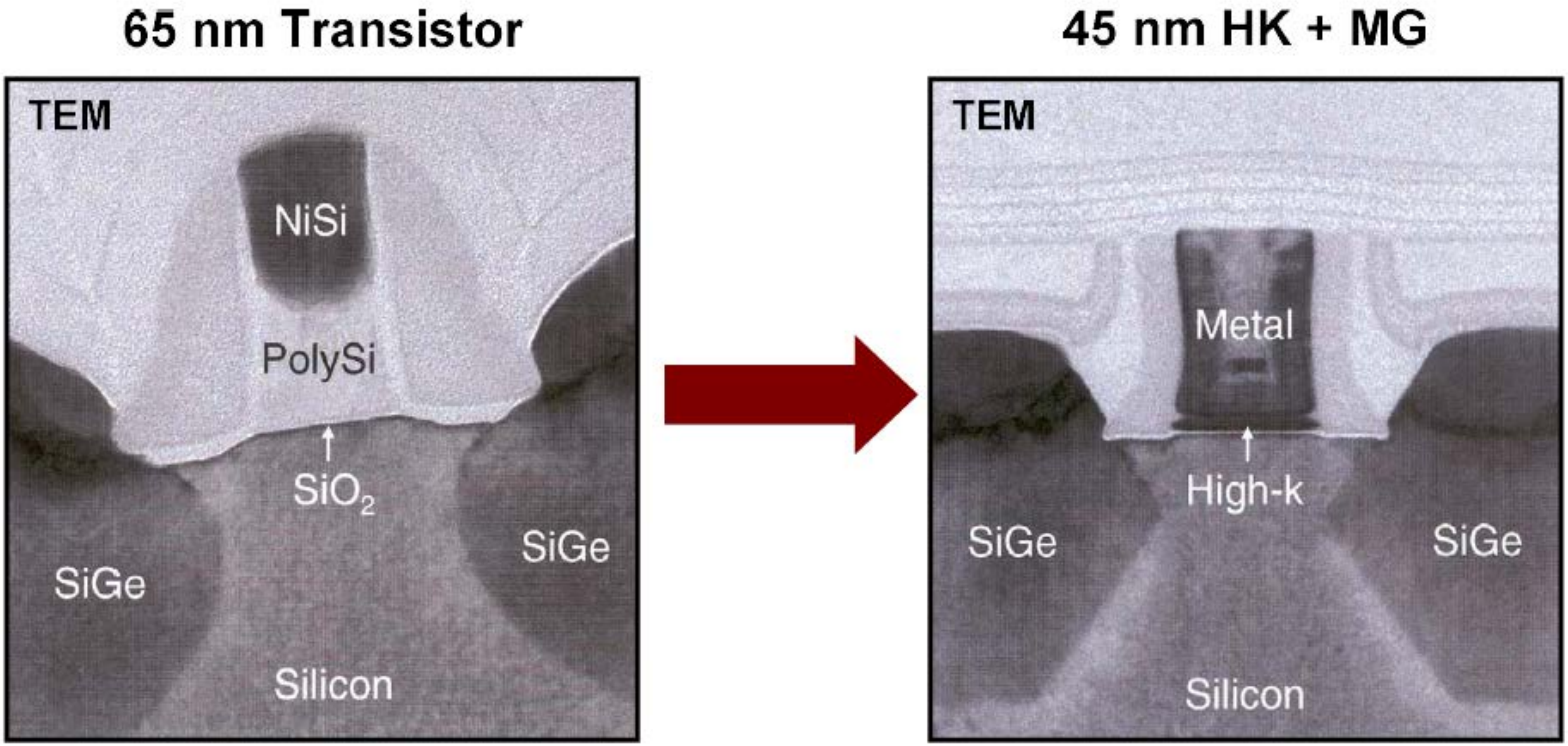
Litografia ad alta risoluzione

richiede l'uso di sorgenti ultraviolette a piccola lunghezza d'onda (< 200 nm)

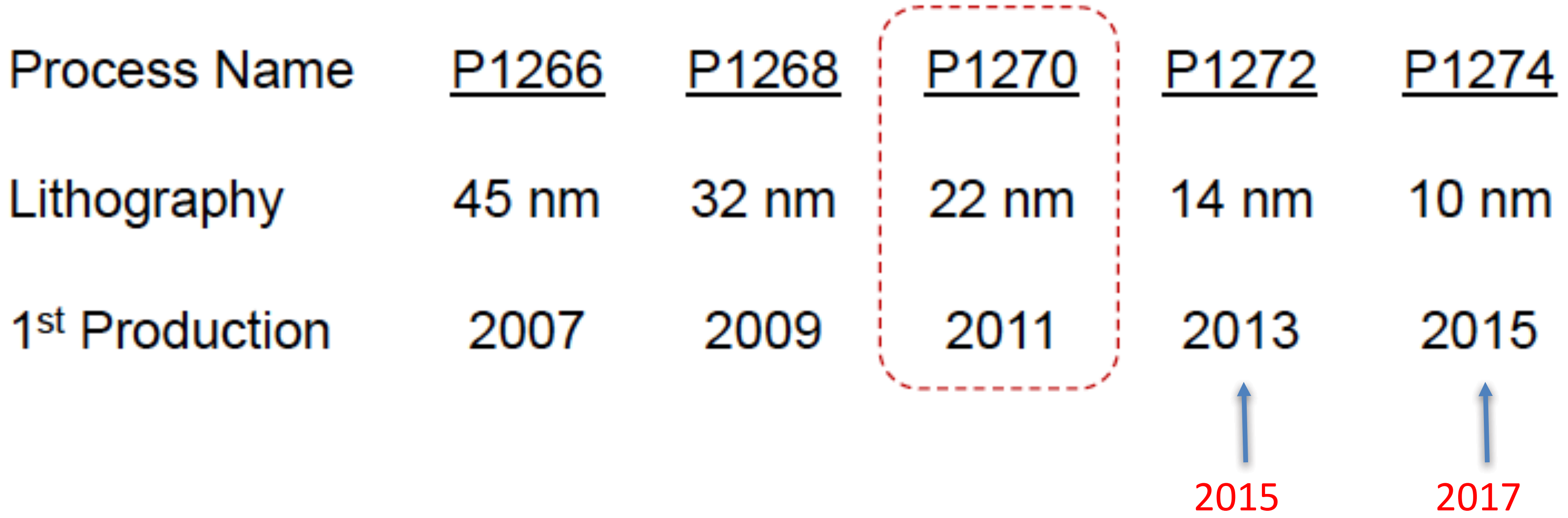
- laser ad eccimeri oppure lampada a plasma
- focalizzazione per mezzo di elementi ottici riflettenti asferici
- nel caso di radiazione EUV (11-13 nm) gli specchi devono essere lavorati con una tolleranza di ~0.1 nm



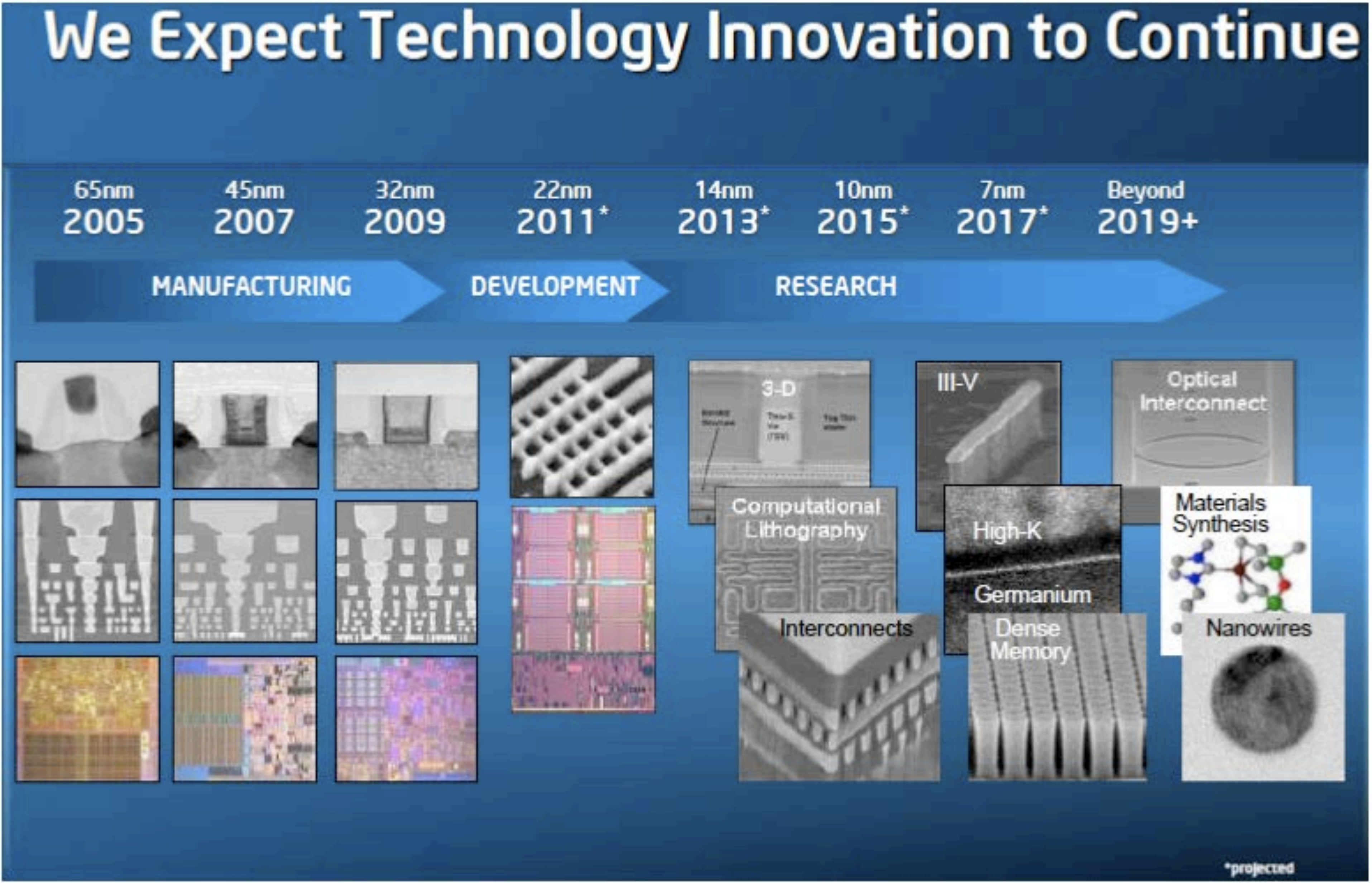

Gate electrode
1.1nm SiO_2
Silicon
substrate


65 nm Transistor
TEM
NiSi
PolySi
SiO_2
SiGe
SiGe
Silicon
45 nm HK + MG
TEM
Metal
High-k
SiGe
SiGe
Silicon

Intel Technology Roadmap



Process Name	P1266	P1268	P1270	P1272	P1274
Lithography	45 nm	32 nm	22 nm	14 nm	10 nm
1st Production	2007	2009	2011	2013	2015
				2015	2017

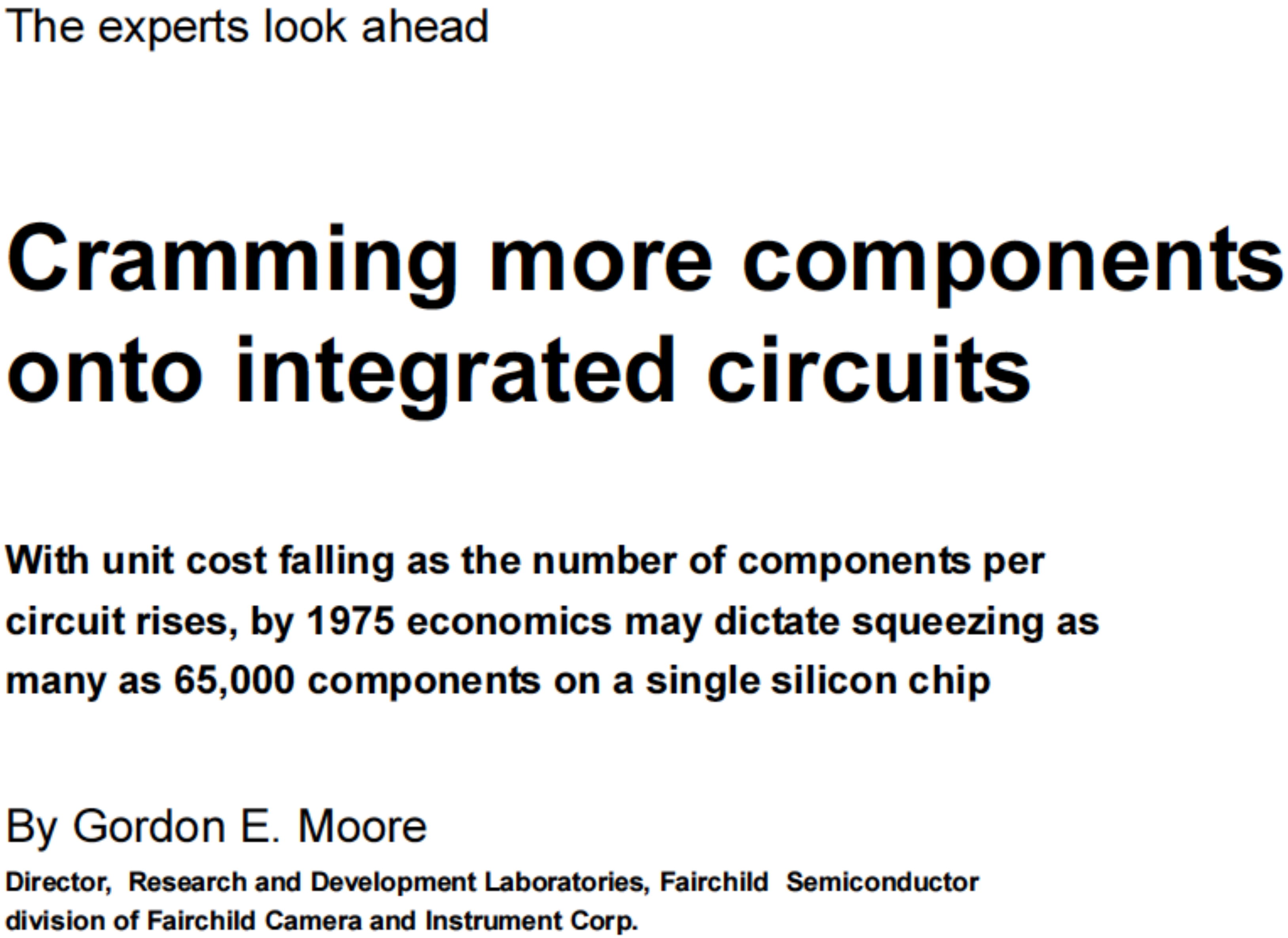


We Expect Technology Innovation to Continue

65nm	45nm	32nm	22nm	14nm	10nm	7nm	Beyond
2005	2007	2009	2011*	2013*	2015*	2017*	2019+

MANUFACTURING → DEVELOPMENT → RESEARCH

*projected



The experts look ahead

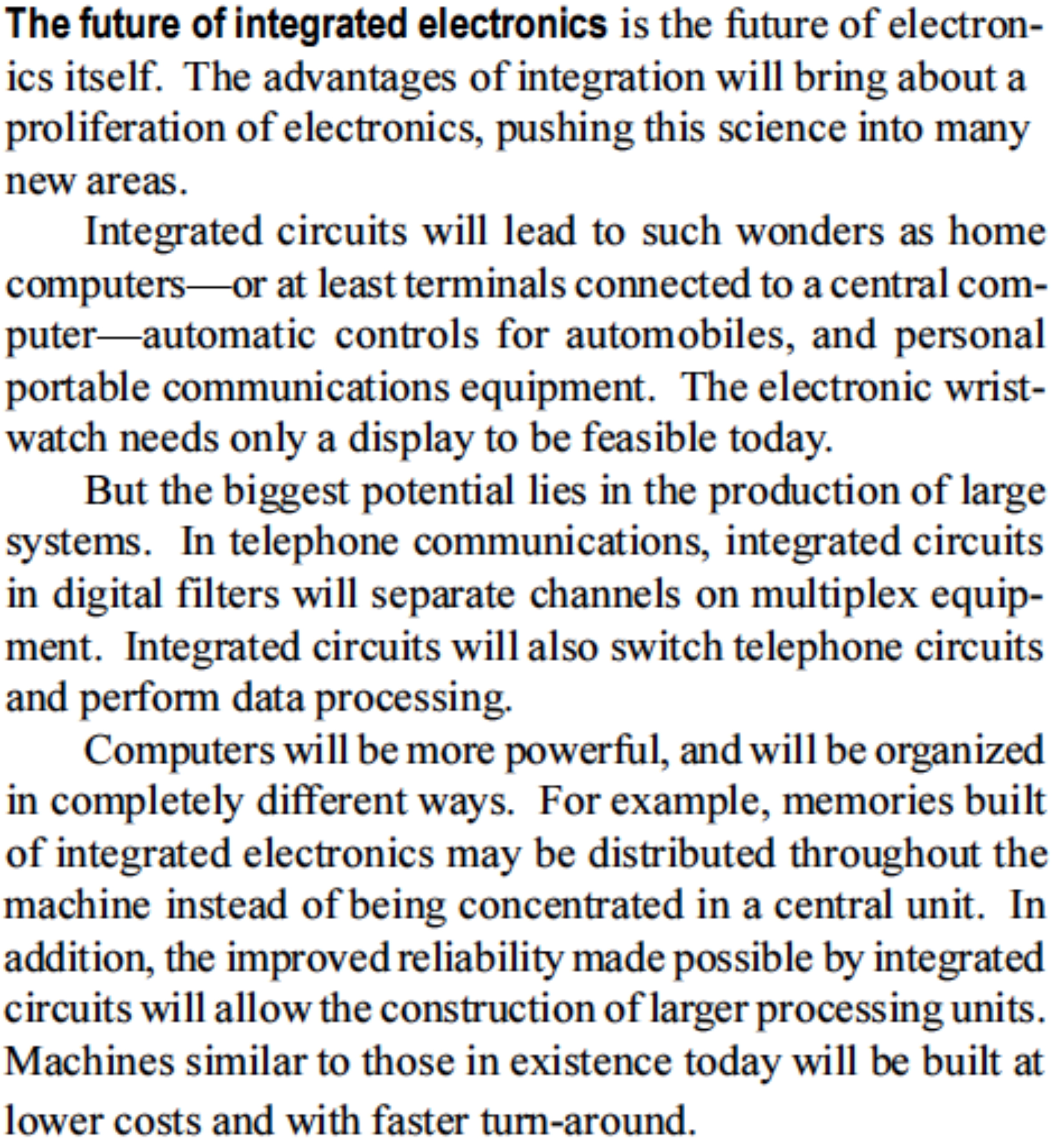
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965

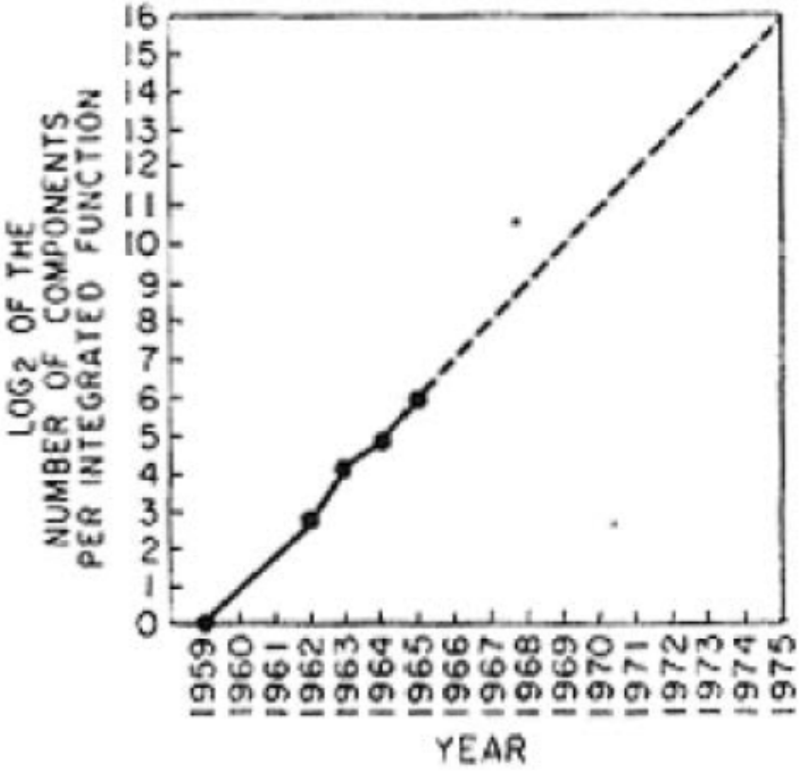


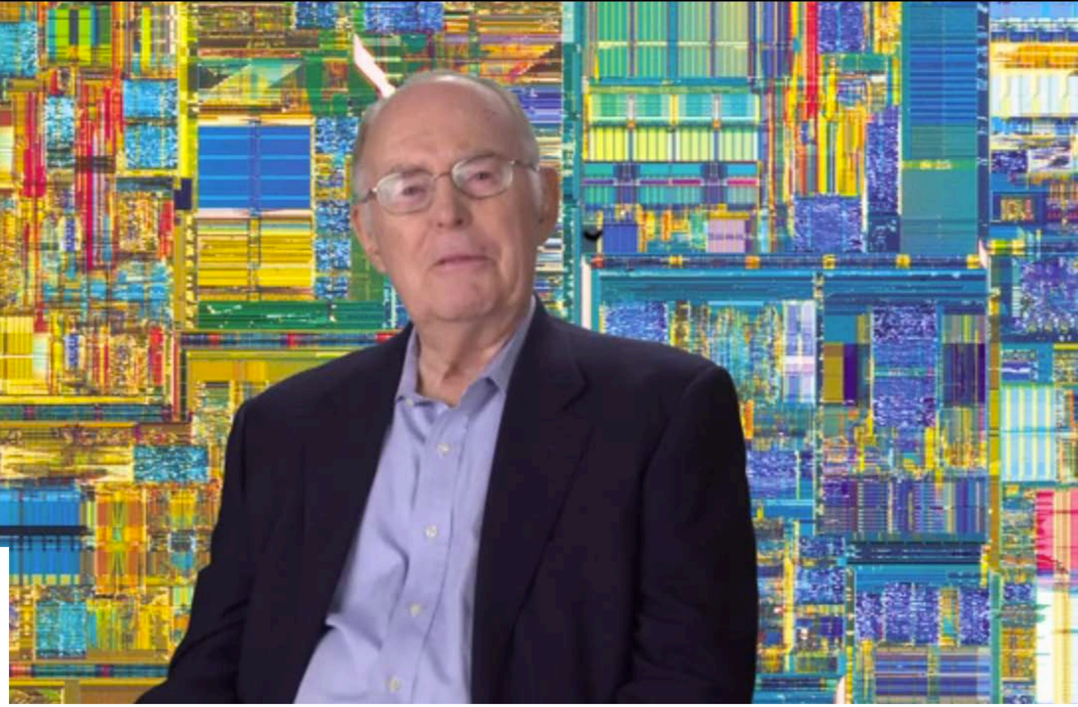
The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.





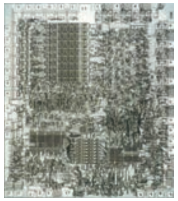
Gordon Moore

Intel Chips

Decades of Intel chips, including the 22nm 3rd generation Intel® Core™ processor with its revolutionary 3-D Tri-Gate transistors, illustrate Intel's unwavering commitment to delivering technology and manufacturing leadership to the devices you use every day. As you advance through the chart, the benefits of Moore's Law, which states that the number of transistors roughly doubles every couple of years, are evident as Intel increases transistor density and innovates the architecture designs that deliver more complex, powerful, and energy-efficient chips that transform the way we work, live, and play.


1


2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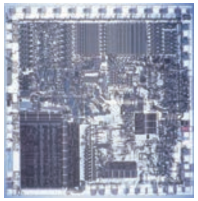
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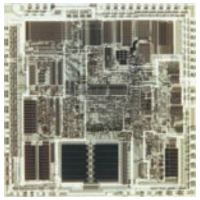
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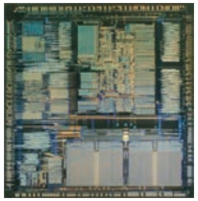
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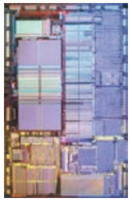
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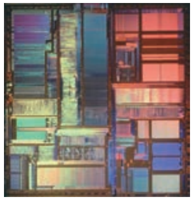
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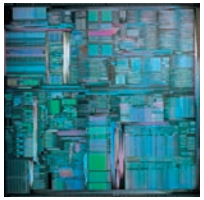
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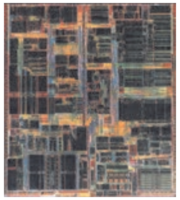
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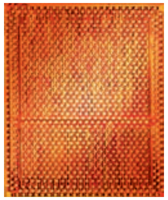
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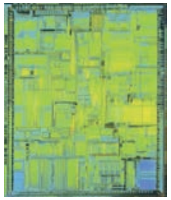
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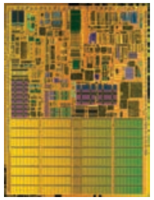
13


14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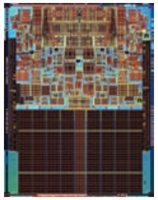
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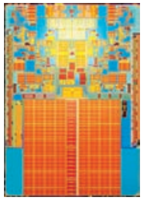
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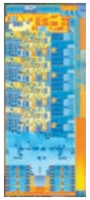
18


19


20

1
1971
Intel® 4004 processor
Initial clock speed:
108KHz
Transistors:
2,300
Manufacturing technology:
10 micron

2
1972
Intel® 8008 processor
Initial clock speed:
800KHz
Transistors:
3,500
Manufacturing technology:
10 micron

3
1974
Intel® 8080 processor
Initial clock speed:
2MHz
Transistors:
4,500
Manufacturing technology:
6 micron

4
1978
Intel® 8086 processor
Initial clock speed:
5MHz
Transistors:
29,000
Manufacturing technology:
3 micron

5
1982
Intel® 286™ processor
Initial clock speed:
6MHz
Transistors:
134,000
Manufacturing technology:
1.5 micron

6
1985
Intel386™ processor
Initial clock speed:
16MHz
Transistors:
275,000
Manufacturing technology:
1.5 micron

7
1989
Intel486™ processor
Initial clock speed:
25MHz
Transistors:
1.2 million
Manufacturing technology:
1 micron

8
1993
Intel® Pentium® processor
Initial clock speed:
66MHz
Transistors:
3.1 million
Manufacturing technology:
0.8 micron

9
1995
Intel® Pentium® Pro processor
Initial clock speed:
200MHz
Transistors:
5.5 million
Manufacturing technology:
0.35 micron

10
1997
Intel® Pentium® II processor
Initial clock speed:
300MHz
Transistors:
7.5 million
Manufacturing technology:
0.25 micron

10
1997
Intel® Pentium® II processor
Initial clock speed:
300MHz
Transistors:
7.5 million
Manufacturing technology:
0.25 micron

11
1998
Intel® Celeron® processor
Initial clock speed:
266MHz
Transistors:
7.5 million
Manufacturing technology:
0.25 micron

12
1999
Intel® Pentium® III processor
Initial clock speed:
600MHz
Transistors:
9.5 million
Manufacturing technology:
0.25 micron

13
2000
Intel® Pentium® 4 processor
Initial clock speed:
1.5GHz
Transistors:
42 million
Manufacturing technology:
0.18 micron

14
2001
Intel® Xeon® processor
Initial clock speed:
1.7GHz
Transistors:
42 million
Manufacturing technology:
0.18 micron

15
2003
Intel® Pentium® M processor
Initial clock speed:
1.7GHz
Transistors:
55 million
Manufacturing technology:
90nm

16
2006
Intel® Core™2 Duo processor
Initial clock speed::
2.66GHz
Transistors:
291 million
Manufacturing technology:
65nm

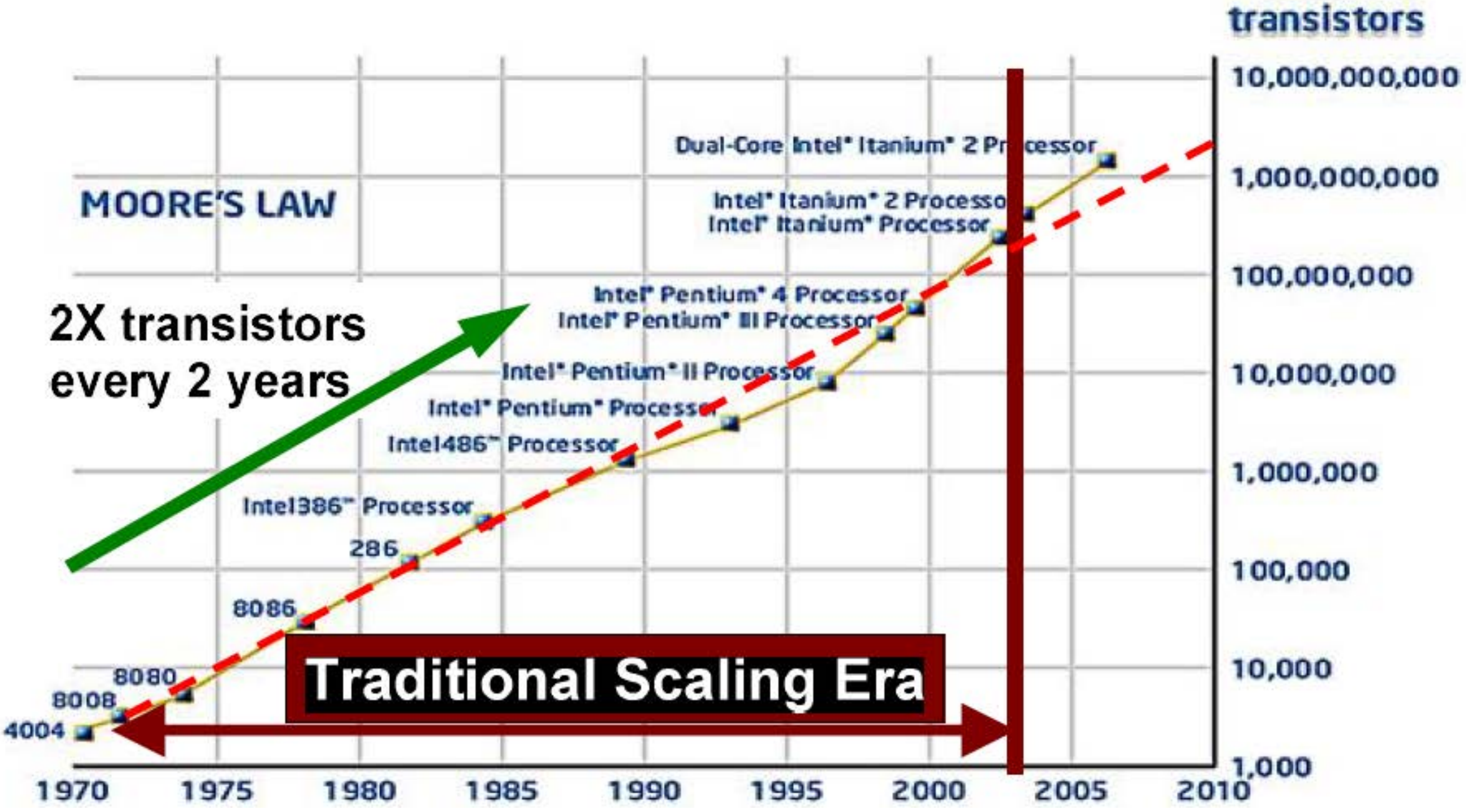
17
2008
Intel® Core™2 Duo processor
Initial clock speed:
2.4GHz
Transistors:
410 million
Manufacturing technology:
45nm

18
2008
Intel® Atom™ processor
Initial clock speed:
1.86GHz
Transistors:
47 million
Manufacturing technology:
45nm

19
2010
2nd generation Intel® Core™ processor
Initial clock speed:
3.8GHz
Transistors:
1.16 billion
Manufacturing technology:
32nm

20
2012
3rd generation Intel® Core™ processor
Initial clock speed:
2.9GHz
Transistors:
1.4 billion
Manufacturing technology:
22nm

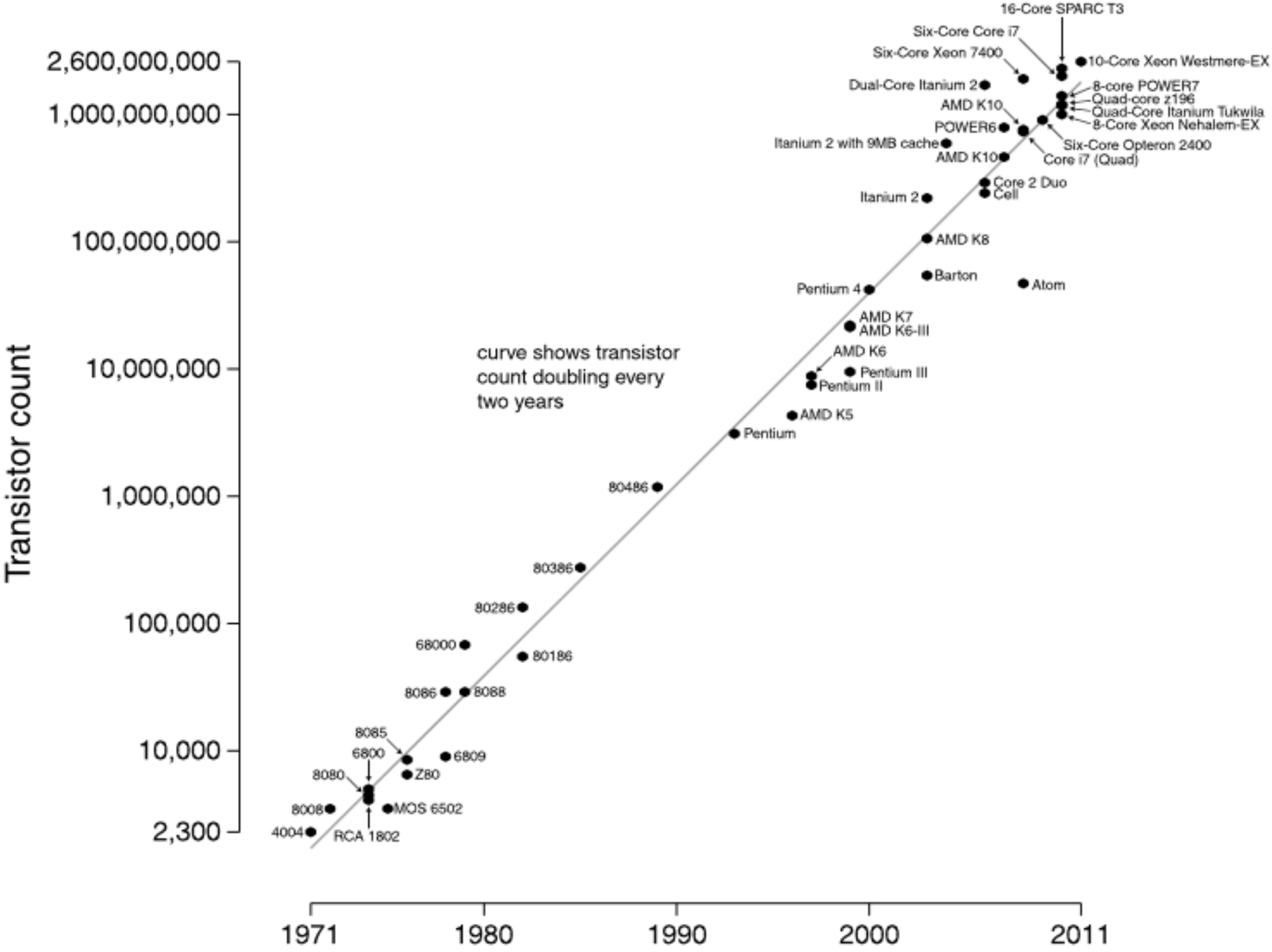
40+ Years of Moore's Law at INTEL: From Few to Billions of Transistors



2X transistors every 2 years

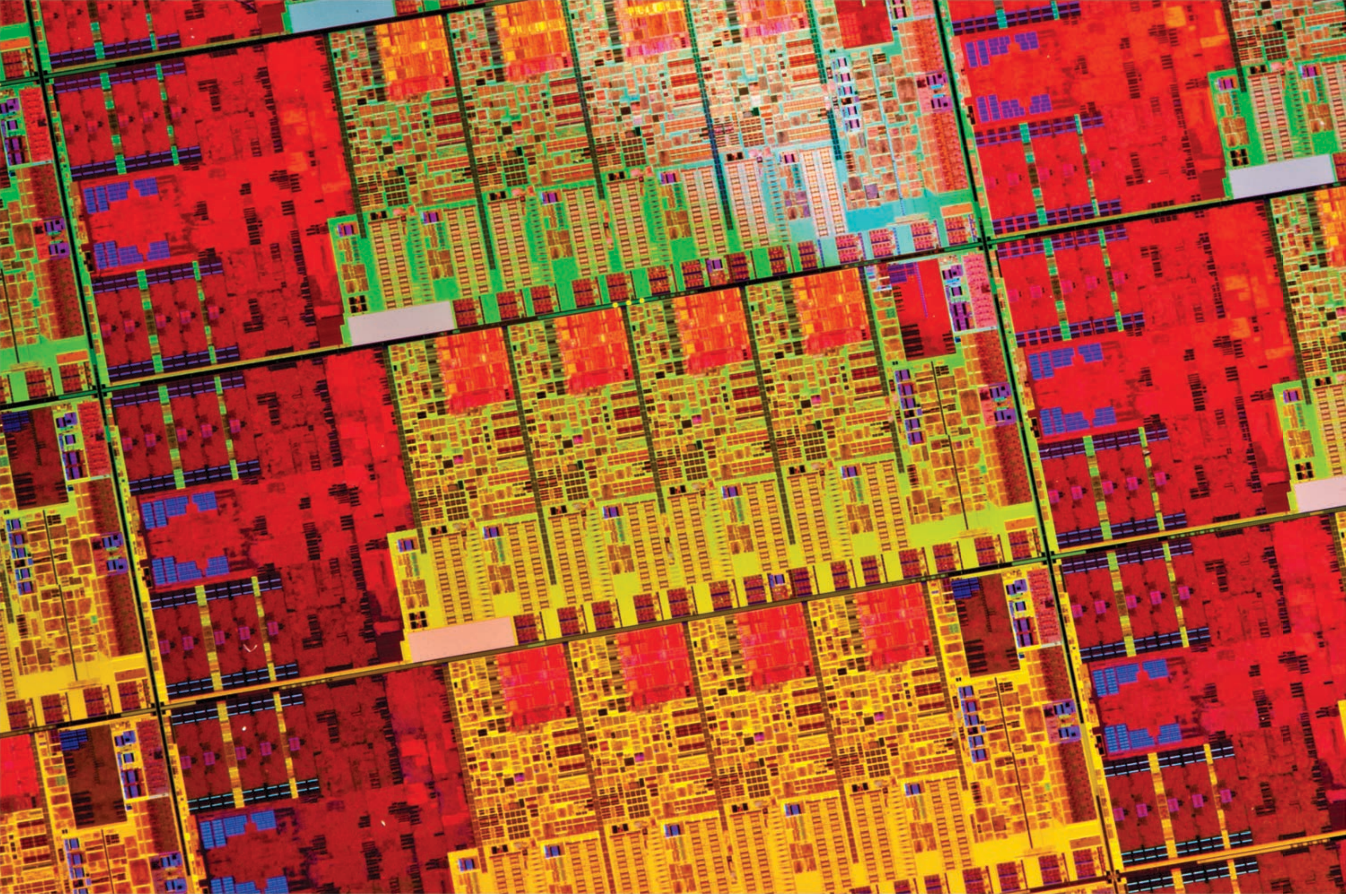
Traditional Scaling Era

Microprocessor Transistor Counts 1971-2011 & Moore's Law

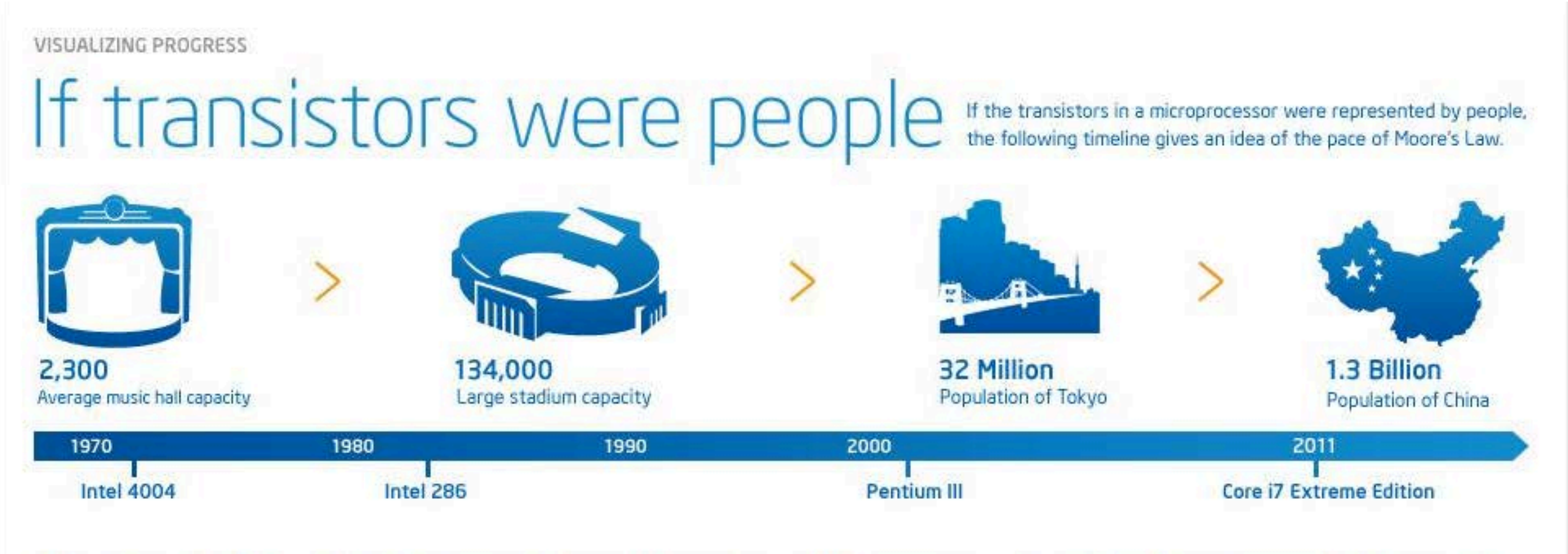


Six-core Xeon 7400	1,900,000,000	2008	Intel	45 nm	503 mm²
Quad-core Itanium Tukwila	2,000,000,000[25]	2010	Intel	65 nm	699 mm²
Apple A8 (dual-core ARM64 "mobile SoC")	2,000,000,000	2014	Apple	20 nm	89 mm²
8-core POWER7+ 80 MB L3 cache	2,100,000,000	2012	IBM	32 nm	567 mm²
Six-core Core i7/8-core Xeon E5 (Sandy Bridge-E/EP)	2,270,000,000[26]	2011	Intel	32 nm	434 mm²
8-core Xeon Nehalem-EX	2,300,000,000[27]	2010	Intel	45 nm	684 mm²
8-core Core i7 Haswell-E	2,600,000,000[28]	2014	Intel	22 nm	355 mm²
10-core Xeon Westmere-EX	2,600,000,000	2011	Intel	32 nm	512 mm²
Six-core zEC12	2,750,000,000	2012	IBM	32 nm	597 mm²
Apple A8X (tri-core ARM64 "mobile SoC")	3,000,000,000[29]	2014	Apple	20 nm	128 mm²
8-core Itanium Poulson	3,100,000,000	2012	Intel	32 nm	544 mm²
IBM z13	3,990,000,000	2015	IBM	22 nm	678 mm²
12-core POWER8	4,200,000,000	2013	IBM	22 nm	650 mm²
15-core Xeon Ivy Bridge-EX	4,310,000,000[30]	2014	Intel	22 nm	541 mm²
61-core Xeon Phi	5,000,000,000[31]	2012	Intel	22 nm	350 mm²
Xbox One main SoC	5,000,000,000	2013	Microsoft/AMD	28 nm	363 mm²
18-core Xeon Haswell-E5	5,560,000,000[32]	2014	Intel	22 nm	661 mm²
IBM z13 Storage Controller	7,100,000,000	2015	IBM	22 nm	678 mm²

RV790	959,000,000[33]	2008	AMD	55 nm	282 mm²
GT200 Tesla	1,400,000,000[34]	2008	NVIDIA	65 nm	576 mm²
Cypress RV870	2,154,000,000[35]	2009	AMD	40 nm	334 mm²
Cayman RV970	2,640,000,000	2010	AMD	40 nm	389 mm²
GF100 Fermi	3,200,000,000[36]	Mar 2010	NVIDIA	40 nm	526 mm²
GF110 Fermi	3,000,000,000[36]	Nov 2010	NVIDIA	40 nm	520 mm²
GK104 Kepler	3,540,000,000[37]	2012	NVIDIA	28 nm	294 mm²
Tahiti	4,312,711,873[38]	2011	AMD	28 nm	365 mm²
GK110 Kepler	7,080,000,000[39]	2012[40]	NVIDIA	28 nm	561 mm²
Hawaii	6,300,000,000	2013	AMD	28 nm	438 mm²
GM204 Maxwell	5,200,000,000	2014	NVIDIA	28 nm	398 mm²
GM200 Maxwell	8,100,000,000	2015	NVIDIA	28 nm	601 mm²
Fiji	8,900,000,000	2015	AMD	28 nm	596 mm²



Microfotografia di una parte di un processore Haswell (Intel) realizzato con la tecnologia a 22 nm (2013).



VISUALIZING PROGRESS

If transistors were people

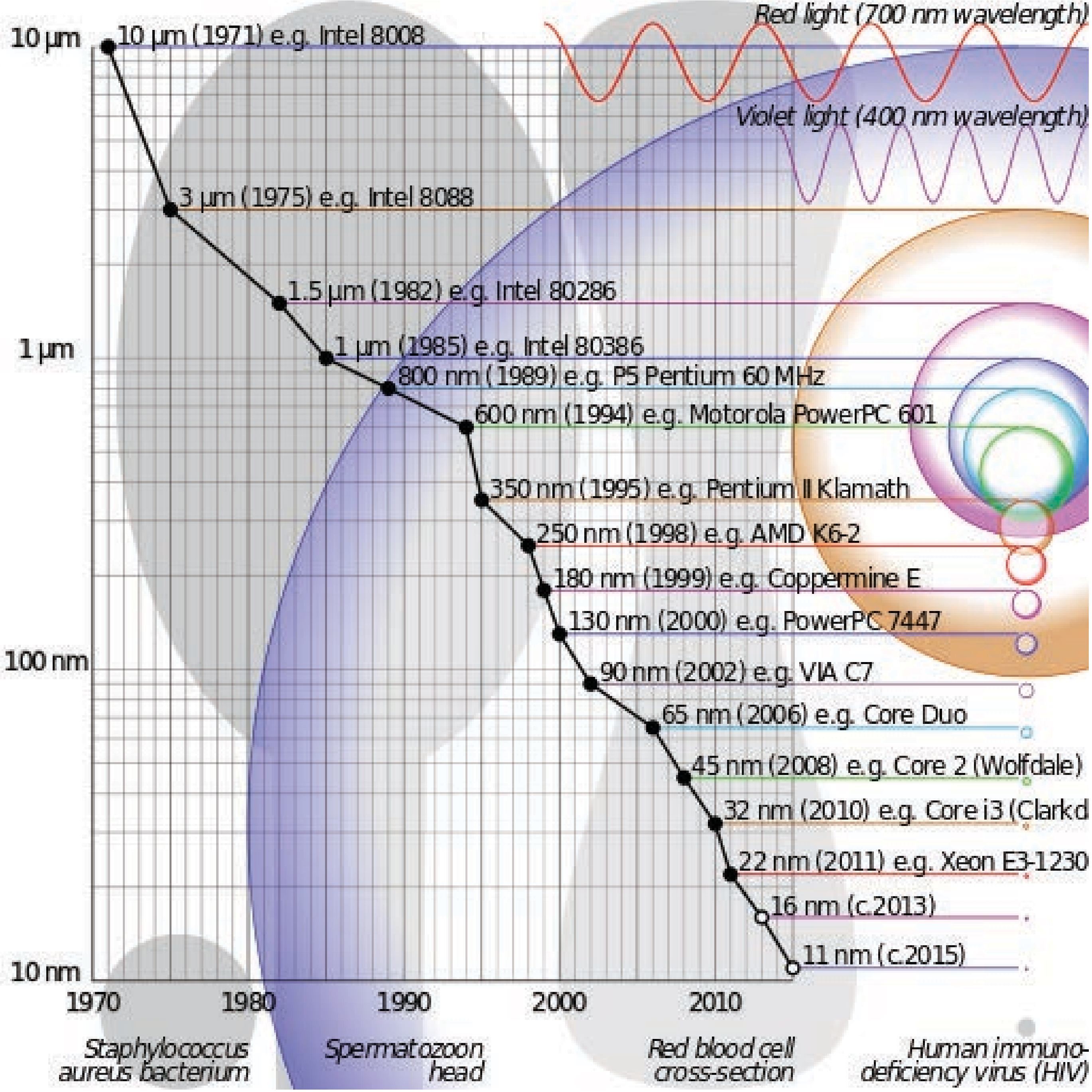
If the transistors in a microprocessor were represented by people, the following timeline gives an idea of the pace of Moore's Law.

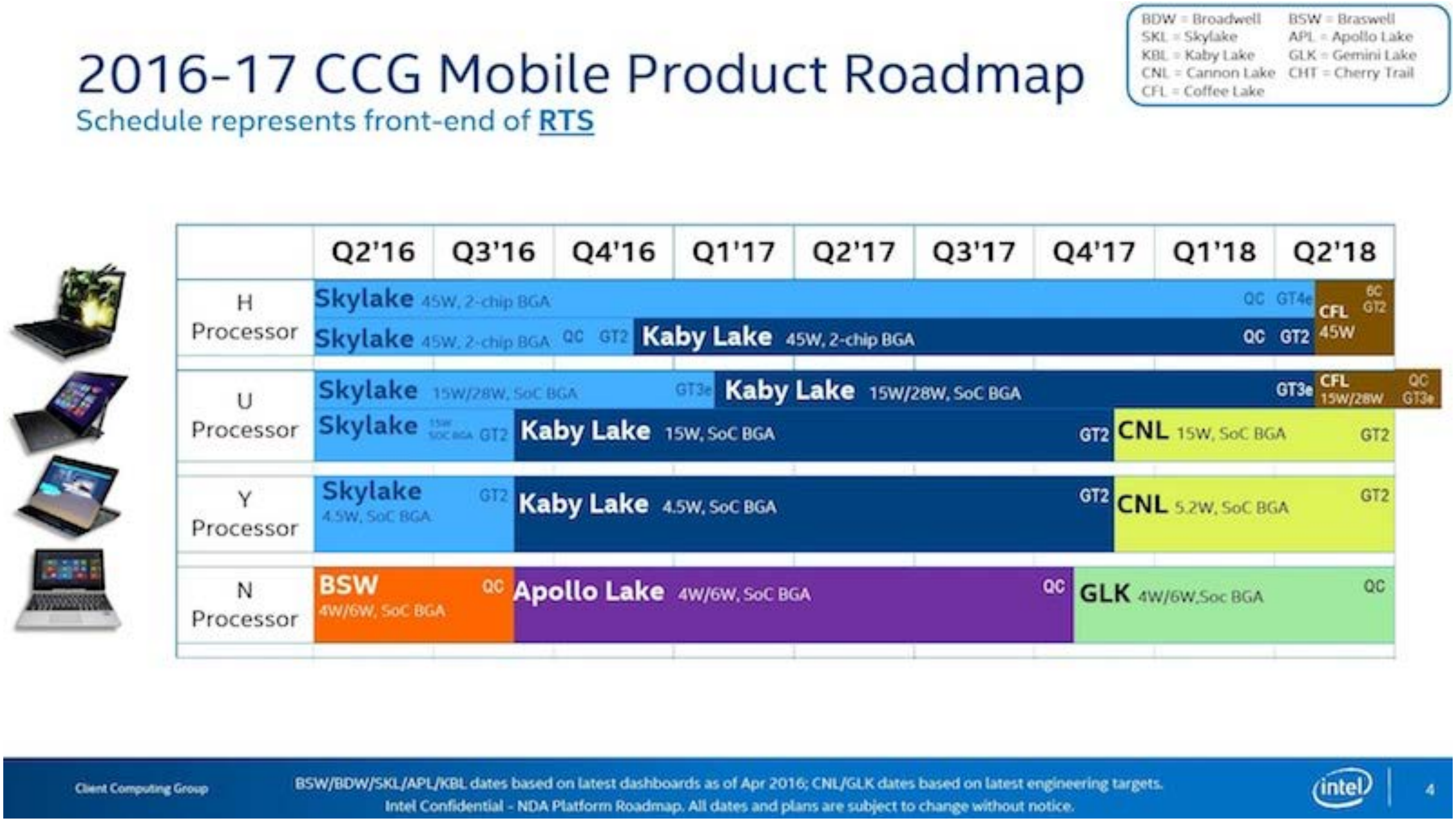
2,300
Average music hall capacity

134,000
Large stadium capacity

32 Million
Population of Tokyo

1.3 Billion
Population of China


Red light (700 nm wavelength)
Violet light (400 nm wavelength)
10 µm
1 µm
100 nm
10 nm
10 µm (1971) e.g. Intel 8008
3 µm (1975) e.g. Intel 8088
1.5 µm (1982) e.g. Intel 80286
1 µm (1985) e.g. Intel 80386
800 nm (1989) e.g. P5 Pentium 60 MHz
600 nm (1994) e.g. Motorola PowerPC 601
350 nm (1995) e.g. Pentium II Klamath
250 nm (1998) e.g. AMD K6-2
180 nm (1999) e.g. Coppermine E
130 nm (2000) e.g. PowerPC 7447
90 nm (2002) e.g. VIA C7
65 nm (2006) e.g. Core Duo
45 nm (2008) e.g. Core 2 (Wolfdale)
32 nm (2010) e.g. Core i3 (Clarkd
22 nm (2011) e.g. Xeon E3-1230
16 nm (c.2013)
11 nm (c.2015)
1970
1980
1990
2000
2010
Staphylococcus aureus bacterium
Spermatozoon head
Red blood cell cross-section
Human immuno-deficiency virus (HIV)



2016-17 CCG Mobile Product Roadmap

Schedule represents front-end of **RTS**

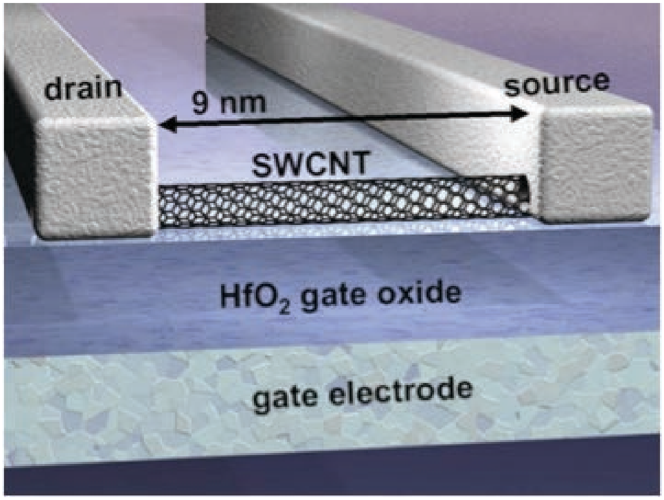
BDW = Broadwell
SKL = Skylake
KBL = Kaby Lake
CNL = Cannon Lake
CFL = Coffee Lake
BSW = Braswell
APL = Apollo Lake
GLK = Gemini Lake
CHT = Cherry Trail

	Q2'16	Q3'16	Q4'16	Q1'17	Q2'17	Q3'17	Q4'17	Q1'18	Q2'18
H Processor	**Skylake** 45W, 2-chip BGA							QC GT4e	**CFL** 6C GT2 45W
	Skylake 45W, 2-chip BGA		QC GT2 **Kaby Lake** 45W, 2-chip BGA					QC GT2	
U Processor	**Skylake** 15W/28W, SoC BGA			GT3e **Kaby Lake** 15W/28W, SoC BGA				GT3e	**CFL** 15W/28W QC GT3e
	Skylake 15W SoC BGA GT2	**Kaby Lake** 15W, SoC BGA					GT2 **CNL** 15W, SoC BGA		GT2
Y Processor	**Skylake** 4.5W, SoC BGA GT2	**Kaby Lake** 4.5W, SoC BGA					GT2 **CNL** 5.2W, SoC BGA		GT2
N Processor	**BSW** 4W/6W, SoC BGA QC	**Apollo Lake** 4W/6W, SoC BGA					QC **GLK** 4W/6W,Soc BGA		QC

Client Computing Group

BSW/BDW/SKL/APL/KBL dates based on latest dashboards as of Apr 2016; CNL/GLK dates based on latest engineering targets.
Intel Confidential - NDA Platform Roadmap. All dates and plans are subject to change without notice.

intel 4

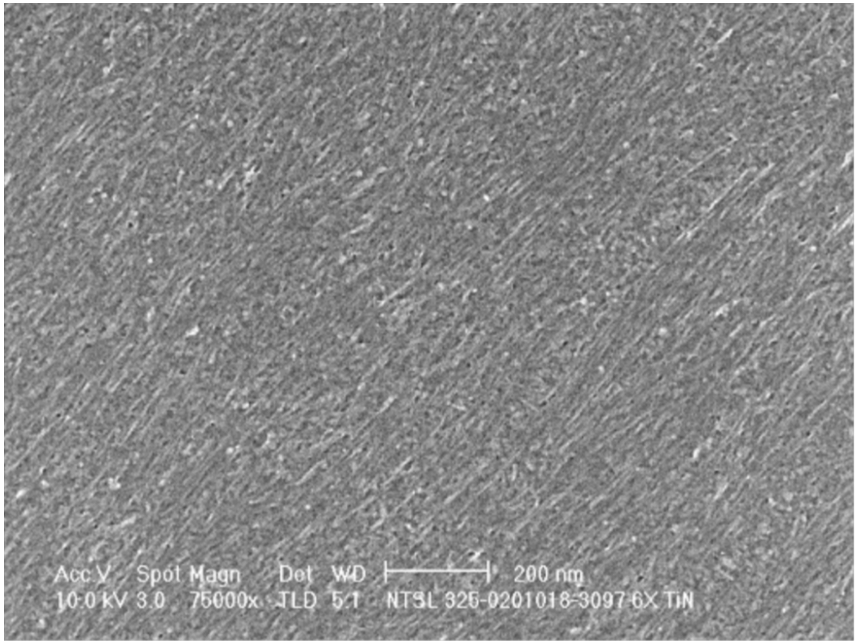


Quale futuro? Forse FET realizzati con nanotubi?

Press release dell'Univ. di Madison su recente ricerca che ha portato a nanotube transistors migliorati

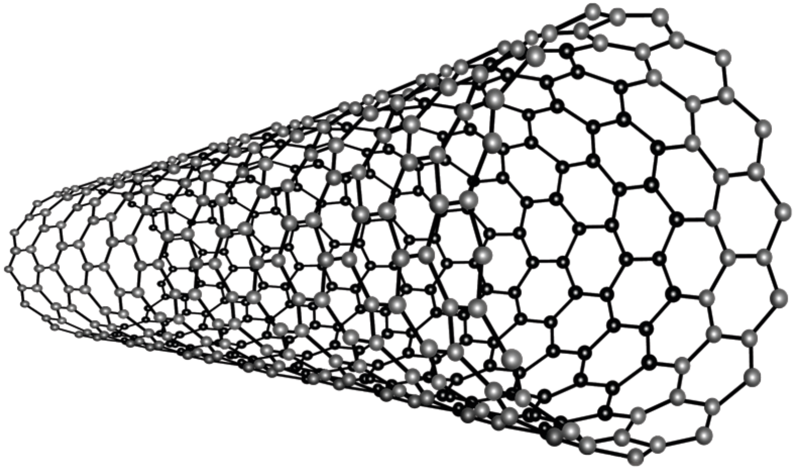
https://www.youtube.com/watch?v=BT9o_mO1GtY

Nanotube memory

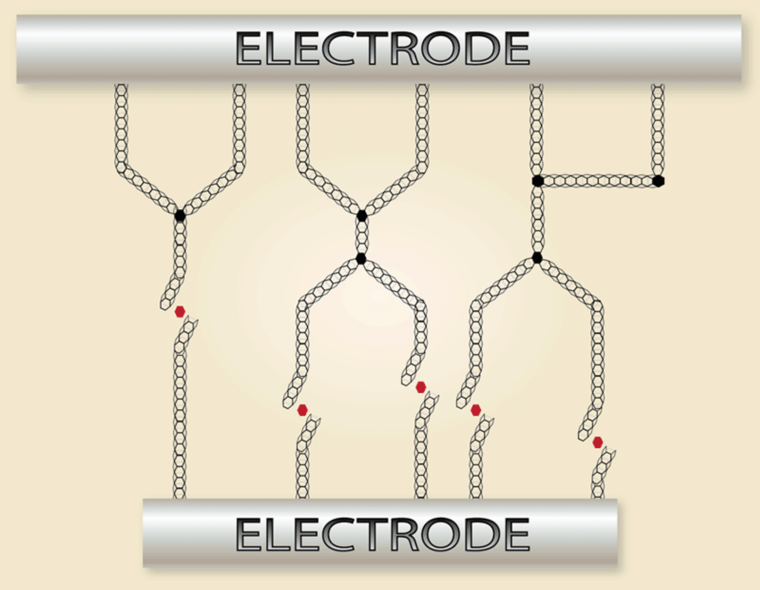


Nantero's NRAM is based on forming a film of CNTs that are deposited onto a standard silicon substrate that contains an underlying cell select device and array lines (typically transistors or diodes) that interface the NRAM switch.

The figure is a SEM image of the deposited film (or fabric) of crossed nanotubes that can be either touching or slightly separated depending on their position.



Carbon Nanotube used to create Nantero's NRAM®
50 times stronger than steel
1/50,000th the diameter of a human hair



Our limit to visibility goes out ~10 years

TECHNOLOGY GENERATION

45nm 2007

32nm 2009

22nm 2011

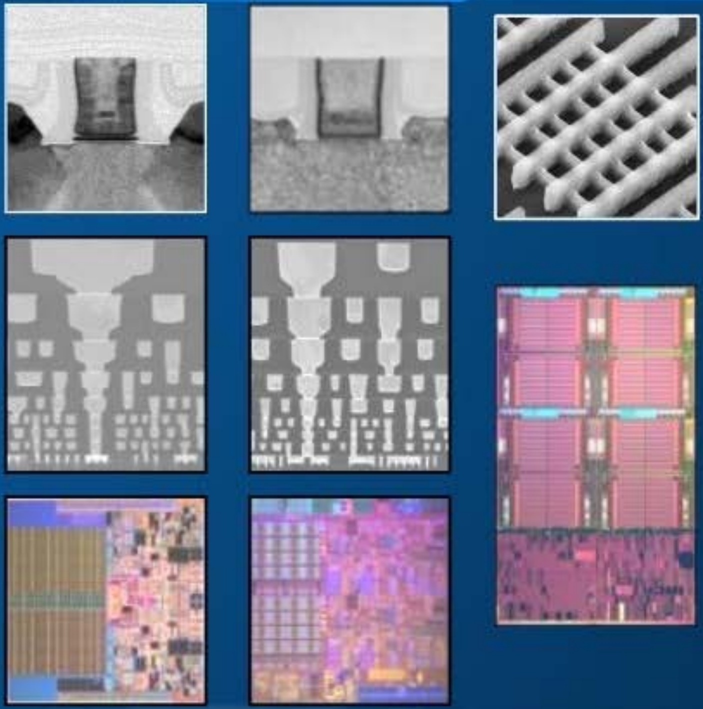
14nm ~~2013~~ 2014

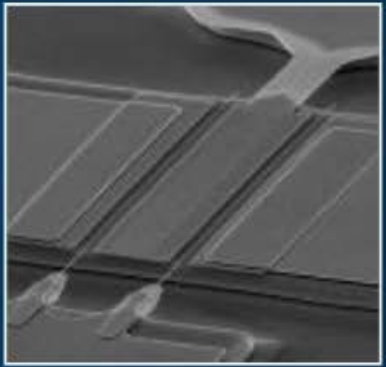
10nm ~~2015~~ 2017

7nm ~~2017~~ 2020

Beyond 2020

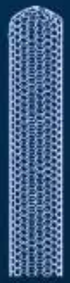
MANUFACTURING → DEVELOPMENT → RESEARCH



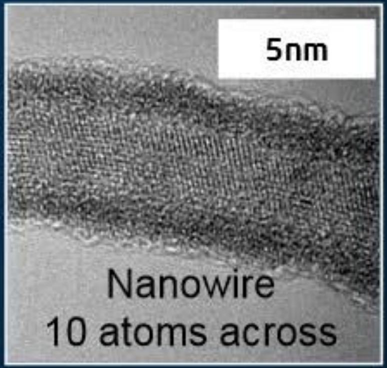


QW III-V Device

Carbon Nanotube
~1nm diameter



Graphene
1 atom thick



Not to scale