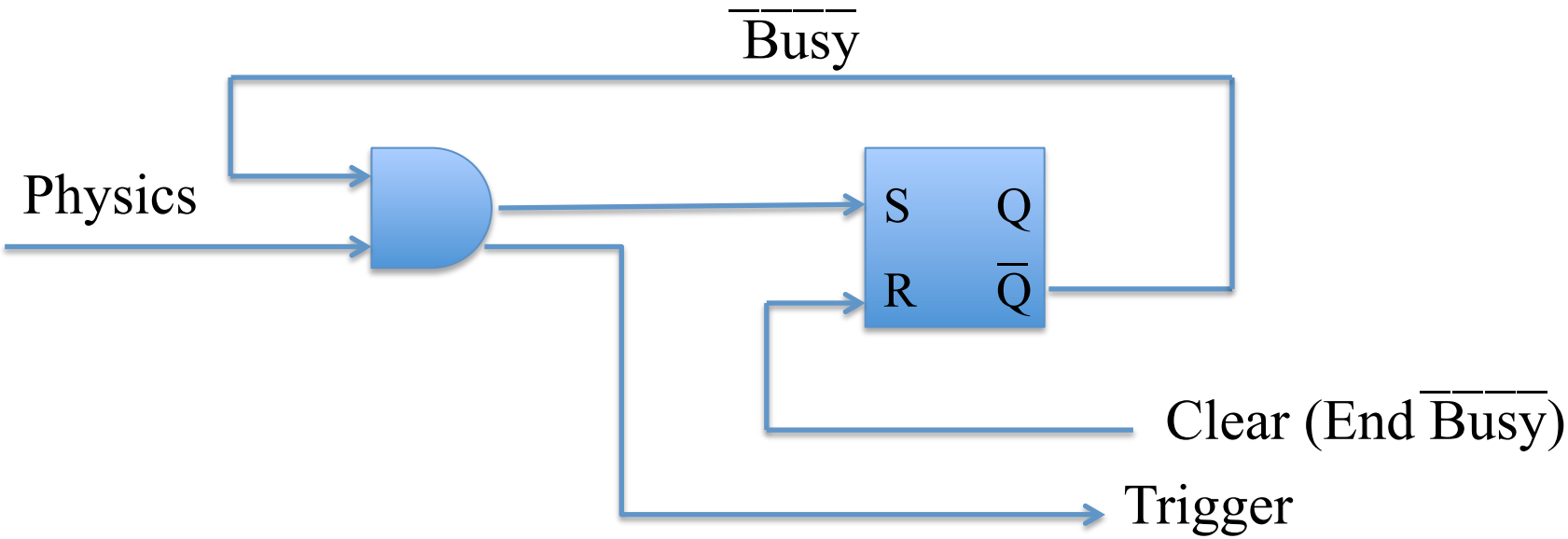
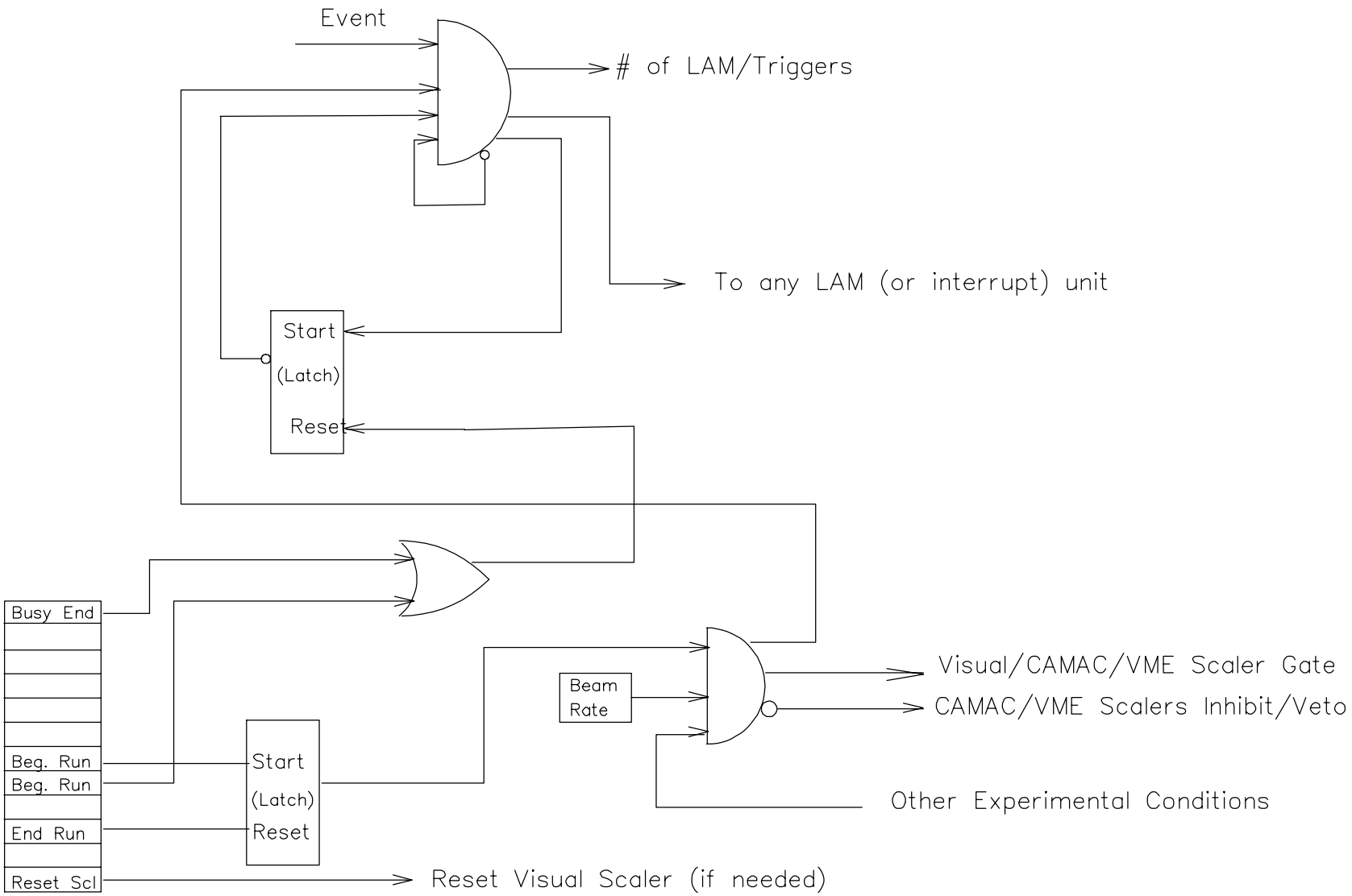
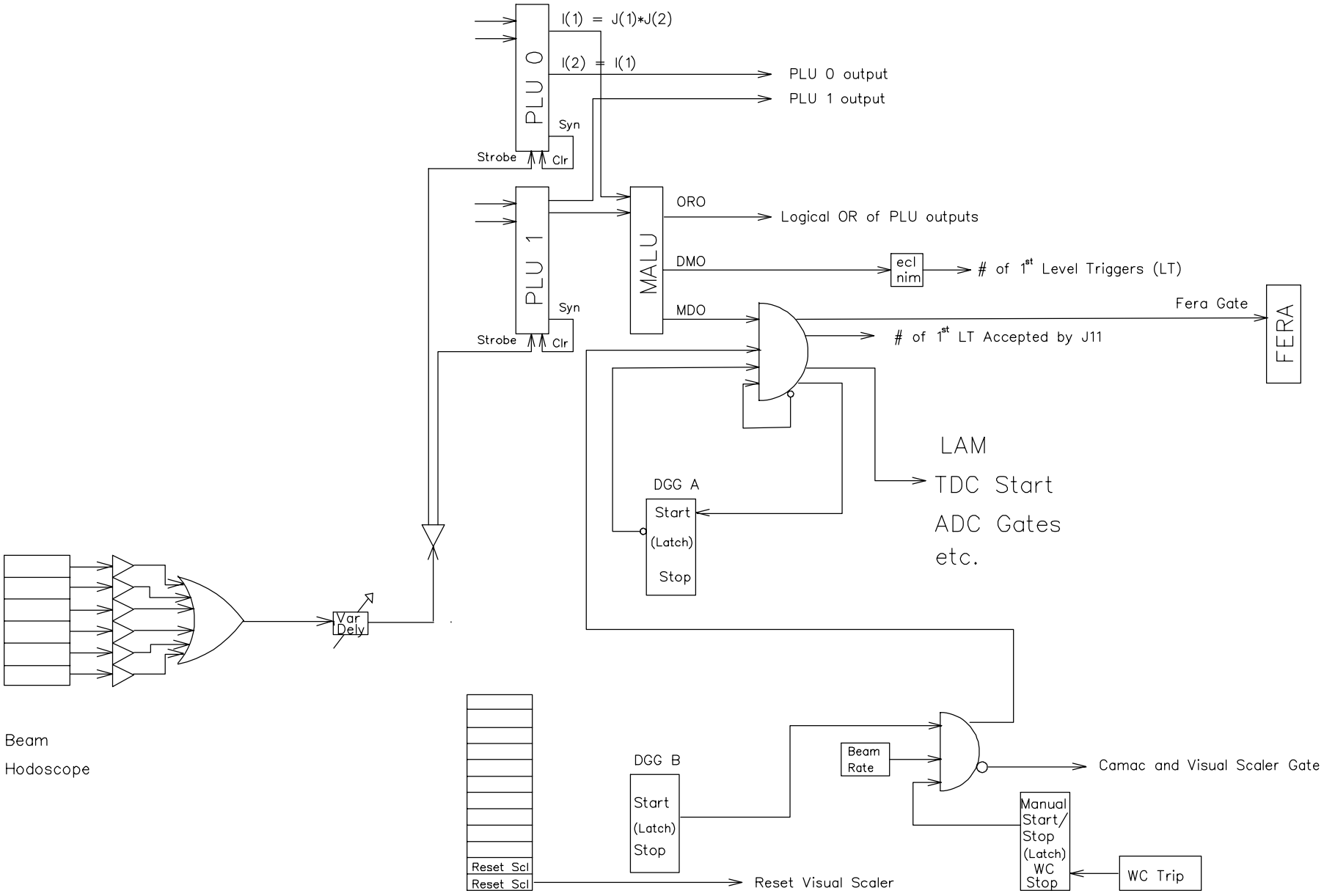
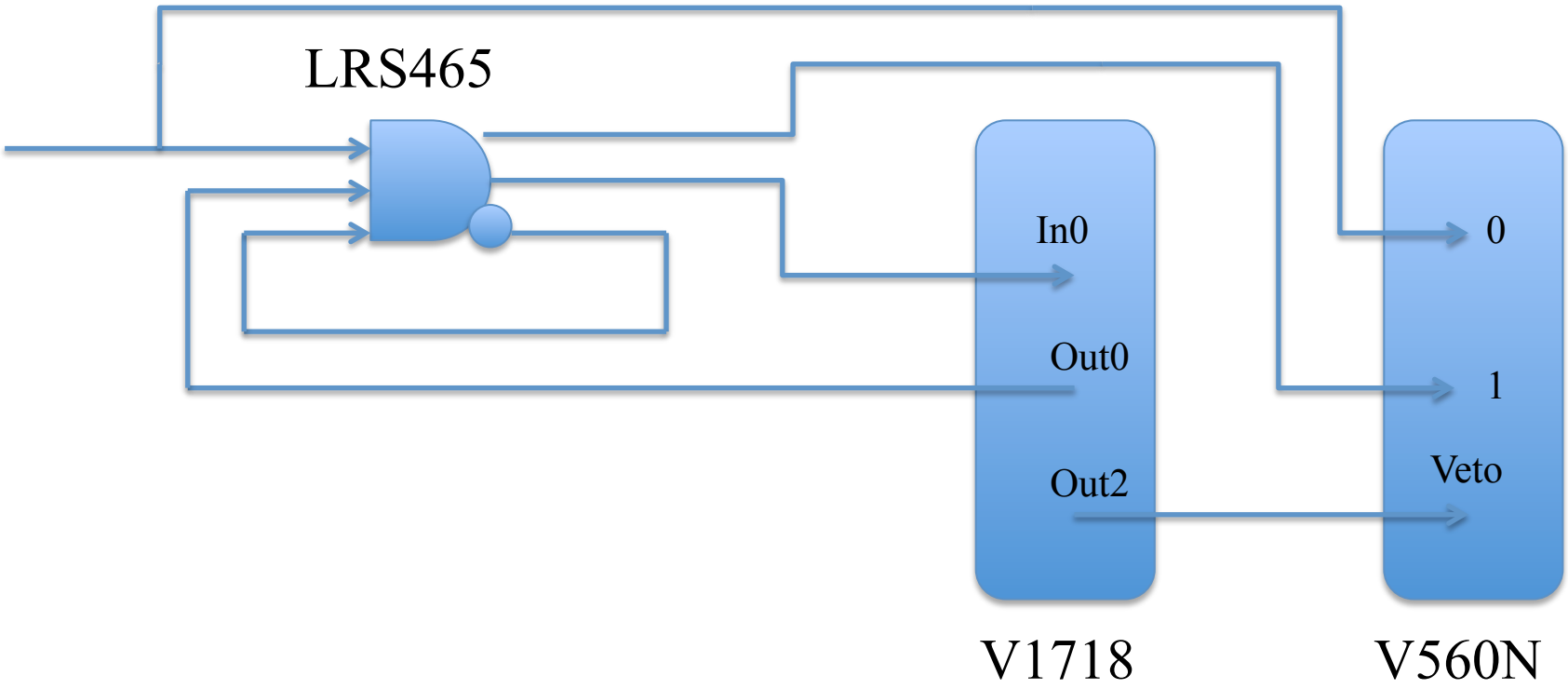


The arrival of a “Physics” event will generate a “Trigger” signal which is sent to the computer. At the same time the Trigger will inhibit the coincidence to future events by setting the “Busy-bar” signal (which will go to “zero”). The coincidence will remain inhibited until a Clear signal is sent by the computer which will end the Busy-bar signal and open the coincidence to future Physics events.

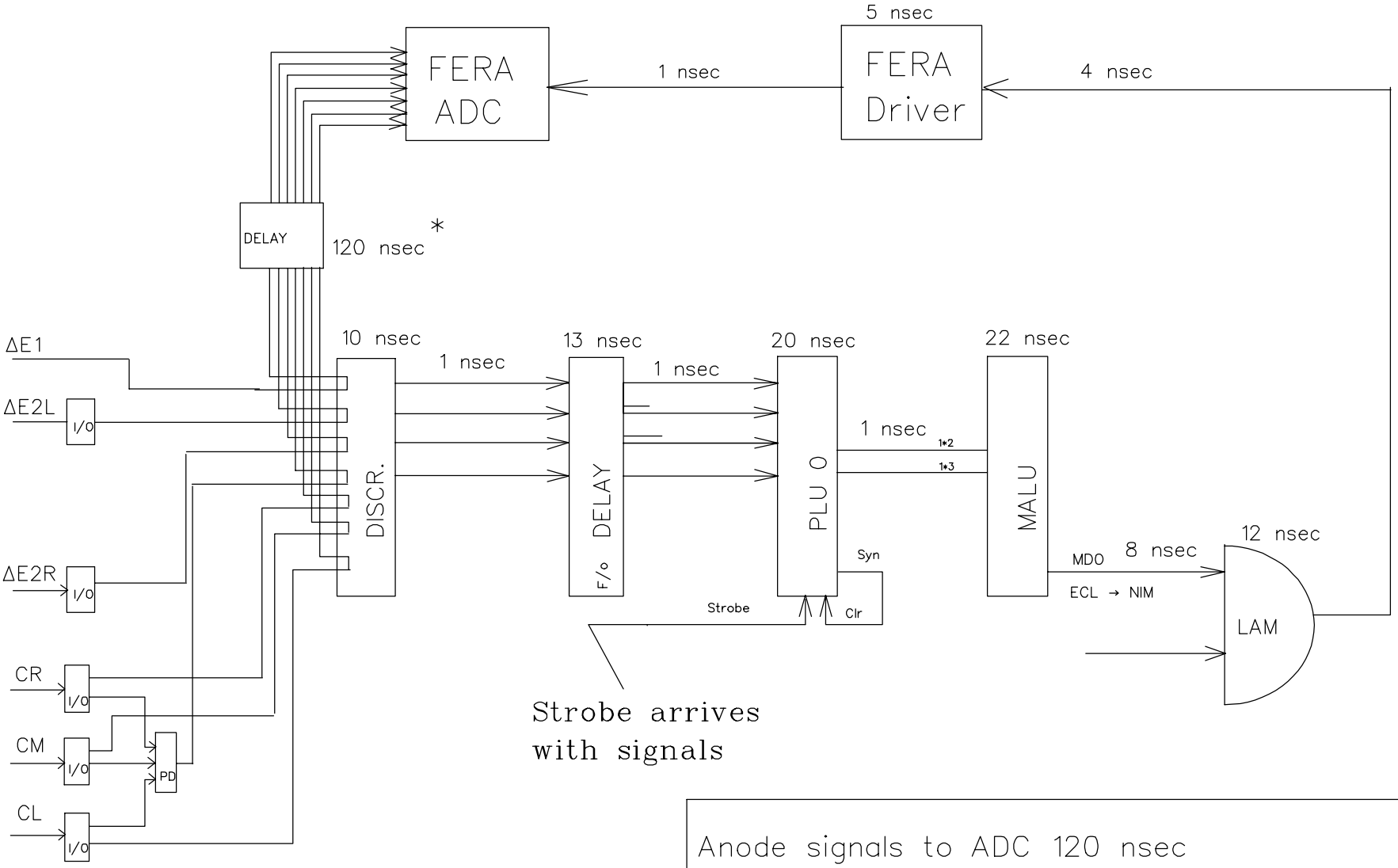

Event
# of LAM/Triggers
To any LAM (or interrupt) unit
Start
(Latch)
Reset
Busy End
Beg. Run
Beg. Run
End Run
Reset Scl
Start
(Latch)
Reset
Beam
Rate
Visual/CAMAC/VME Scaler Gate
CAMAC/VME Scalers Inhibit/Veto
Other Experimental Conditions
Reset Visual Scaler (if needed)


I(1) = J(1)*J(2)
I(2) = I(1)
PLU 0
PLU 0 output
PLU 1 output
Syn
Strobe
Clr
PLU 1
MALU
ORO
Logical OR of PLU outputs
DMO
ecl nim
# of 1st Level Triggers (LT)
MDO
Fera Gate
FERA
# of 1st LT Accepted by J11
LAM
TDC Start
ADC Gates
etc.
DGG A
Start
(Latch)
Stop
Var Dely
Beam
Hodoscope
DGG B
Beam Rate
Camac and Visual Scaler Gate
Manual Start/ Stop (Latch) WC Stop
WC Trip
Reset Scl
Reset Scl
Reset Visual Scaler




```
Out0 = Busy-bar :  Start via SW at Begin Run
                   Reset via In0 at "Physics"
                   Start via SW at End of Read Cycle
Out2 = Veto     :  Start via SW at Begin Run [Inv.Pol.]
                   Stop via SW at End of Run

Out0 and Out2 are levels, since width > period
```



*Time difference between cables can be as much as 7 nsec!!!

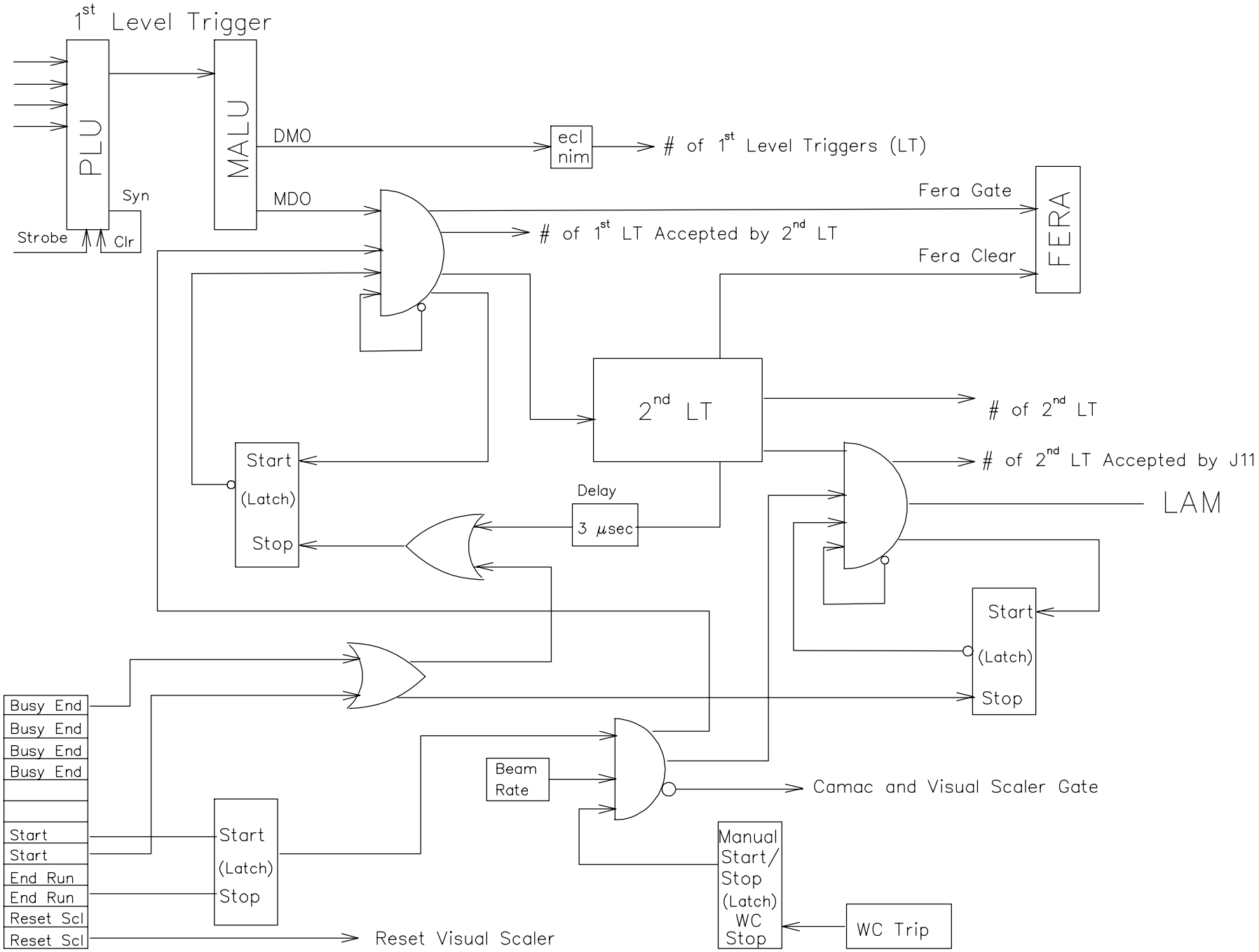
Table of Delay times

Anode signals to ADC 120 nsec

Gate to FERA ADC 98 nsec

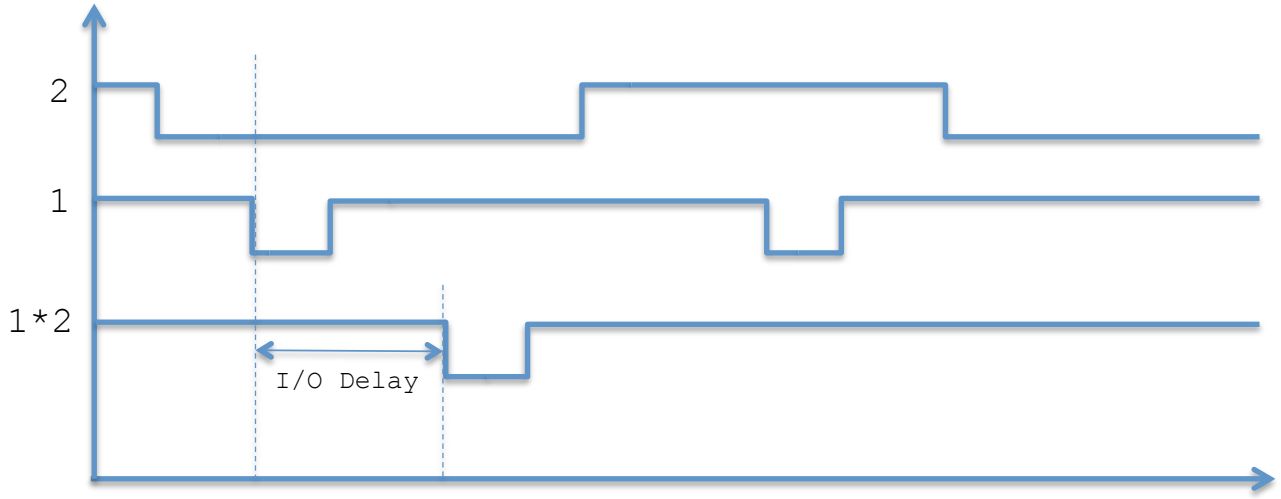
Gate arrives 20 nsec before signals

N.B. Times 0 is entrance to Discriminator

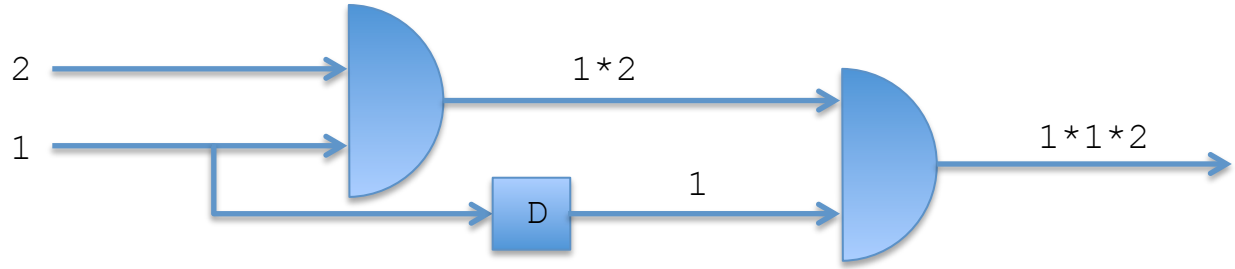

1st Level Trigger
PLU
MALU
Syn
Strobe
Clr
DMO
ecl nim
# of 1st Level Triggers (LT)
MDO
Fera Gate
# of 1st LT Accepted by 2nd LT
Fera Clear
FERA
2nd LT
# of 2nd LT
# of 2nd LT Accepted by J11
LAM
Start
(Latch)
Stop
Delay
3 μsec
Busy End
Busy End
Busy End
Busy End
Start
Start
End Run
End Run
Reset Scl
Reset Scl
Start
(Latch)
Stop
Reset Visual Scaler
Beam Rate
Camac and Visual Scaler Gate
Manual Start/ Stop (Latch) WC Stop
WC Trip

Coincidence between physics signal and external clock (Prescaling)

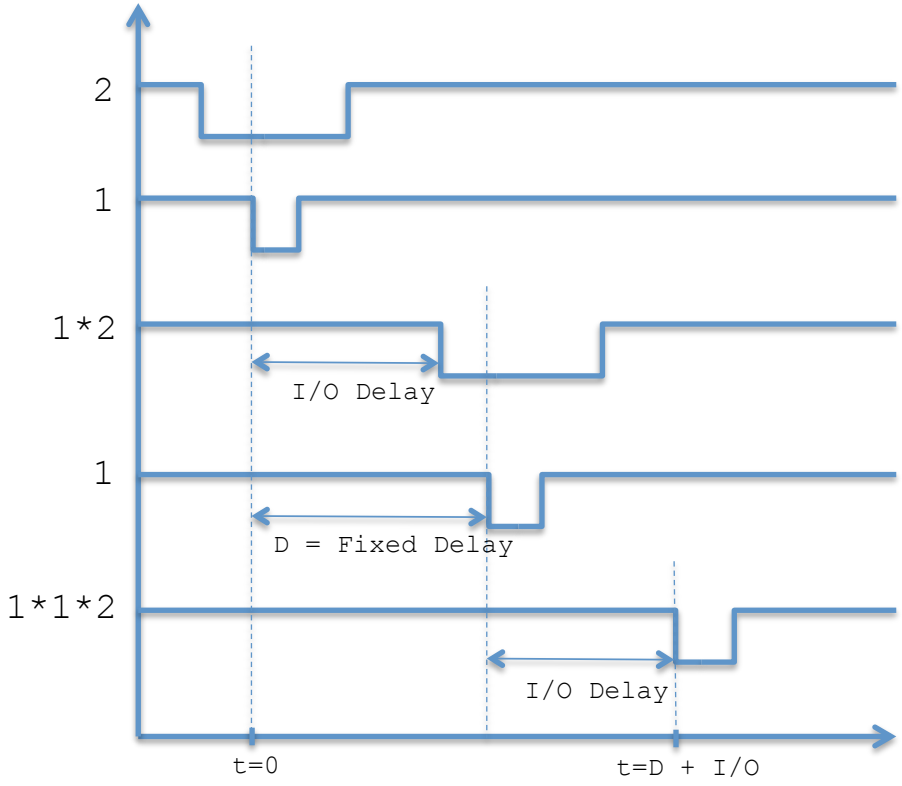
"1" is the physics signal and "2" is a clock used for for Prescaling (i.e. reducing) the number of events.



PROBLEM: If the leading edge of "2" arrives after that of "1" then we have the time of the coincidence given by the clock and NOT by the physics signal. The solution to this is to build a proper coincidence circuit (next page). Let's assume that the Input-Output delay of the instrument to be "I/O". Then by making a proper choice of the fixed delay "D" (function of "I/O" and of the width of the two signals "1" and "2") the circuit can be built in such a way that the timing is ALWAYS given by signal "1", even in those cases in which signal "2" arrives after "1". The output of the second coincidence will be delayed wrt the input of "1" by the same amount given by "I/O + D".



Timing of first coincidence given by "1"



Timing of first coincidence given by "2"