Analogue to Digital Conversion

- Turns electrical input (voltage/current) into numeric value
- Parameters and requirements

Resolution

the granularity of the digital values

Integral Non-Linearity

proportionality of output to input

Differential Non-Linearity

uniformity of digitisation increments

Conversion time

how much time to convert signal to digital value

Count-rate performance

how quickly a new conversion can begin ofter a previous event

Stability

how much values change with time

Resolution

- To convert an analogue value, eg voltage, to digital two parameters are required

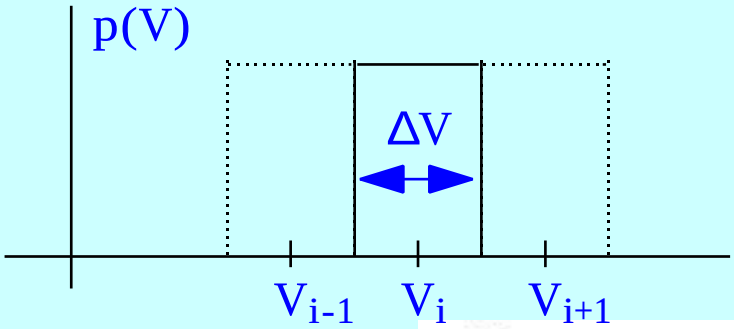
  range and number of bits

  quantum = $\Delta V = (V_{max}-V_{min})*2^{-N}$ referred to as 1LSB (least significant bit)

- eg 10 bits = $2^{10} = 1024$, $V_{max}-V_{min} = 1V$ => $\Delta V = 1V/1024 \approx 1mV$

- Ideal ADC behaviour

  probability vs amplitude

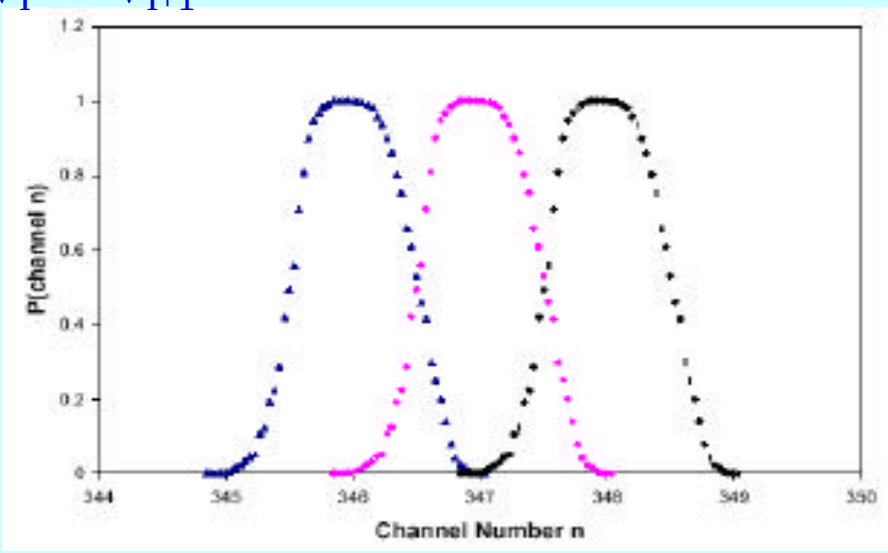


- Real ADC behaviour

  noise in digitisation process

  smears resolution

  $\sigma_{noise} < \Delta V/4$



Speed vs resolution

- from Analog Devices ADC selection guide

bits per sec (or samples per sec)

		Throughput rate (bps)					
		<10k	10-100k	100k-1M	1-10M	10-100M	>100M
Resolution (bits)	≥17	|	-------	-------	-------	-------	-------
	14-16	|	|	|	|	|	-------
	12-13	-------	|	|	|	|	|
	10-11	-------	|	|	|	|	|
	8-9	-------	-------	|	|	|	|
	≤8	-------	-------	-------	-------	|	-------

Maximum speed 200Mbps 12 bits 1.3W single channel

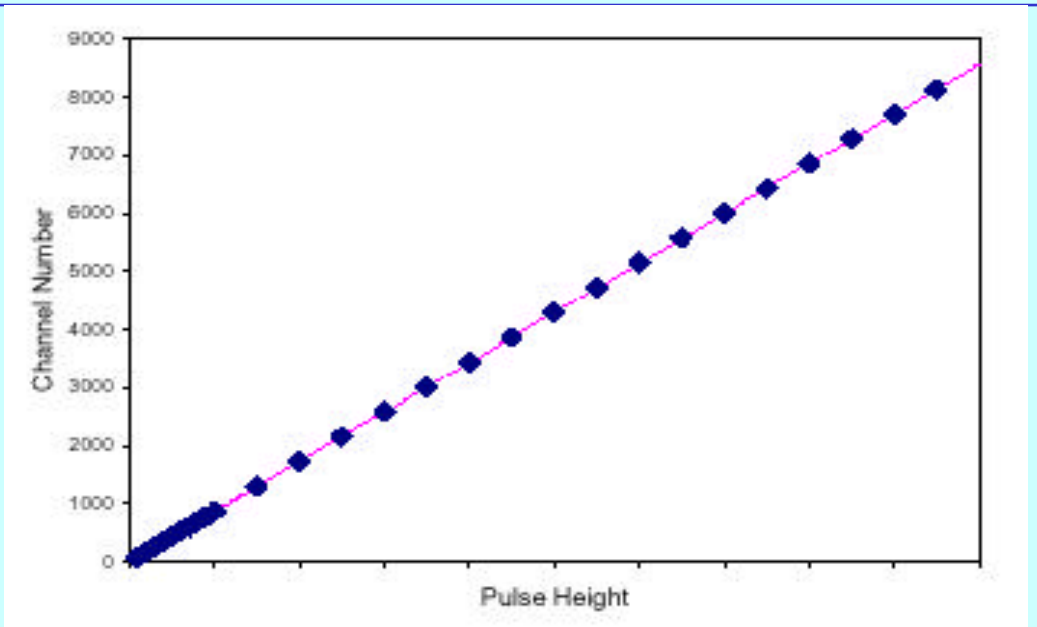
210Mbps 10bits 2.4W single channel

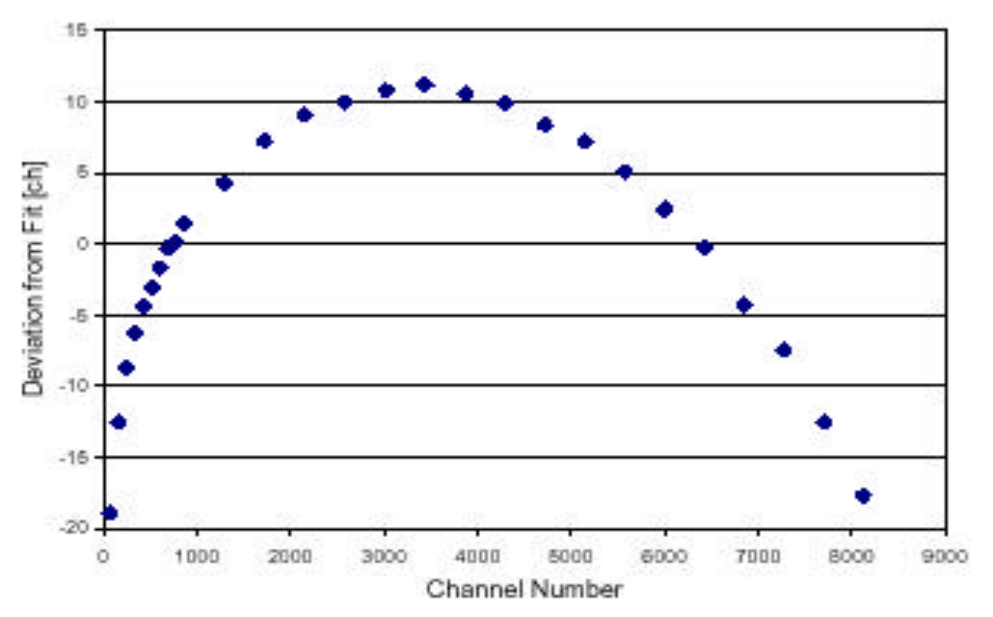
Maximum resolution 24 bits 6.4kbps

- What determines this relationship?

Integral non-linearity

- Output value D should be linearly proportional to V
  - check with plot
  - for more precise evaluation of INL
  - fit to line and plot deviations
  - plot $D_i - D_{fit}$ vs n_{chan}





Differential non-linearity

- measures non-uniformity in channel profiles over range

  $DNL = \Delta V_i / \langle \Delta V \rangle - 1$

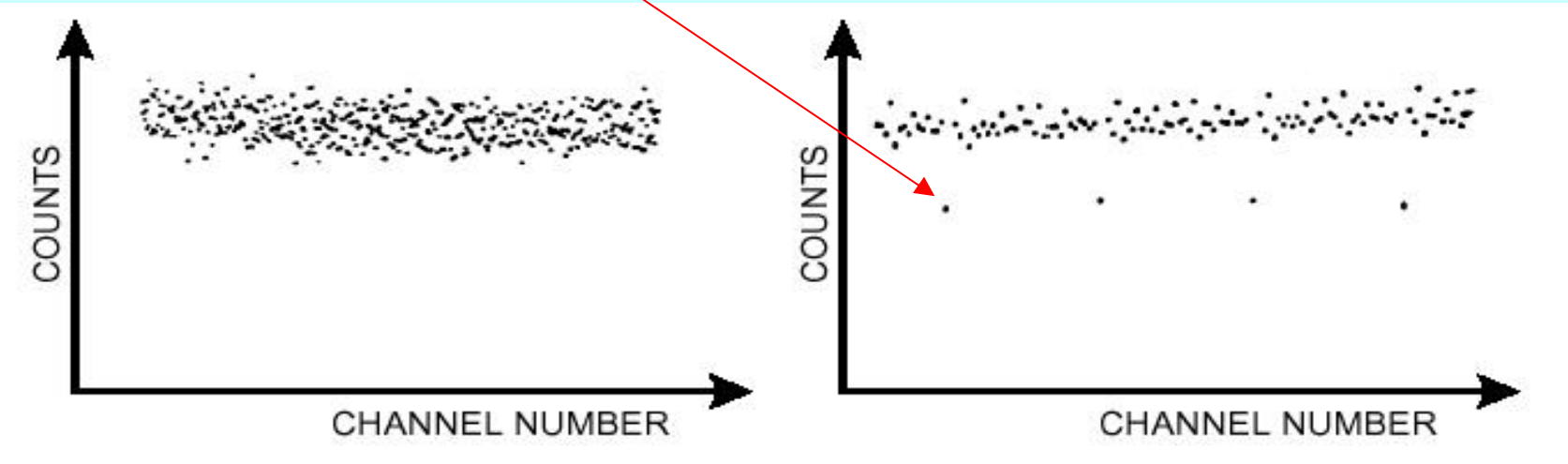
  ΔV_i = width of channel i

  $\langle \Delta V \rangle$ = average width

- rms or worst case values may be quoted

  DNL ~ 1% typical but 10^{-3} can be achieved

  can show up systematic effects, as well as random



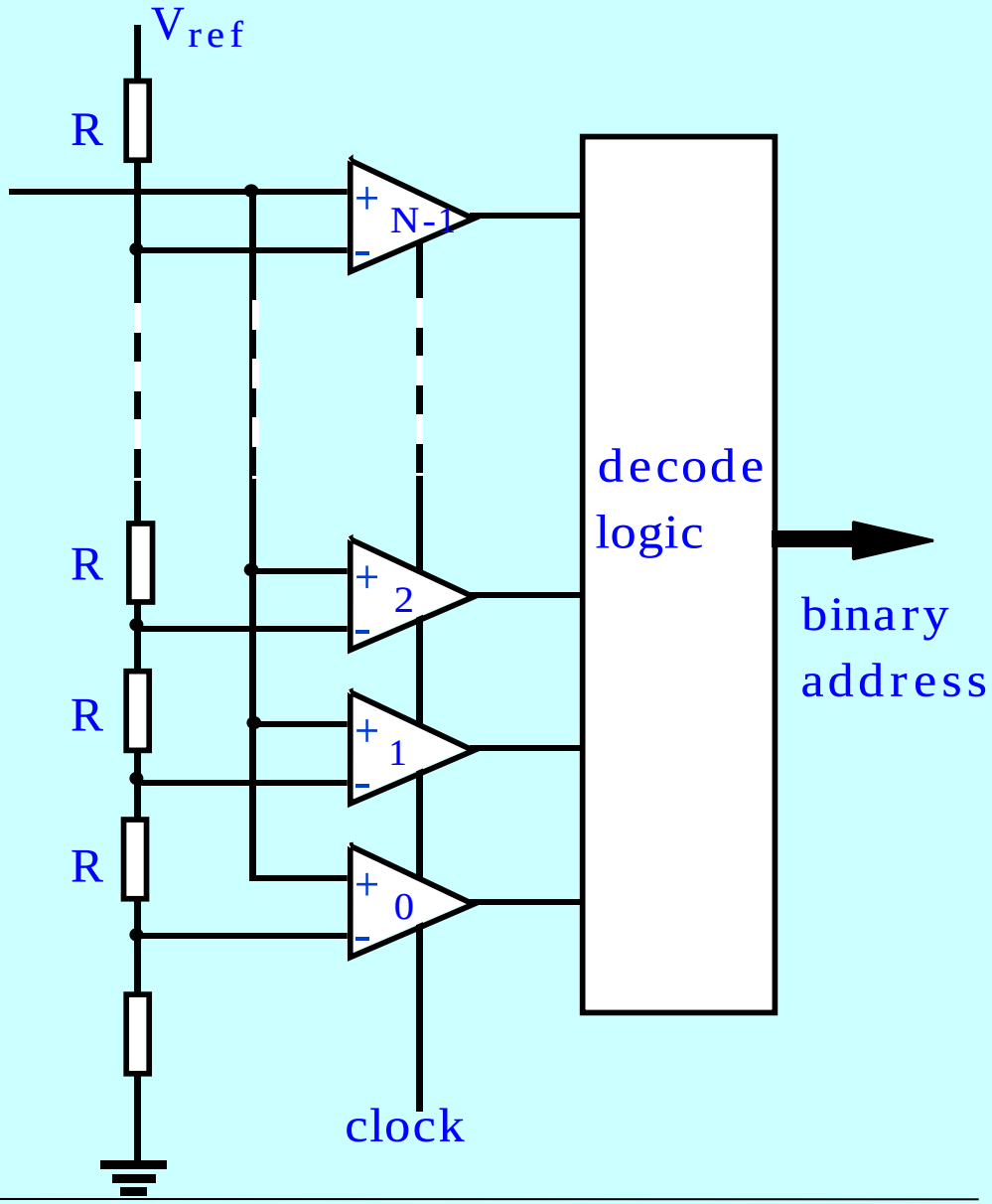
Other variables

- Conversion time
  - finite time is required for conversion and storage of values
  - may depend on signal amplitude
  - gives rise to dead time in system
    - ie system cannot handle another event during dead time
  - *may need accounting for, or risk bias in results*
- Rate effects
  - results may depend on rate of arrival of signals
  - typically lead to spectral broadening
- Stability
  - temperature effects are a typical cause of variations

- A partial solution to most of these problems is regular calibration, preferably under real operating conditions, as well as control of variables

Parallel (Flash) ADC

- Input value is compared simultaneously...
- against a set of comparators
  - 2^N comparators required for N bits
  - Threshold values defined by
  - resistor chain
  - relative accuracy important,
    - not absolute values
- Pros
  - short conversion time
    - *eg 10bits @ 40MHz*
- Cons
  - limited resolution,
    - *size of IC grows with N*
  - DNL ~ 1%
  - power consumption



Successive approximation ADC

- analogous to binary search

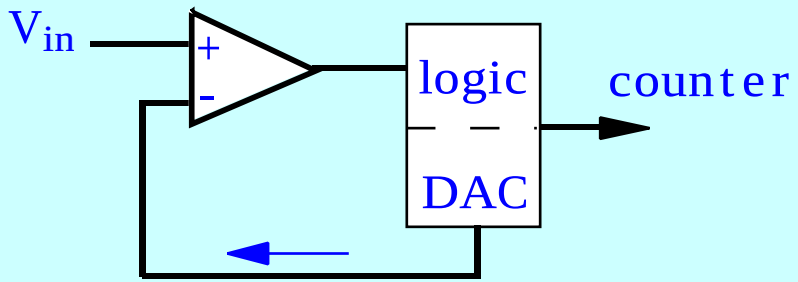
  generate $V_{ref} = \Delta V \times (2^{N-1}, 2^{N-2}, \ldots 2^0)$ in N steps

  set bit = 1

  if $V_{in} > V_{ref}$

  leave

  else bit = 0



- Pros

  speed ~ µsec

  high resolution

- Cons

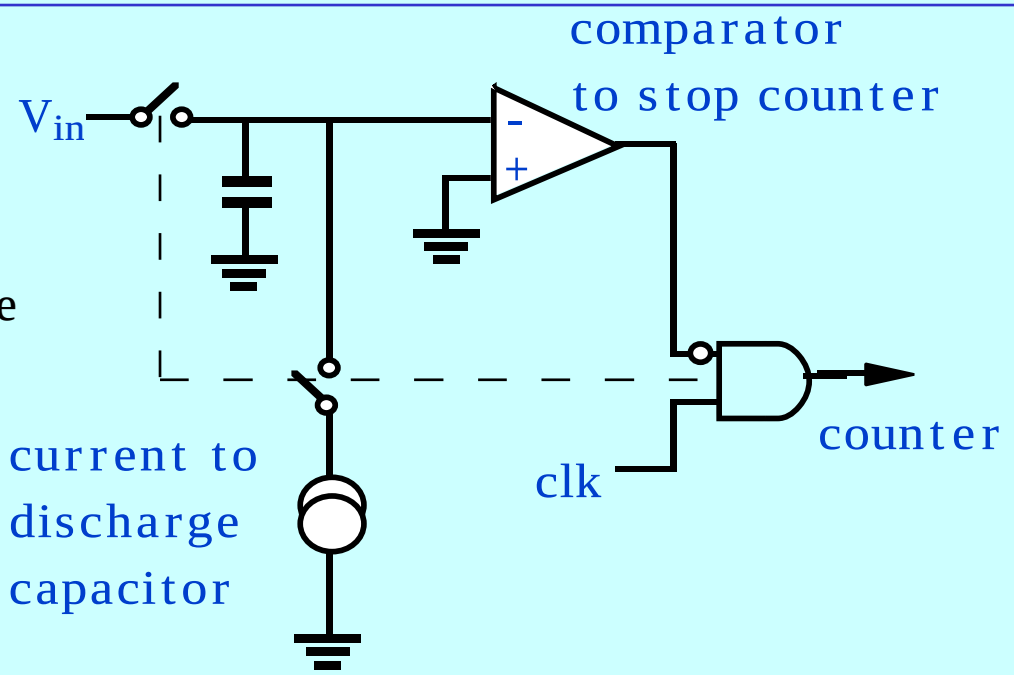
  DNL 10-20%

  very precise resistors required with DAC for V_{ref}

DAC = digital to analogue converter
ie number -> voltage

Single slope (Wilkinson) ADC

- Single slope conversion
  - input signal charges capacitor
  - discharged by constant current
  - counter (eg 200MHz) times discharge
- Pros
  - Excellent DNL
- Cons
  - modest absolute accuracy
  - slow, and conversion time depends
  - on amplitude
  - $T_{conv} = nT$ eg T = 10ns, 13 bits $T_{conv} = 82\mu s$



- Dual slope conversion reduces systematic (absolute) errors
  - charge C with constant current and then measure time for discharge
  - charge and discharge subject to same comparator and capacitor variations

Time to Digital Conversion (TDCs)

- Count clock pulses between start and stop pulses
  - up to ~1GHz, limited by technology so $\Delta t \approx 1$ns
  - capable of digitising more than one hit in an acquisition
    - *provided logic is sufficient*

- Analogue ramp
  - for greater precision, $\Delta t \geq 10$ps
  - charge capacitor with constant current source
  - start pulse: turns on current
  - stop pulse: turns off
  - then measure V on storage capacitor using ADC
    - *can't accept more than one signal in digitising period*