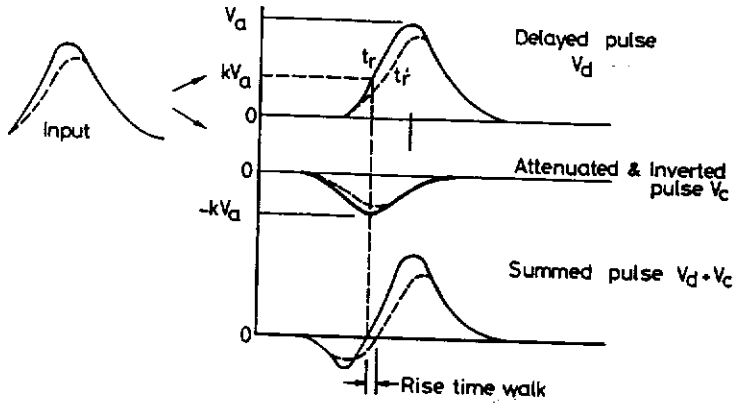

Fig. 17.5. Technique for constant fraction triggering. In order for this technique to work rise times of all signals must be the same. The dotted line shows the result with a different rise time signal

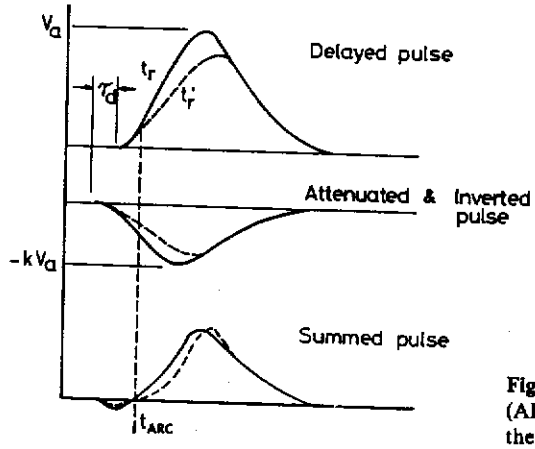

Fig. 17.6. Amplitude and risetime compensation (ARC) triggering. The zero-crossover occurs before the signal peak is reached

moved with a variant of CFT known as *amplitude and risetime compensation* (ARC) triggering. The difference is simply in the delay τ_d. In the true CFT method, τ_d must be long enough to allow the undelayed signal to reach its peak. In the ARC method, τ_d is made smaller than the rise time so that the summed signal crosses before the signal maximum is reached. The zero-crossing time thus depends only on the early portion of the signal where differences between pulse shapes are at a minimum. This is illustrated in Fig. 17.6. ARC triggering is the most precise method available today and is most useful with large volume semiconductor detectors where the pulses vary in shape as well as amplitude.

17.3 Analog Timing Methods

Assuming that the proper choice of time-pickoff method is chosen, let us now consider some electronic techniques for measuring the time difference between two signals. We divide these into analogic and digital techniques.

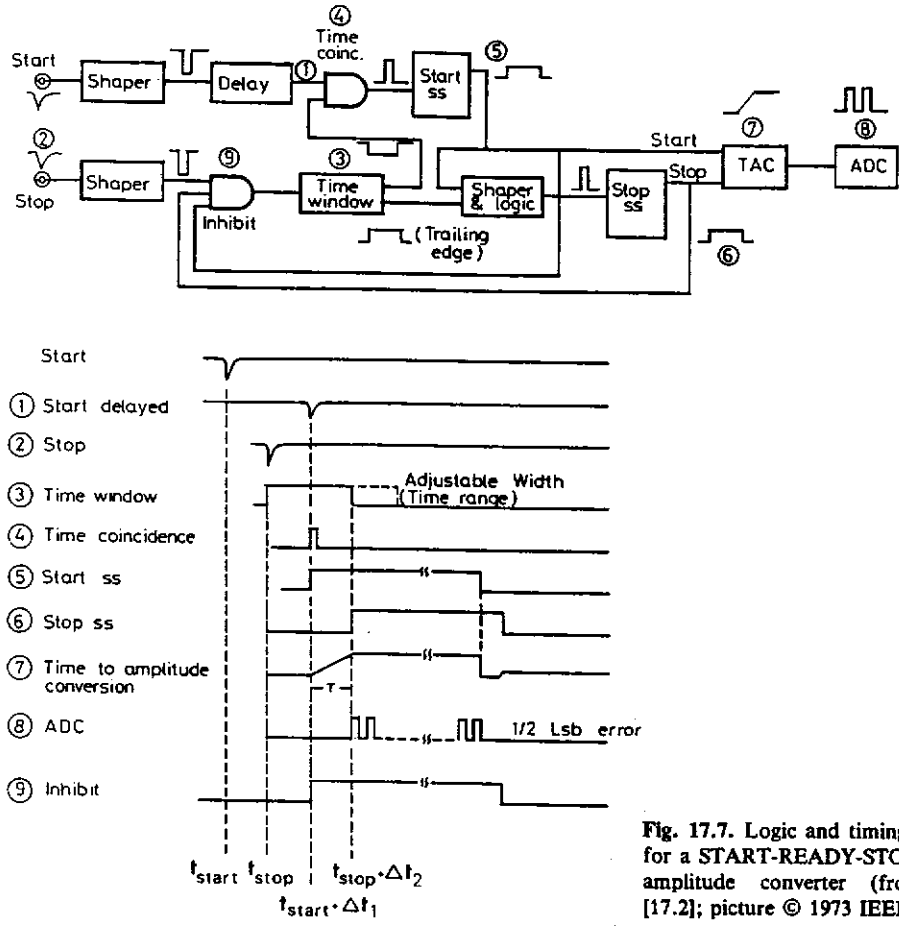

Fig. 17.7. Logic and timing diagrams for a START-READY-STOP time-to-amplitude converter (from *Porat* [17.2]; picture © 1973 IEEE)

17.3.1 The START-STOP Time-to-Amplitude Converter

The primary example of analogic time interval measurement is the START-STOP time-to-amplitude converter. The basic method is to relate the time interval between two events to the quantity of charge discharged by a capacitor during this period. As shown in Fig. 14.22, the arrival of the first signal (START) gates on the capacitor which discharges at a constant rate until the arrival of the STOP signal. The total charge collected thus forms an output signal whose height is proportional to the time difference between the START and STOP signals. The capacitor is then recharged and the next event awaited. If no STOP signal arrives, however, the output signal reaches its maximum amplitude which then causes an overflow condition. Such events, of course, cause a great deal of dead time. To remedy this, some START-STOP TAC's include additional logic circuits at the beginning to test for the presence of a STOP within the allowed time window before discharging of the capacitor begins. This technique, sometimes known as START-READY-STOP, is illustrated in Fig. 17.7.

17.3.2 Time Overlap TAC's

An alternate method reminiscent of coincidence circuits is the *time-overlap* technique. In this scheme, the overlap between two wide START and STOP pulses is measured

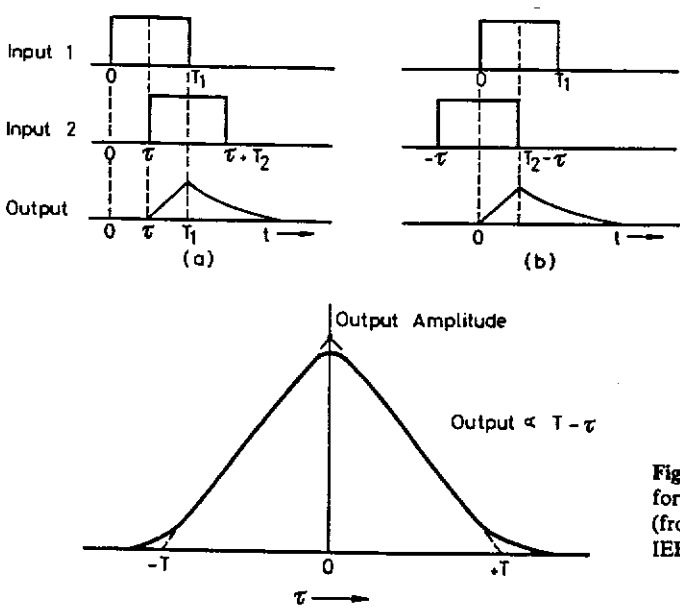

Fig. 17.8. The time overlap method for time-to-amplitude conversion (from *Porat* [17.2]; picture © 1973 IEEE)

and the difference taken. This is illustrated in Fig. 17.8. The capacitor is charged during the overlap period yielding a pulse whose height is proportional to

$$T - \tau \,, \tag{17.2}$$

where τ is the time interval to be measured and T is the full width of the pulse. Knowing T, the period τ then follows. This method, of course, is restricted only to periods smaller than the pulse with T. Intervals larger than this provoke an overflow signal or no signal at all. Note also that without further auxiliary logic, the method does not distinguish between which pulse arrives first.

17.4 Digital Timing Methods

17.4.1 The Time-to-Digital Converter (TDC)

To obtain a time interval measurement in digital form, one obvious method is to digitize the TAC using an ADC. However, more direct methods are available using counting techniques and stable oscillators. The basic principle here is to use the START signal to gate on a scaler which counts a constant frequency oscillator (or clock). At the arrival of a second STOP signal, this scaler is gated off to yield a number proportional to the time interval between the pulses.

Counting-type TDC's are easily constructed from simple logic modules found in the laboratory. Figure 17.9 illustrates one such system using AND and OR gates, simple SR flip-flops and timers. Here, the arrival of the START sets a flip-flop (Busy) which inhibits any further STARTs which may arrive while the TDC is in operation. At the same time, a gate signal is generated for the scaler, and a timer, set to a maximum time window, triggered. The scaler may be stopped in either of two ways: (1) by a *true* STOP which arrives within the defined time window, or, (2) by the end of this window. A *true*

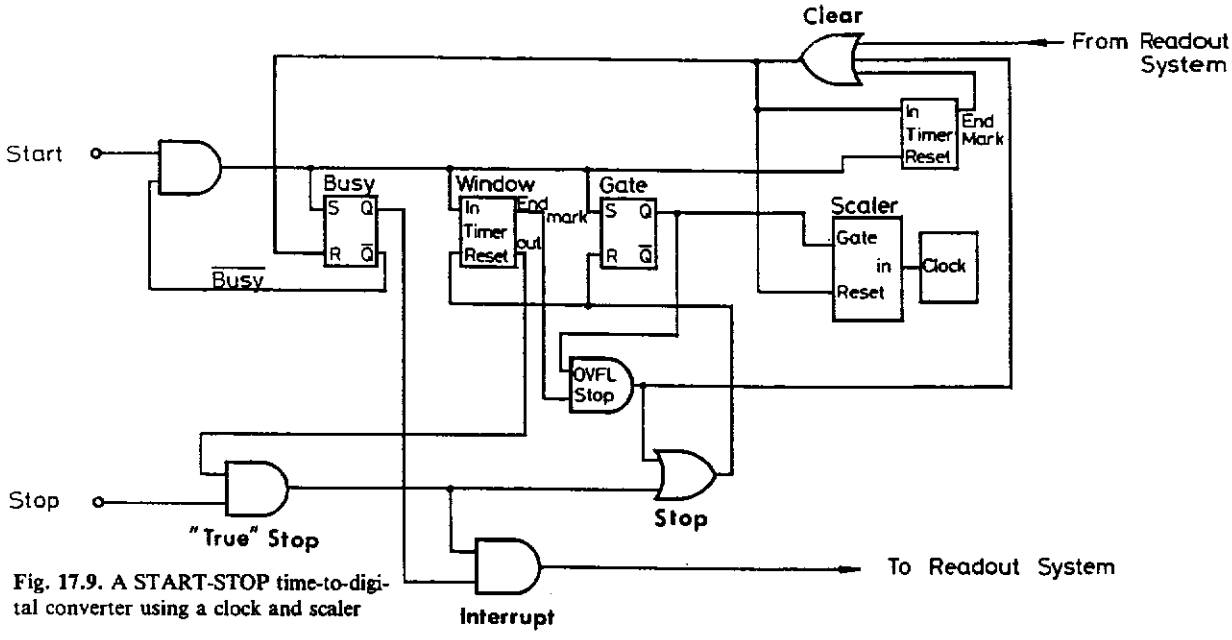

Fig. 17.9. A START-STOP time-to-digital converter using a clock and scaler

STOP is defined by the requirement that the timer still be running when the signal arrives. This is tested by the first AND gate in the STOP channel. If this condition is met, both the scaler and the window timer are gated off. An interrupt signal is then generated to trigger the readout system. After the value of the scaler is read and safely stored, the readout system generates a CLEAR signal which then resets the scaler and the BUSY flip-flop. The system then awaits the next event. If no STOP arrives within the time window, the end marker from the timer then automatically triggers a STOP and CLEAR without interrupting the readout system.

One must consider the possibility of events in which both a START and STOP signal arrive at the same time. Such an event is prohibited by the SR flip-flop logic and may cause the flip-flop to "*hang-up*" in an indeterminate state, blocking the system. This may be remedied by using a second "*watchdog*" timer which is triggered by each CLEAR, and reset by each START. The period of the timer should be set to a value large compared to the time between events. If no START arrives in such a long period, then the system is most likely blocked, and a CLEAR signal issued.

The resolution of the counting TDC depends on the frequency of the clock used: the higher the frequency, the smaller the time interval measured. For a given frequency however, this resolution can be doubled by using two clocks synchronized on opposite phases. This method is shown in Fig. 17.10.

17.4.2 The Vernier TDC

A second counting method is the *vernier* technique. The basic principle is illustrated in Fig. 17.11. Two oscillators of slightly different frequencies, f_1 and f_2, are used. The arrival of a START gates on the first clock while the second remains off. The moment the STOP arrives, the second clock is gated on and continues oscillating along with the first clock until the two are in phase. At this point, both are stopped. The contents of the two scalers are then related by

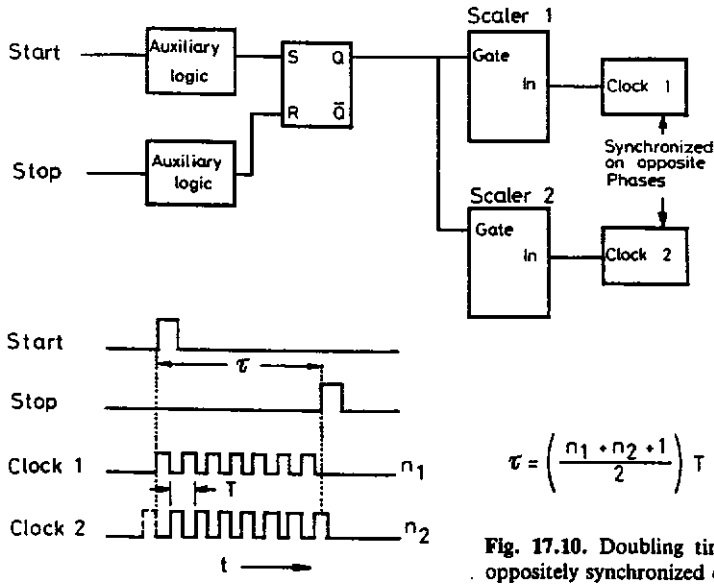

Fig. 17.10. Doubling timing resolution by using two oppositely synchronized clocks

$$n_1 T_1 = n_2 T_2 + \tau \ , \tag{17.3}$$

where n_1 and n_2 are the number of pulses counted, T_1 and T_2 are the periods of the two clocks and τ is the time interval to be measured. Solving for τ then is trivial, and

$$\tau = \frac{n_1}{f_1} - \frac{n_2}{f_2} \ . \tag{17.4}$$

For time intervals smaller than the period of the clocks, $n_1 = n_2 = n$, so that,

$$\tau = n\left(\frac{1}{f_1} - \frac{1}{f_2}\right) = n\frac{\Delta f}{f_1 f_2} \ . \tag{17.5}$$

From the above, we see immediately, then, that the resolution depends on the frequency difference Δf. If most vernier TDC's, this is usually 1% although this can be improved.

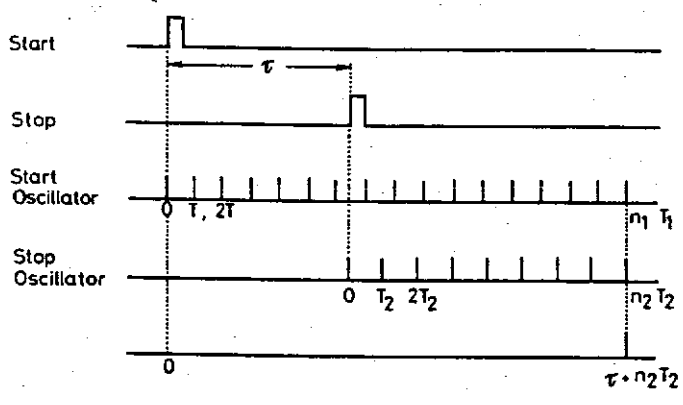

Fig. 17.11. Working principle of the vernier TDC

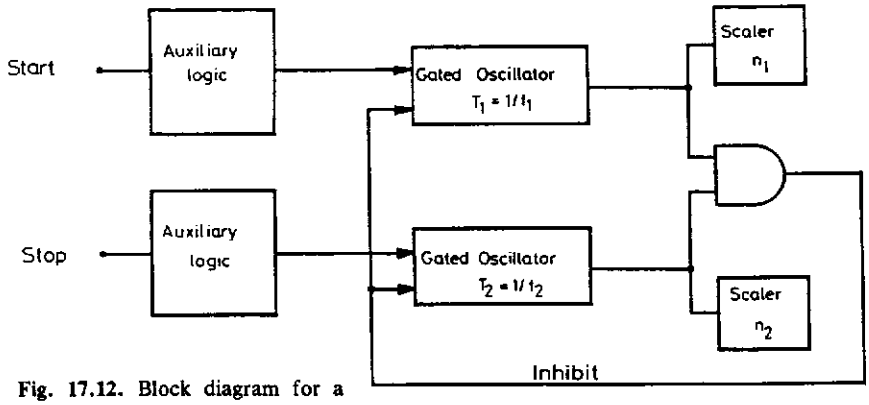

Fig. 17.12. Block diagram for a vernier TDC

Like the normal counting TDC discussed above, the vernier TDC may also be easily constructed from simple logic modules. One such set-up is shown in Fig. 17.12.

17.4.3 Calibrating the Timing System

Once a timing system has been chosen and constructed, it is necessary to calibrate the time scale and also to have a measure of system linearity and resolution. A simple method for calibrating the absolute channel width is to use a single source such as a fast pulse generator or a photomultiplier to drive both the START and STOP channels. The output signal is split in two with the STOP channel signal passing through a variable delay. Simple cable delays are the easiest and most accurate delay devices. The distance between peaks produced by the different delays then gives a calibration of the time scale. The width of each peak serves also as a measure of the time resolution. This is illustrated in Fig. 17.13.

In order to measure the linearity of the system, a source of random events uniformly distributed in time is necessary. While random pulse generators are commercially available, a simpler method is to use photomultiplier pulses produced by a radioactive source and a pulse generator with a frequency comparable to the counting rate. The clock pulses are applied to the START channel while the photomultiplier pulses are used for the STOP channel (see Fig. 17.14). The time intervals thus produced are uniformly distributed on the time scale and, within statistical errors, should produce the same number of counts in each channel. The degree of uniformity then provides a measure of the differential linearity of the system. From this, the integral linearity can be

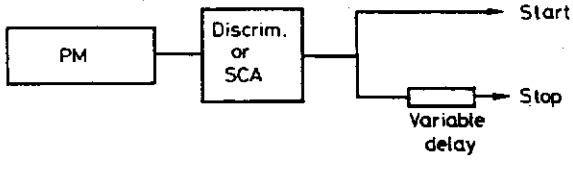

Fig. 17.13. Time scale calibration with a single source

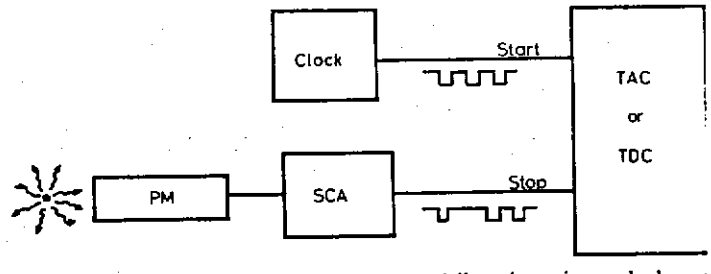

Fig. 17.14. Measuring differential and integral linearity using a clock and radioactive source

obtained by plotting the integral counts versus channel number. The accuracy of this method is generally very good and is only limited by the amplitude walk inherent in the triggering system used. An improvement can be made, however, by restricting accepted pulses to a small amplitude range. As described in Chap. 5, this method may also be used to determine the dead time of the system.