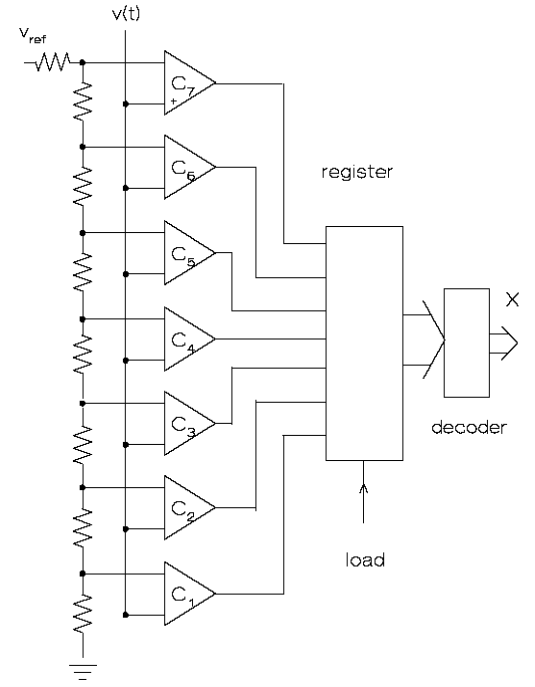
Analog–to- Digital Conversion (ADC)

An analog-to-digital converter (ADC, A/D or A-to-D) is an electronic circuit, which converts continuous signals (voltage or current) to discrete digital numbers (may be different coding systems, such as binary, Gray code or two's complement binary

A variety of arrangements have been developed:

1. Parallel or flash
2. Counting converter
3. Sample and hold
4. Tracking ADC
5. Successive approximation ADC
6. Voltage-to-time converter
7. Dual-slope converter

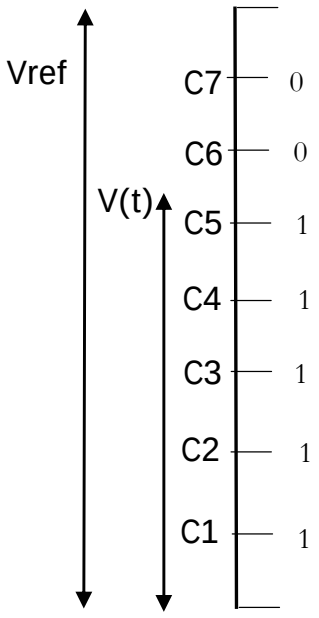
Flash or parallel converter



- Employing 2^N resistors, Vref;
- Signal V(t) is sent to 2^N-1 comparators;
- Assume N=3 bit resolution

ADC with resolution of N=3 can encode input to one in 8 different levels, since $2^3 = 8$

Conversion using parallel ADC is analog to the use of ruler:



For n-th comparator
the set of outputs of the form:

Cn=1 with and Cn=0 with k>n.

This set of outputs can be considered as a 2^N-1 bit word.

Resolution (quantizing voltage) :
number of discrete values that can be produced

Resolution can be calculated as:

$$V_0 = \frac{V_{ref}}{2^N} = \frac{V_{ref}}{2^3}$$

where V_{ref} is the reference voltage and
N is the number of bits.

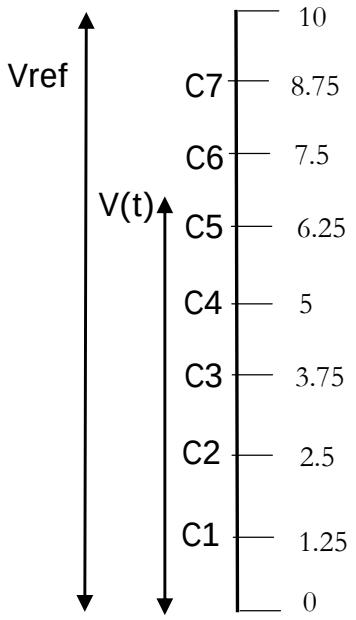
Example1:
Vref = -10 to +10 volts
N=3 bits:
2^3 = 8 codes

$$V_0 = \frac{V_{ref}}{2^3} = \frac{20volts}{8} = 2.5volts/code$$

Example2:
Vref = 0 to +10 volts
N=3 bits:
2^3 = 8 codes

$$V_0 = \frac{10volts}{2^3} = 1.25volts/code$$

continue example2:



The segment

is mapped onto the integer 5.

Why? no rounding up is allowed
the integer value is defined
so that integer 5.9999=5

• it is clearly advantageous to divide the interval into as many segments as possible to minimize the uncertainty in the estimate of input imposed by mapping.

• in practice, resolution is limited by the signal-to-noise ratio

Input-output relation:

$$\mathbb{I}_{10}(X) = \text{int}(2^N \frac{V(t)}{V_{ref}})$$

N-bit word X which is the digital output on unsigned binary integer code.
This equation is true for all ADCs.

Advantages of parallel ADC:

•ready “in a flash”- conversion time is limited by propagation delays.

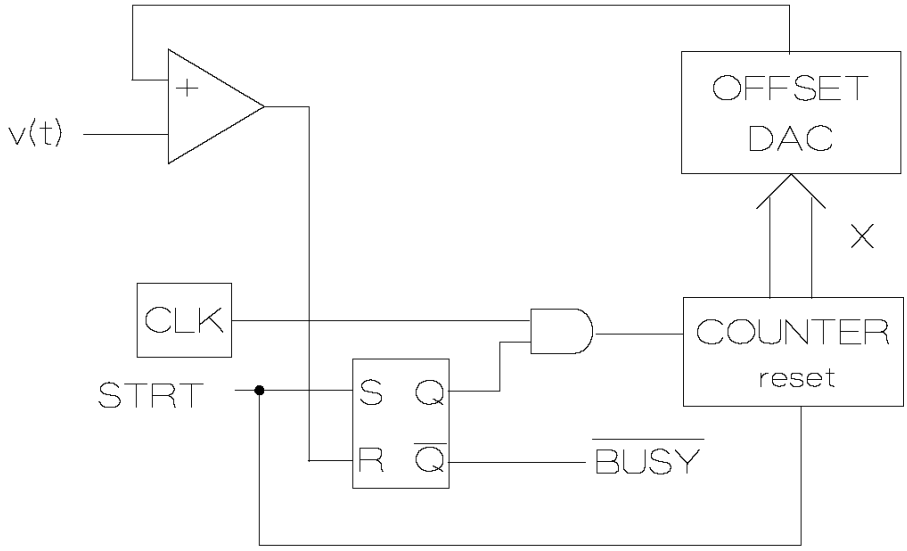
Disadvantages of ‘flash’:

•high resolution flash ADC is rare since
large number of components is required.
(12-bit resolution required 2^{12}=4096 comparators);

Folding ADC (Gilbert multiplier) re-uses the comparators multiple times
M-times folding circuit reduces number of comparators from 2^N-1 to 2^N/M.

Alternatively, use counting converter,
but at the expense of the conversion time.

Counting converter



If n is the number of pulses holds by the COUNTER , then the DAC output voltage is:

$$V_{DAC} = (n+1)V_0$$

And measured voltage V(t) is within the range:

$$nV_0 \le V(t) < (n+1)V_0$$

note: equality at the lower boundary

Conversion time:

$$T_{con} = \frac{n}{f} + \tau$$

where f is the clock frequency, n is the number of clock pulses and τ is the propagation delay

For high resolution ADC conversion time might be considerable

Example:
13-bit
Number of pulses n=6000
F=1MHz
Tcon > 6milliseconds

Disadvantages:

There is an uncertainty in time t at which the measurement of $v(t)$ is made (time t can be sensed as a positive going edge of the NOT BUSY signal)

Tracking ADC

•Modification of the counting converter;

• Suitable for stable signals;

•Used up/down counter and not reset after each measurement;

•Limitation is the slew rate, maximum rate of change of signal; for signal changes exceeding slew rate it is not possible for ADC to 'keep up'.
Slew rate is defined by conversion time $T_{conversion}$

Limitation of tracking ADC
is the slew rate- maximum rate of change of signal.

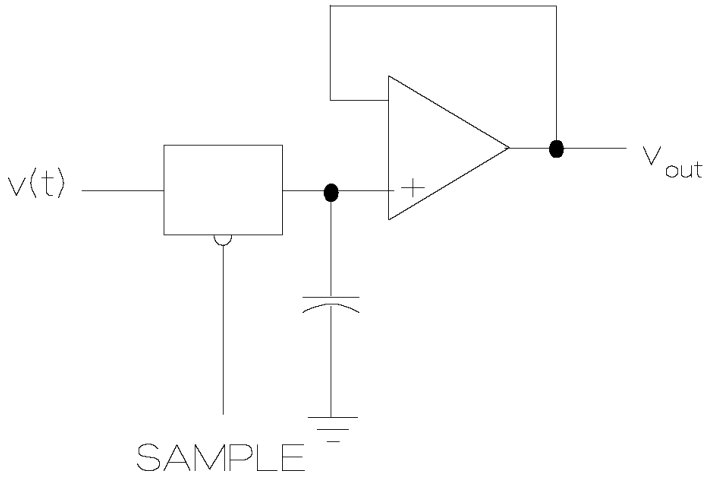
For signal changes exceeding slew rate it is not possible for ADC to 'keep up'.

Slew rate is defined by conversion time $T_{conversion}$:

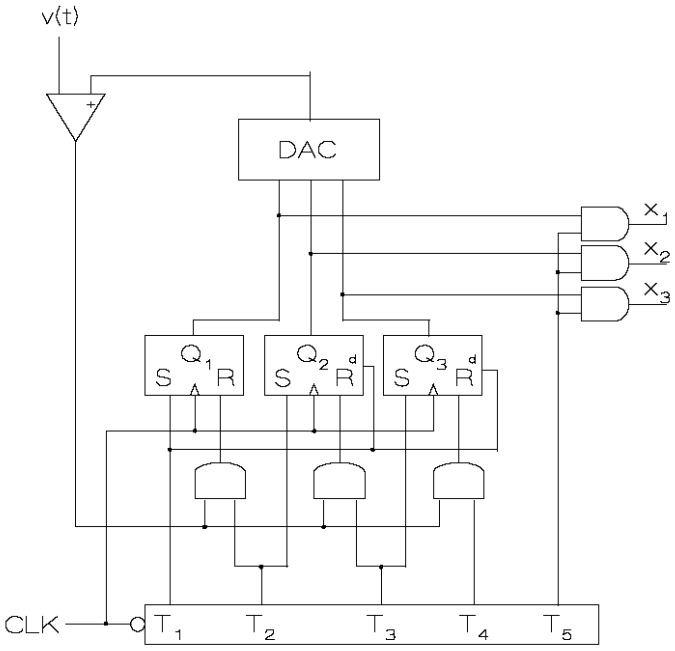
example:
after **n** clock pulses the DAC output increases by $\mathbf{nV_0}$ volts;
the time taken is $\mathbf{n/f}$, where f is the clock frequency.
Thus, the slew rate is $\mathbf{V_0 f}$ volts per second.

‘Sample and Hold’ converter

This type of ADC is used when it is desired to precisely define the time at which the signal is measured.



Successive Approximation ADC



Major sub-circuits:

- Analog voltage comparator
- Successive approximation register
- Internal reference DAC
- Sample and hold circuit to acquire the input voltage V(t) (not shown)

Action is similar to weighing a sample on the scale.

•At time T1 the flip-flop1 set is high and ff2 and ff3 are reset;

•Code 100 is fed into DAC and then supplies the analog equivalent (V_{test}) into comparator for comparison with input V(t);
if Vtest > V(t), then 100(4volts) is reset for 010(2volts)
if Vtest < V(t) then 100(4volts) is 110(6volts)

•Search continues until every bit is tested;

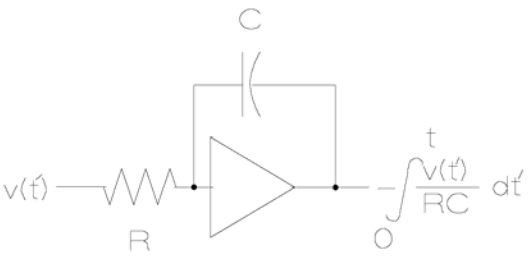
•The resulting code is the digital approximation of the sampled input voltage and is finally output by the ADC at the end of the conversion.

Register is driven by CLK so that positive clock edge occurs at the middle of each phase.

Voltage to time converter

Wilkinson type

Generates a ramp voltage using integrating op-amp (input constant, output varies linearly with time)



Assume V(t`)=-Vref, then the output is $V_{out}(t) = V_{ref}\frac{t}{RC}$

Time to increase ramp to desired value is

$$T = RC\frac{V_{measured}}{V_{ref}}$$

Time interval T can be digitized by CLK pulses

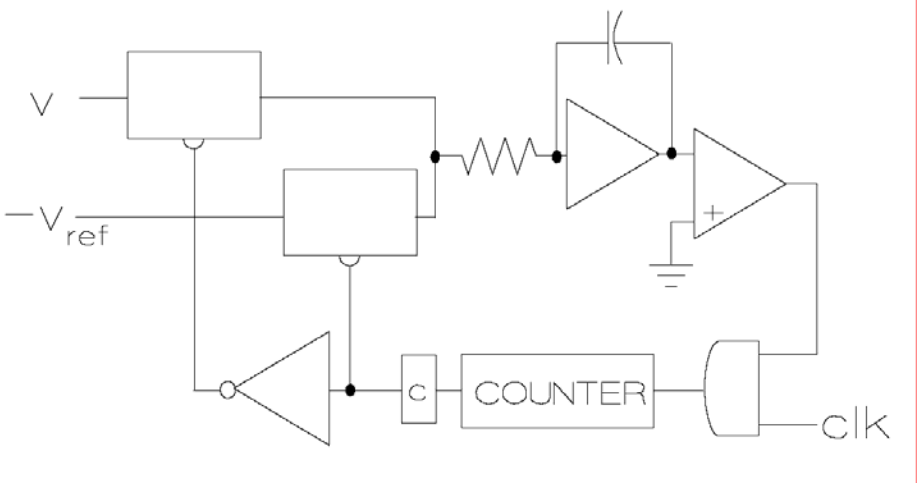
$$n = \text{int}(fT) = \text{int}(fRC\frac{V_{measured}}{V_{ref}}) = \text{int}(2^N\frac{V_{measured}}{V_{ref}})$$

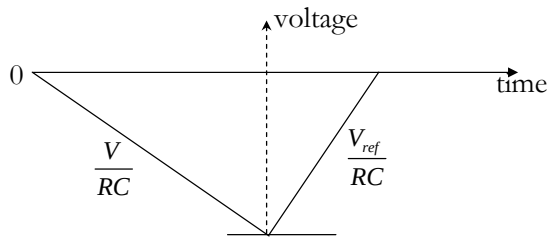
here f is the time interval between the clock pulses in seconds.

choice of the circuit parameters so that

Dual-slope voltage converter

- modification of Wilkinson
- counts down and than up to make the result independent of f, R, and C





$$-2^N \frac{V}{fRC} = \frac{-V_{ref} T}{RC}$$

The contents of the counter at the end of the conversion:

$$n = \text{int}(fT) = \text{int}(2^N \frac{V_{measured}}{V_{ref}})$$

Conversion time now is: $T_{conversion} = (2^N + n) / f$

Note about accuracy

sources of errors in voltage calculations:

1. Quantization error - due to the finite resolution of the ADC

2. Non-linearity - output to deviate from a linear function; can be eliminated by calibration

3. Aperture error- due to a clock jitter (unwanted variation of the signal)