Chapter 2
Time-to-Digital Converter Basics

Abstract On the basis of a generic mixed-signal system the scaling difficulties of analog and mixed-signal circuits based on a signal representation in the voltage domain are discussed for nanometer CMOS technologies. Therewith, the advantages of a signal representation in the time domain are emphasized. The primary approach to time-to-digital converters (analog TDCs) based on a two step approach translating the time interval into a voltage and this voltage into a digital value is explained. Analog impairments and resolution limitations are examined. Counter based time interval measurement and delay-line based TDCs (digital TDCs) are introduced and analyzed with respect to operating principle, basic implementation issues, and quantization error, i.e. resolution.

Key words: Basic Time-to-Digital Converter, Analog TDC, Digital Delay-Line TDC, Mixed-Signal Systems

2.1 Motivation – The Way to the Time Domain

Time-to-digital converters (TDC) – certainly most engineers link this expression with all-digital phase-locked loops (PLL) where a TDC serves as phase detector [34, 51–53]. Interestingly, TDCs have been used for more than 20 years in the field of particle and high-energy physics, where precise time-interval measurement is required [27, 28, 32, 54]. Other applications cover time-of-flight measurement, or measurement and instrumentation applications such as digital scopes and logic analyzers. Currently the micro-electronics community rediscovers time-to-digital converters and this is the justification for a complete book on this topic. While the all digital PLL is the first and most famous TDC application others emerge rapidly. TDC based analog-to-digital converter for instance shows that TDCs are not just phase detectors but useful in a much wider field [8, 48]. Of course the requirements for any micro-electronics application differ from the applications mentioned above with respect to acceptable price, reproducibility, and suitability for mass production. These issues will be discussed in detail throughout the book. At this point

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the motivating question shall be discussed why TDCs suddenly become popular in mainstream micro-electronics: Modern VLSI technology is mainly driven by digital circuits. The reasons for this are the many advantages of digital compared to analog circuits: Atomic digital functions can be realized by very small and simple circuits. This results in a compact and cheap implementation of elementary logic functions and enables complex and flexible signal processing systems. A comparable complexity was not feasible with an analog implementation due to area and power consumption but also due to variability and signal integrity. Flexible means reconfigurable, adjustable or even programmable. Data can be stored easily in digital systems without any loss of information. The design of digital circuits is highly automated resulting in high design efficiency and productivity. However, the main advantage of digital signal processing is the inherent robustness of digital signals against any disturbances, i.e. noise and coupling, as well as the inherent robustness of digital circuits against process variations. Both signal integrity and variability in digital circuits are heavily discussed in technical literature during the last years. It is true that these are critical issues especially for large chips fabricated in ultra deep sub-micron technologies. But compared to analog realizations digital solutions are still by far more robust. As a consequence of all these advantages most digital signal processing systems are realized according to the generic structure depicted in Fig. 2.1. A small mixed-signal shell provides the interface between the digital core and the environment which is always analog.[1] While the mixed-signal interface is mainly responsible for the data conversion, the actual signal processing task is performed in the digital domain. In the input path some basic analog signal conditioning, e.g. coarse filters, amplifiers and mixers are followed by a sampler and a quantizer, i.e. an ADC. The sampler evaluates the input signal at discrete time instances and the quantizer maps the resulting continuous values to discrete ones. Both together result in a digital signal representation. In the output path the digital values provided by the signal processing core at discrete time instances are converted in voltages/currents and held constant until the next value occurs. An optional analog low pass filter removes the (sinc-filtered) mirror spectra and provides smooth output signals.

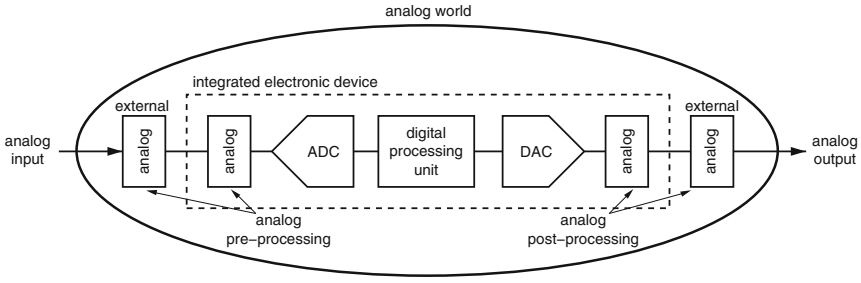

Fig. 2.1 Generic digital signal processing system comprising a digital core embedded in a mixed-signal shell for interfacing with the analog environment

[1] In fact even interfaces with digital functionality are analog. Digital signal transmission over high-speed serial links for instance poses lots of analog challenges, which become obvious on the lower abstraction levels.

But what has all of this to do with time-to-digital converters? What is the problem with this generic structure that has been successfully used for so many years? The difficulties arise from technology scaling in the ultra deep sub-micron regime: With each technology generation the intrinsic gain of a single MOS transistor namely the $\frac{g_m}{g_{ds}}$ decreases. This does not only result from parasitic short channel effects but is a fundamental result from MOS physics.[2]

In principle there are classical countermeasures to cope with decreasing transistor gain. Cascode transistors, for instance, increase the output resistance of basic amplifiers, current mirrors, and active loads dramatically, but cause at least one V_{Dsat} in the DC voltage budget. With the reduced supply voltages of scaled technologies there is often not enough voltage headroom to use cascodes. But even though this is possible, the speed of the circuit and the signal swing is reduced. The latter effect is particularly disadvantageous because of the reduced signal-to-noise ratio (SNR). In general technology scaling comes with a reduction in supply voltage and so reduced signal levels. As noise does not scale the SNR in the voltage domain is reduced in proportion to V_{DD}^2.

Altogether, the design of classical mixed-signal circuits becomes increasingly difficult. This rises two questions: First we have to check whether the mixed-signal content of modern signal processing systems is really reduced to a minimum. Second we have to answer why classical mixed-signal systems have that bad scaling behavior. In many systems mixed-signal circuits are just used for interfacing, so the first question can be approved. However, digital enhancement techniques within the mixed-signal building blocks, e.g. calibration techniques can help to improve the performance considerably. This means that the mixed-signal content of the generic system in Fig. 2.1 is minimized, but that the mixed-signal blocks themselves could be flavored with additional digital enhancement techniques.

The second question can be answered by considering the strengths of technology scaling. Although the main benefit of scaling in the deep sub-micron regime is the area reduction, there is still a speed improvement. This effect becomes smaller especially in low-power technologies, but continues to push digital performance. Despite increasing leakage currents [13] the power also scales to some extend. Good scaling behavior is thus achieved for all systems that take advantage of the fast digital switching speed. The reduction of the gate delay results in continuously improving temporal resolution which is contrary to the amplitude resolution [53]. Therewith, there is no principal restriction of mixed-signals blocks in aggressively scaled technologies but the problem is the signal representation in the voltage domain. An implementation of the same functionality in the time-domain would immediately take advantage of technology scaling again. The enabler for the time-domain processing of continuous signals is the time-to-digital converter. With this key building block a transformation of classical mixed-signal systems with a signal representation in the voltage domain is possible. This final rush for digitalization has just started.

[2] The channel length modulation coefficient $\lambda = \frac{1}{V_E L}$ is inverse proportional to the channel length L and the Early voltage V_E. The channel length scales considerably faster than V_E so the dependence of the drain current on the drain-to-source voltage increases with technology scaling [50].

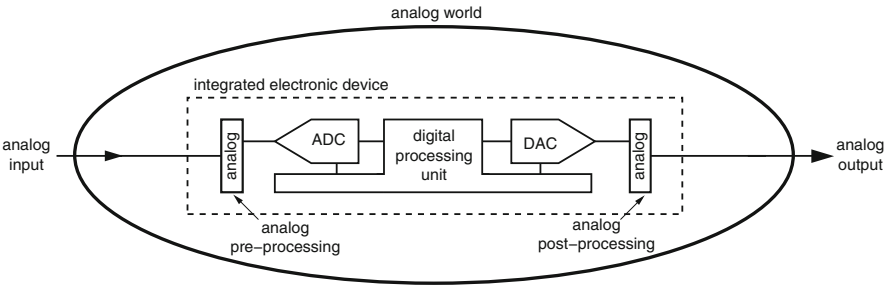

Fig. 2.2 Future digital signal processing system where the mixed-signal shell is heavily flavored with digital enhancement techniques that help to cope with the impairments of analog circuits in the deep sub-micron CMOS technologies

During the next years the amount of classical mixed-signal circuitry will be further reduced. The remaining mixed-signal components will be heavily supported by digital enhancement techniques and digital post-processing of imperfect data (ref. Fig. 2.2). Non-idealities due to analog impairments will be corrected by digital signal processing. For sure this is no digitalization in a VHDL or Verilog sense but a conversion of the continuous voltage domain into the continuous time domain. A substantiated expert knowledge in transistor level circuit design will still be the essential basis to cope with the increasing challenges in deep sub-micron CMOS technologies.

2.2 Analog Time-to-Digital Converters – The First Generation

The traditional approach to time-to-digital conversion is first to convert the time interval into a voltage. In a second step this voltage is digitized by a conventional analog-to-digital converter (ADC). A basic block diagram is given in Fig. 2.3. The start and the stop event are used to form a pulse with a width corresponding to the time interval to be measured. An analog integrator transforms this pulse into a voltage which is then fed to the ADC. A fundamental trade-off between the dynamic range DR, i.e. the maximum time interval to be measured and the maximum number of bits N the ADC can accomplish is revealed by the following equation:

$$DR = 2^N \cdot T_{LSB} \tag{2.1}$$

The minimum time interval that can be resolved is given by T_{LSB}. As the maximum resolution of the ADC is limited by analog constraints a long measurement interval means low resolution and vice versa. A high resolution measurement of long time intervals requires a two stage approach, i.e. a coarse quantization of the long time interval and a fine quantization of the remainder. Another approach is to integrate up and down periodically. The number of periods gives a coarse quantization and the

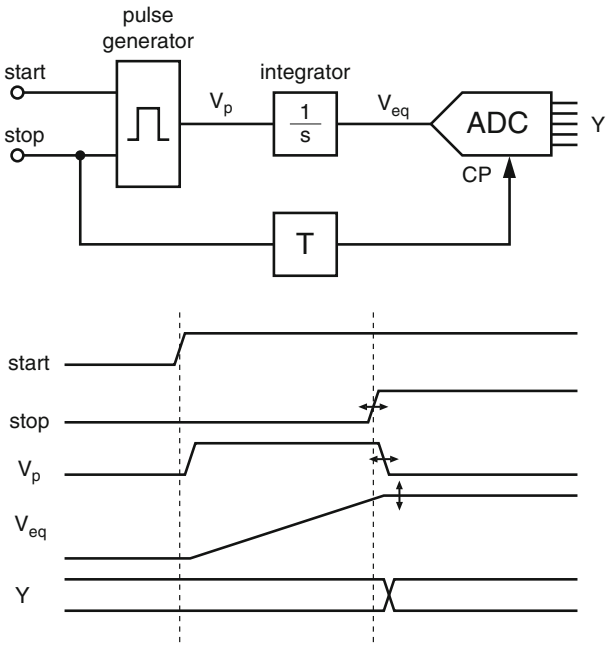

Fig. 2.3 Block and signal diagram of basic analog time-to-digital converter, e.g. [32, 42]

analog voltage level can be converted by the ADC to achieve a high resolution. We will see later in this book that the limitation given by eq. 2.1 does not exist for digital TDCs which is a great advantage over ADCs. There are also multi-stage approaches for digital TDCs (ref. Section 4.5) but the motivation behind this is the reduction of area and power.

Although the conversion principle in Fig. 2.3 is quite simple there are several analog issues that degrade the TDC performance: All building blocks, i.e. the pulse generator, the integrator, and the ADC have to meet the full linearity demands of the overall TDC. A basic integrator implementation that allows for high-speed, i.e. short measurement intervals, is a current source which is connected to an integration capacitance during the measurement interval. Due to the finite output resistance of the current source the linearity is weak. To overcome this problem an active RC-integrator may be used. As the potential at the virtual ground is nearly constant the linearity is improved. However, the finite bandwidth of the operational amplifier (opamp) limits the speed and so the minimum time interval considerably.

Absolute time measurement requires the knowledge of the current and the capacitance value. For integrated TDC implementations this is not feasible without calibration. A more elaborate TDC approach which does not require the knowledge of absolute device values is shown in Fig. 2.4. An exemplary signal diagram is given in Fig. 2.5. Again the pulse defined by the start and the stop signals is integrated. On the arrival of the stop signal a second integrator starts integrating but with a

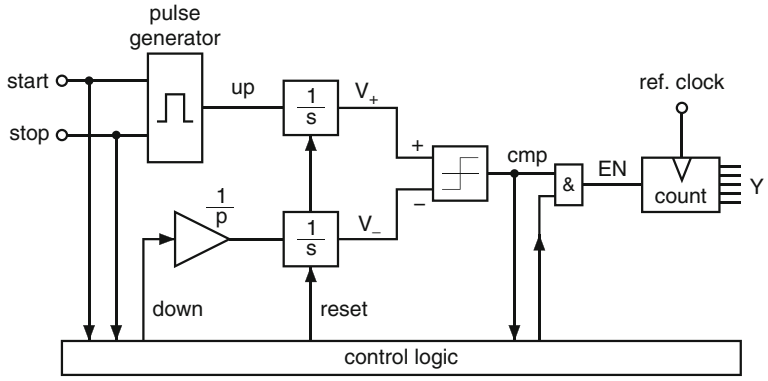

Fig. 2.4 Blockdiagram of analog TDC based on dual-slope analog-to-time-interpolation [43]

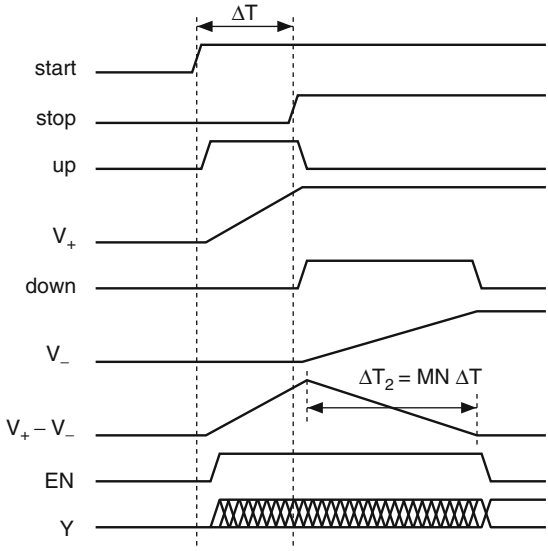

Fig. 2.5 Basic signal diagram of analog time-to-digital converter based on dual-slope analog-to-time interpolation. By means of pulse stretching the initial time interval ΔT is converted into a digital representation

reduced integration constant $\frac{1}{p}$. A comparator detects when the output of the second integrator is equal to the first one. This happens $(1+p)\Delta T$ seconds after the start event. The initial time interval ΔT is stretched by the factor $(1+p)$. Therefore this dual-slope approach is also known as time amplification. If p is large enough the enlarged time interval may be quantized by a simple digital counter.

In principle the dual-slope TDC is a reversed dual-slope analog-to-digital converter. In a dual-slope ADC an unknown analog signal is integrated for a well defined time. In the dual-slope TDC a well defined voltage namely the pulse height is

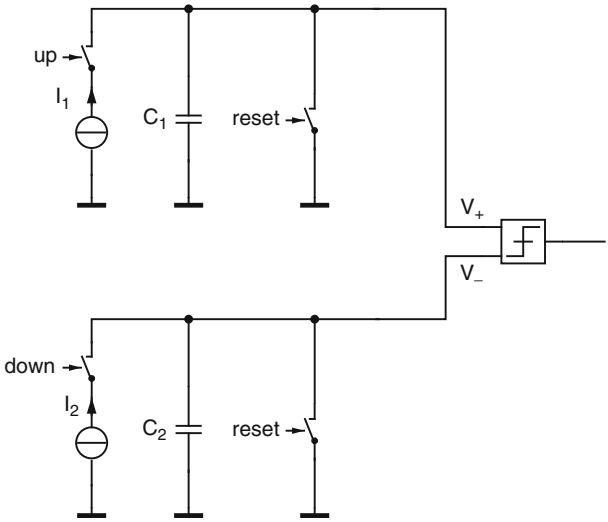

Fig. 2.6 Schematic circuit diagram of a basic dual-slope TDC [43]

integrated for the unknown time interval ΔT. In both cases the output voltage of the integrator after the first phase is integrated down by a predefined rate until a reference level is reached and a basic counter measures the required time. A major advantage of the dual-slope with respect to the basic single-slope ADC is the fact that absolute device values cancel out. The same should hold for the dual-slope TDC: To demonstrate this, the implementation in Fig. 2.6 is considered. At the beginning both capacitances C_1 and C_2 are discharged by the reset devices. During the time interval ΔT a first current source is connected to C_1. Assuming a perfect current source, the voltage V_+ increases linearly and reaches a final value given by $V_+ = \frac{I_1}{C_1}\Delta T$. On the arrival of the stop signal C_1 becomes floating and C_2 is connected to a second current source I_2. The voltage V_- across C_2 is given by $V_- = \frac{I_2}{C_2}\Delta T_2$ where ΔT_2 is the time elapsed since the stop event has occurred. The comparator connected to both capacitors detects when the two voltages V_+ and V_- are equal. This happens a time interval

$$\Delta T + \Delta T_2 = \left(1 + \frac{C_2}{C_1}\frac{I_1}{I_2}\right)\Delta T \tag{2.2}$$

after the start event. With a capacitance ratio $M := \frac{C_2}{C_1}$ and a current ratio $N^{-1} = \frac{I_2}{I_1}$ the initial time interval is stretched (amplified) by a factor $(1 + M \cdot N)$. As both factors M and N are ratios of physical quantities namely capacitances and currents the absolute values are not relevant. This makes the dual-slope approach very robust against process variations and enables an integration without the need for calibration. The fact that both ratios are multiplied is also advantageous for integration as large stretching factors can be realized even without unreasonably large capacitance or current ratios.

2.3 Fully Digital TDCs – The Second Generation

If the motivation for a TDC was just to implement a precise timer, an analog approach like one of those discussed in the previous section would be enough. However, the strategy to provide TDCs as generic mixed-signal building blocks for various applications rises questions about the suitability in ultimately scaled CMOS technologies. In Section 2.1 the advantages of time domain signal processing and the superior scaling properties of TDCs have been emphasized. Obviously this does not hold for any analog TDC which converts time domain information first into the analog and then to the digital domain. Such TDCs consist mainly of an ADC so have all the impairments of analog circuits in deep sub-micron technologies. The advantages of the time domain can be exploited only if there is no analog conversion step in the time-to-digital conversion. Only if the TDC is clearly dominated by digital circuitry the scaling and robustness arguments hold. Therefore, digital conversion techniques are investigated in the remainder of this book: The simplest technique to quantize a time interval is to count the cycles of a reference clock fitting into the respective measurement interval. As shown in Fig. 2.7 the measurement interval defined by the start and stop signal is completely asynchronous to the reference clock signal. This causes a measurement error ΔT_{start} at the beginning and ΔT_{stop} at the end of the time interval. The measurement interval ΔT can be expressed as

$$\begin{aligned} \Delta T &= N \cdot T_{CP} + (T_{CP} - \Delta T_{stop}) - (T_{CP} - \Delta T_{start}) \\ &= N \cdot T_{CP} - \Delta T_{stop} + \Delta T_{start} \\ &= N \cdot T_{CP} + \varepsilon_T \end{aligned} \tag{2.3}$$

$$\begin{aligned} \Delta T_{start} &\in [0; T_{CP}] \\ \Delta T_{stop} &\in [0; T_{CP}] \\ \varepsilon_T &= \Delta T_{start} - \Delta T_{stop} \in [-T_{CP}; T_{CP}] \end{aligned} \tag{2.4}$$

where N is the counter value and T_{CP} the reference clock period. ΔT_{start} and ΔT_{stop} are the time intervals between the start and the stop signal, respectively, and the next rising edge of the clock signal. The quantization error of the ΔT measurement is between $-T_{CP}$ and $+T_{CP}$, i.e. is limited to twice the period of the clock signal.

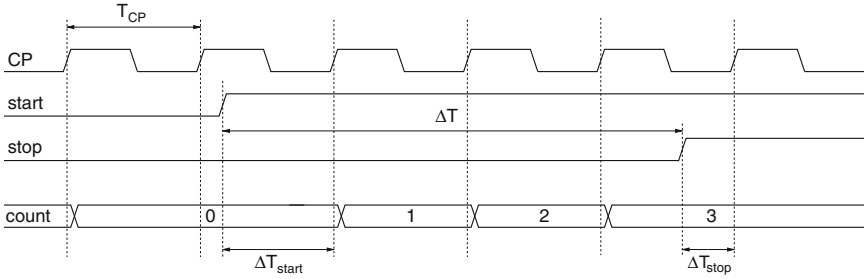

Fig. 2.7 Principle of counter based TDC

The measurement accuracy can be increased by a higher clock frequency. However, the higher the clock frequency the higher the power consumption for the generation and the processing of the clock signal. Above a certain clock frequency (corresponding to 3–4 FO2 inverter delays[3]) CMOS based oscillators are not available anymore, so even more expensive CML or LC oscillators are required for the clock generation. Timing restrictions in the counter as well as in the controller circuit pose another limit on the maximum frequency. In a 65 nm technology for instance the maximum frequency is limited to 5–10 GHz, i.e. a maximum measurement accuracy of $2 \cdot 100$–200 ps may be achieved.

An even higher resolution is achieved by subdividing one clock period asynchronously into smaller time intervals. The engine that performs this subdivision is actually what we call a digital time-to-digital converter. Hence, the resolution is the criterion that distinguishes a counter from a TDC. The measurement interval quantized with a TDC can be described by

$$\Delta T = NT_{CP} - (T_{CP} - \Delta T_{start}) + (T_{CP} - \Delta T_{stop}) \tag{2.5}$$

$$\Delta T_{start} = N_1 \frac{T_{CP}}{k} - \varepsilon_1 \tag{2.6}$$

$$\Delta T_{stop} = N_2 \frac{T_{CP}}{k} - \varepsilon_2 \qquad \varepsilon_1, \varepsilon_2 \in \left[0; T_{LSB} = \frac{T_{CP}}{k}\right] \tag{2.7}$$

$$\Delta T = NT_{CP} + N_1 \frac{T_{CP}}{k} - \varepsilon_1 - N_2 \frac{T_{CP}}{k} + \varepsilon_2 \tag{2.8}$$

$$\varepsilon_T = \varepsilon_2 - \varepsilon_1 \in \left[-\frac{T_{CP}}{k}; \frac{T_{CP}}{k}\right] \tag{2.9}$$

where the resolution $T_{LSB} = \frac{T_{CP}}{k}$ is increased by the factor k. The interpolation factor k describes in how many sub-intervals the reference clock cycle is partitioned, N_1 and N_2 indicate the position of the start and the stop event within such a reference clock cycle. The subsequent chapters describe the basic concepts of digital time-to-digital converters and explain how a higher resolution can be achieved even without a higher reference clock frequency.

2.4 Basic Digital Delay-Line Based TDC

To increase the measurement resolution beyond the maximum feasible clock frequency each counter clock cycle has to be sub-divided asynchronously by a time-to-digital converter. Figure 2.8 illustrates that the counter value then provides a coarse quantization of the measurement interval and the TDC a fine sub-quantization [37]. The subdivision of the reference clock interval, also known as reference clock

[3] FO2 refers to the fan-out of two inverter delay, i.e. to the delay of an inverter that is loaded with twice its input capacitance.

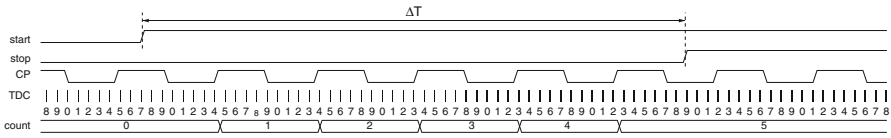

Fig. 2.8 Principle of a counter based TDC where the resolution is increased by subdividing one clock interval asynchronously into smaller time intervals [37]

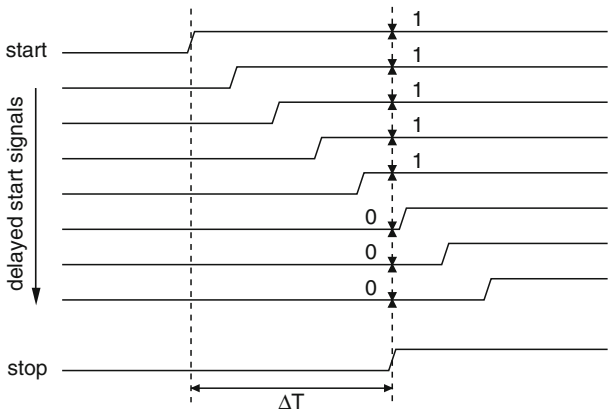

Fig. 2.9 Operating principle of a time-to-digital converter. Delayed versions of the start signal are sampled on the rising edge of the stop signal, resulting in a thermometer code at the outputs of the sampling elements (flip-flops or comparators)

interpolation, is done by using multiple phases of the reference clock. For a small interpolation factor, i.e. medium resolution, the phases may be directly derived from the oscillator which generates the reference clock. A ring oscillator consisting of k delay stages for instance generates k equally spaced versions of the clock signal. An even higher resolution is achieved by delaying the original reference clock in a chain of digital delay elements. The resolution then depends on the delay of the delay elements in the chain. Figure 2.9 illustrates the operating principle of a TDC based on a digital delay-line. The reference clock which is in a more general sense an arbitrary start signal is delayed along the delay-line. On the arrival of the stop signal the delayed versions start_i of the start signal are sampled in parallel. Either latches or flip-flops can be used as sampling elements. The sampling process freezes the state of the delay-line at the instance where the stop signal occurs. This results in a thermometer code because all delay stages which have been already passed by the start signal give a HIGH value at the outputs of the sampling elements, all delay stages which have not been passed by the start signal yet give a LOW value. The position of the HIGH-LOW transition in this thermometer code indicates how far the start signal could propagate during the time interval spanned by the start and the stop signal. Hence this transition is a measure for the time interval. The number N

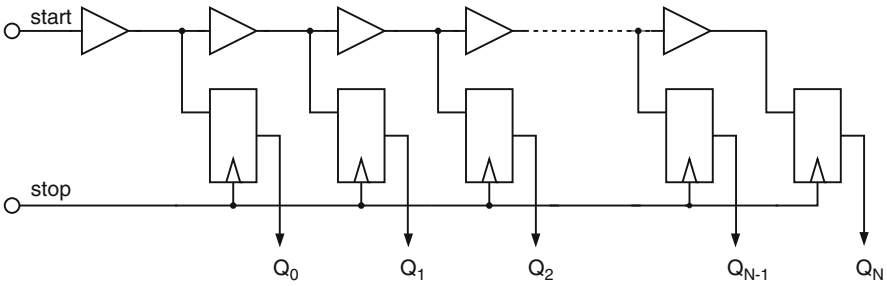

Fig. 2.10 Implementation of a basic delay-line based time-to-digital converter (DL-TDC)

of all sampling elements with a HIGH output is related to the measurement interval ΔT according to

$$N = \left\lfloor \frac{\Delta T}{T_{LSB}} \right\rfloor \tag{2.10}$$

where T_{LSB} is the delay of a single delay element in the delay-line. The time interval ΔT can be calculated from the number of HIGH outputs by

$$\Delta T = NT_{LSB} + \varepsilon \tag{2.11}$$

where ε describes the quantization error that arises as a delay element has been either passed by the start signal yet or not. Any intermediate state is not possible. The quantizer characteristic of a TDC and its non-idealities are discussed in Chapter 3 extensively.

An implementation of the basic delay-line TDC is shown in Fig. 2.10. The start signal ripples along a buffer chain that produces the delayed signals start_i. Flip-flops are connected to the outputs of the delay elements and sample the state of the delay-line on the rising edge of the stop signal. The stop signal drives a high number of flip-flops so a buffer-tree (not shown) is required. Any skew in this buffer-tree directly contributes to the non-linearity of the TDC characteristics. For a correct thermometer code the skew between adjacent branches in this tree has to be smaller than T_{LSB} which makes the design challenging.

2.4.1 Inverter Based Time-to-Digital Converter

The resolution of the delay-line based TDC discussed in the previous section is limited by the delay of the buffers. The resolution can be doubled by replacing the buffers by CMOS inverters. This, however, rises some implementation challenges which will be discussed next: The use of inverters means that both the rising and the falling signal transitions are used for measurement. Hence the thermometer code

at the outputs of the sampling elements becomes a pseudo thermometer code with alternating ones and zeros:

111111111111111 ⌋⌈ 000000000000000	buffer TDC
010101010101010 ⌋⌈ 010101010101010	inverter TDC

The length of the measurement interval is indicated not by a HIGH-LOW transition but by a phase change of the alternation HIGH-LOW sequence.

In principle the delays for a rising and a falling transition of a CMOS inverter are different and only partially correlated. There is some correlation due to common process steps during manufacturing of NMOS and PMOS devices. Examples for such process steps are the formation of the gate oxide and the gate lithography. However, there are also completely independent process steps such as the ion implantation for threshold voltage adjustment. This leads to systematic non-linearity of the converter characteristic. For nominal process conditions the rise and the fall delay can be made equal but any process variation imbalances the delays again. An even stronger effect has the asymmetric setup time of basic sampling elements such as master slave latch pairs. Hence, a high-resolution TDC based on a single inverter delay chain seems to be not feasible if process variations become significant. Figure 2.11 shows a robust inverter based TDC. Fully symmetrical differential flip-flops such as sense amplifier based flip-flops are used as sampling elements. Two delay chains propagate the start as well as the inverted start signal and provide differential data to the flip-flops. The inverting characteristics of the CMOS inverters is compensated by twisting the input signals of the flip-flops in each second stage. This compensates completely for the potential asymmetric setup time of the flip-flops and asymmetric rise and fall delays of the inverters. Local process variations may cause a faster signal propagation in one delay-line compared to the other. Coupling elements such as cross coupled inverter pairs in between two corresponding

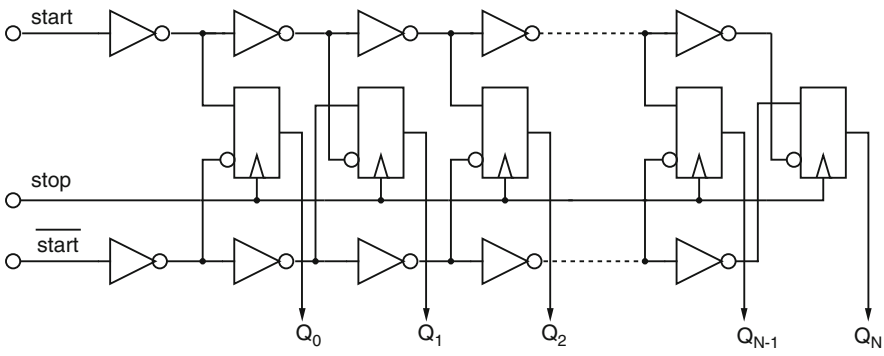

Fig. 2.11 Time-to-digital converter based on inverters instead of buffers. The resolution is doubled with respect to the implementation given in Fig. 2.10

Table 2.1 Performance summary of buffer and inverter delay-line TDC. The performance figures are introduced in the following chapter. However, for comparability with the results presented in Chapter 4 this table is already presented here

	Buffer Delay-Line TDC	Inverter Delay-Line TDC
Principle	Start signal propagates in linear chain of buffers. On the arrival of a stop signal the state of the delay-line is sampled by flip-flops/comparators	Differential start signal propagates in two coupled chains of inverters. On the arrival of a stop signal the state of the delay-line is sampled by (differential) flip-flops/comparators
Resolution T_{LSB}	$t_d^{buffer} = 2t_d^{inv}$	t_d^{inv}
Number of Stages N	$\frac{T_{max}}{T_{LSB}} = \frac{T_{max}}{t_d^{buffer}} = \frac{T_{max}}{2t_d^{inv}}$	$\frac{T_{max}}{T_{LSB}} = \frac{T_{max}}{t_d^{inv}}$
Core Area $A_{core}^{Vernier}$	$\frac{T_{max}}{T_{LSB}}\left(2A^{inv} + A^{FF}\right)$	$\frac{T_{max}}{T_{LSB}}\left(2.2A^{inv} + A^{FF}\right)$
Average Power $\langle P_{vernier}^{core} \rangle$	$f_{meas}\frac{T_{max}}{T_{LSB}}\left(2E_{rise}^{inv} + 2E_{fall}^{inv} + E^{FF}\right)$	$f_{meas}\frac{T_{max}}{T_{LSB}}\left(2.2E_{rise}^{inv} + 2.2E_{fall}^{inv} + E^{FF}\right)$ The factor 2.2 accounts for the overhead required to couple the two delay-lines (differential)
Conversion Time T_{conv}	T	T
Latency $T_{latency}$	0	0
Loop Structure	loop possible	loop possible
PROS	• Simple • Fully digital • Low power • Low latency • Easy control and embedding	• Same as for buffer TDC • Doubled resolution
CONS	• Low resolution • Resolution limited by technology	• Alignment of delay-lines • Resolution limited by technology • Doubled number of comparators for same dynamic range

delay elements reduces this drifting of the signals. However, there is still a very regular and symmetrical layout required for the two delay-lines. This is probably the most challenging task for an actual TDC implementation (Table 2.1).

2.5 Synchronous Versus Asynchronous Time Interval Measurement

Synchronous time interval measurement based on a coarse pre-quantization by a reference clock and a fine quantization with a TDC (ref. Fig. 2.8) has the fundamental drawback that the reference clock jitter deteriorates the measurement accuracy. This can be seen by rewriting eqs. 2.5–2.8 with a jitter term:

$$\Delta T = NT_{CP} - (T_{CP} - \Delta T_{start}) + (T_{CP} - \Delta T_{stop}) \tag{2.12}$$

$$\Delta T_{start} = N_1 \frac{T_{CP}}{k} - \varepsilon_1 + t_{jitter,1} \tag{2.13}$$

$$\Delta T_{stop} = N_2 \frac{T_{CP}}{k} - \varepsilon_2 + t_{jitter,2} \qquad \varepsilon_1, \varepsilon_2 \in \left[0; T_{LSB} = \frac{T_{CP}}{k}\right] \tag{2.14}$$

$$\Delta T = NT_{CP} + N_1 \frac{T_{CP}}{k} - \varepsilon_1 + t_{jitter,1} - N_2 \frac{T_{CP}}{k} + \varepsilon_2 - t_{jitter,2} \tag{2.15}$$

The jitter is a mean free not necessarily gaussian random variable characterized by its rms value σ_{jitter}. It can be seen that two partly independent jitter contributions add to the measurement uncertainty statistically. For short and medium time intervals it may be advantageous to abdicate the reference clock and to use a longer TDC. Therewith the measurement error caused from reference clock jitter vanishes. The start and stop signals for the TDC are directly extracted from the measurement pulse and not referred to any clock (asynchronous time interval measurement). The TDC has to be able to measure the complete time interval not just a reference clock period, i.e. the delay chain has to be long enough or an advanced TDC architecture like the looped TDC (ref. Section 4.2) has to be used. Of course there is also noise in the TDC which translates into a deviation of the switching instances of the delay elements from the ideal time instances and a variation of the sampling instance. The resulting measurement uncertainty increases with $\sqrt{T}$ where T is the length of the measurement interval. Hence for long measurement intervals the intrinsic timing uncertainty of the TDC may be larger than the reference clock jitter. For an actual design and a required measurement time the intrinsic TDC noise and the quality of a possible reference clock generator must be compared. Thereupon it can be decided whether a synchronous or asynchronous approach is preferable. Beside the noise the availability of the clock signal is another criterion as an additional clock PLL contributes considerably to the overall power consumption and die area.

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