Introduction to VME

Laboratory for Data Acquisition and Controls

Last modified on 16-Oct-23 14:54

VMEbus

VMEbus is a computer architecture

VME = Versa Module Eurocard – 1980

Bus is a generic term describing a computer data path

Bus usage was developed from a computing point of view ⇒ completely memory mapped scheme

Every device can be viewed as an address, or block of addresses

Addresses and data are not multiplexed

Crate and Module

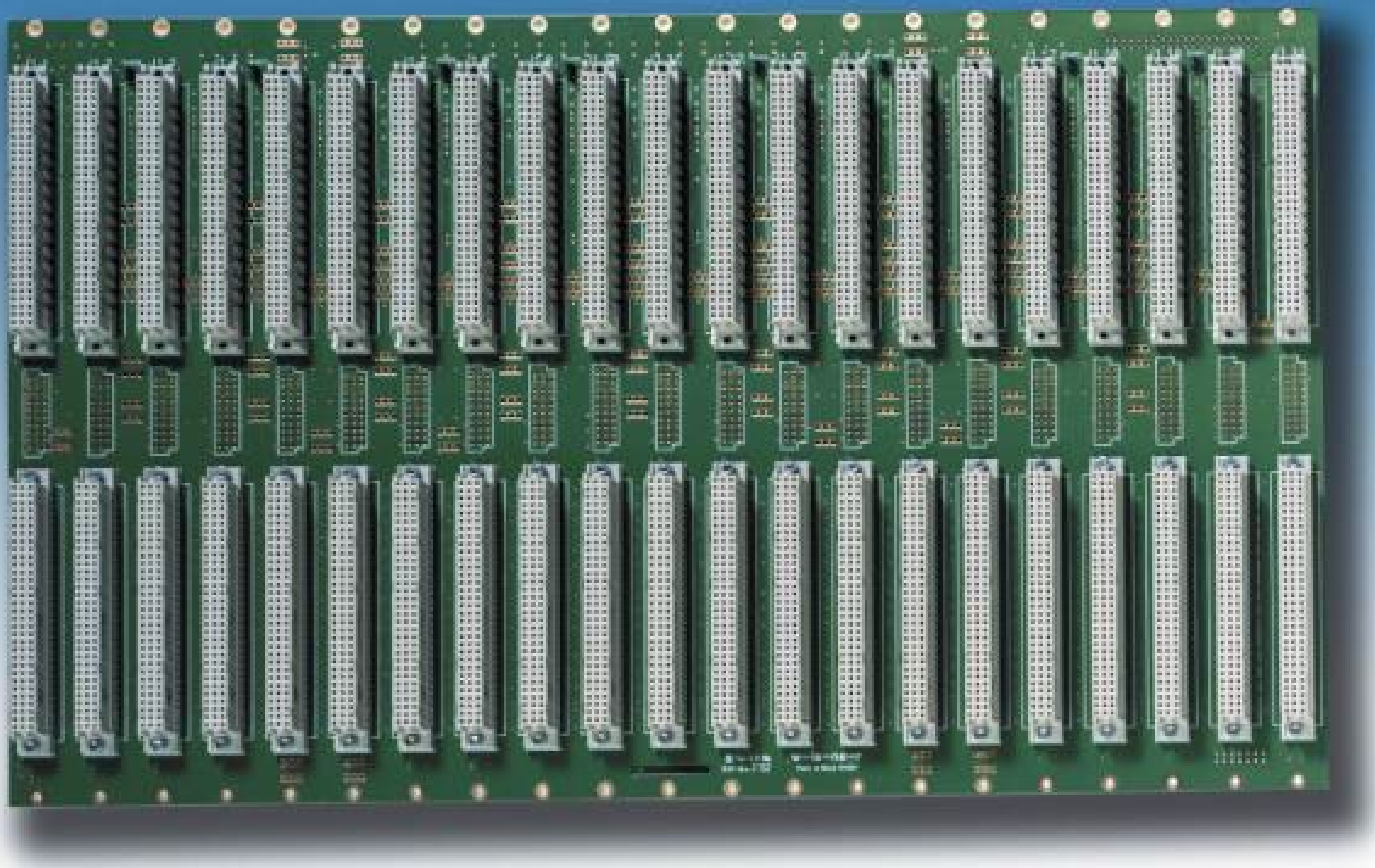
The system is modular (Eurocard standard)

VME: card cages (21 slots) and card (160x216mm 160x100mm)

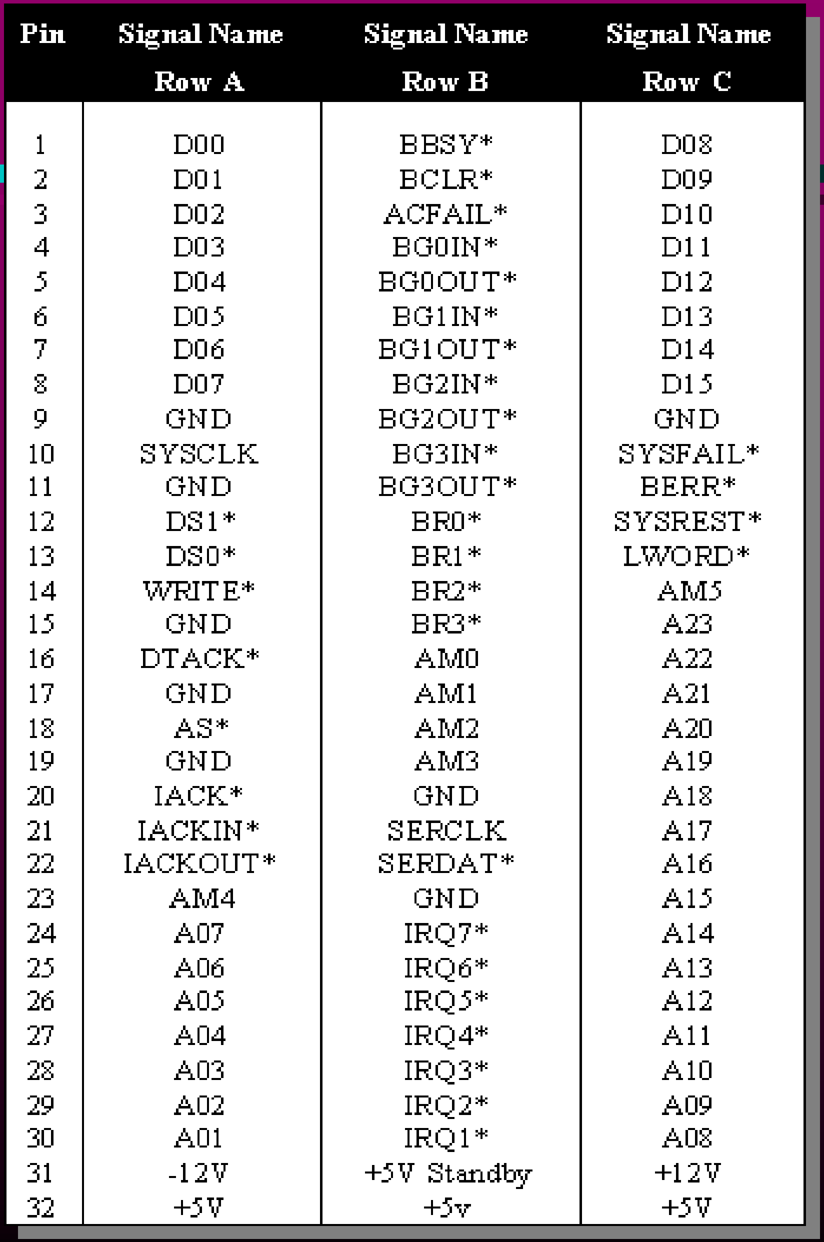
Cards capable of data path widths 8, 16, 24, 32, 64 bit
Addressing range between 16, 24, 32, 64 bit

VME boards have P1 connector, larger cards P2 connector (and JAUX…)

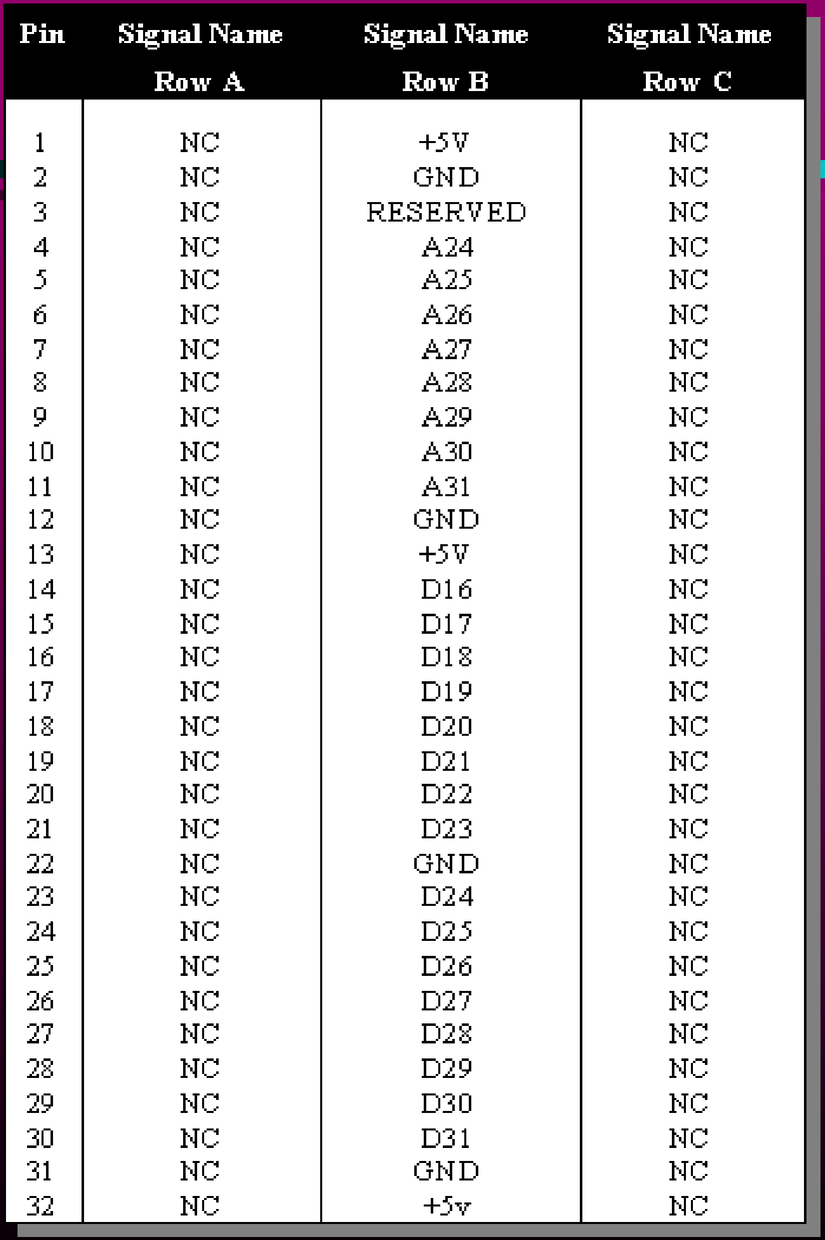
VME Backplane



Pinout: P1 P2



Pin	Signal Name	Signal Name	Signal Name
	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSREST*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V Standby	+12V
32	+5V	+5v	+5V



Pin	Signal Name	Signal Name	Signal Name
	Row A	Row B	Row C
1	NC	+5V	NC
2	NC	GND	NC
3	NC	RESERVED	NC
4	NC	A24	NC
5	NC	A25	NC
6	NC	A26	NC
7	NC	A27	NC
8	NC	A28	NC
9	NC	A29	NC
10	NC	A30	NC
11	NC	A31	NC
12	NC	GND	NC
13	NC	+5V	NC
14	NC	D16	NC
15	NC	D17	NC
16	NC	D18	NC
17	NC	D19	NC
18	NC	D20	NC
19	NC	D21	NC
20	NC	D22	NC
21	NC	D23	NC
22	NC	GND	NC
23	NC	D24	NC
24	NC	D25	NC
25	NC	D26	NC
26	NC	D27	NC
27	NC	D28	NC
28	NC	D29	NC
29	NC	D30	NC
30	NC	D31	NC
31	NC	GND	NC
32	NC	+5v	NC

VMEbus

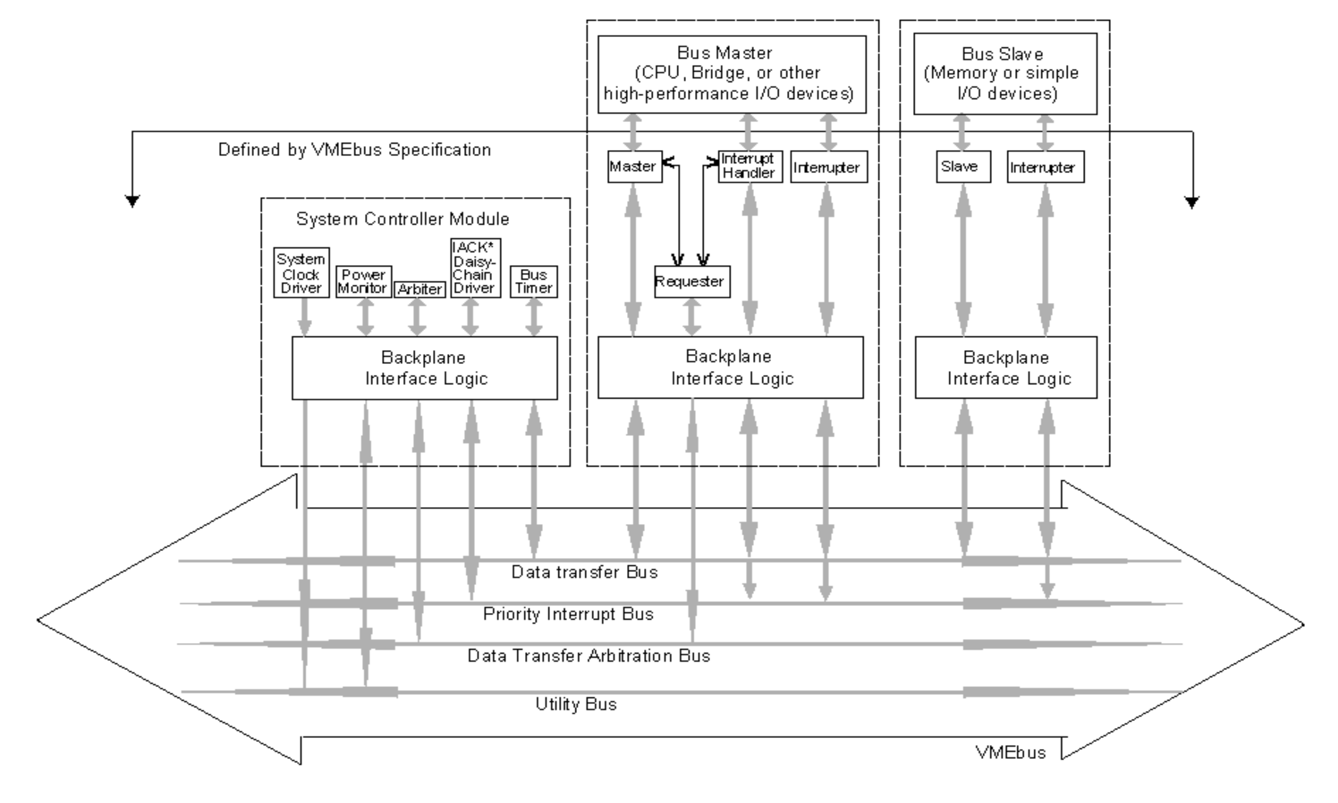
Master/Slave architecture - Asynchronous system
Interrupt scheme

The bus allows multiple masters
A resource manager is required to handle the interrupts

Typical transfer:
an arbitration cycle (to gain bus control)
an address cycle (to select register)
actual data cycle

Read, Write, Modify, Block transfers

Diagram of VMEbus Components



Arbitration bus

*A module controlling the bus will drive the **bus busy line** (**BBSY**) low (IN USE)*

*If not low (NOT IN USE) the arbiter module will sample the **bus request** (**BR0-BR3**) looking for pending action (priority)*

*The arbiter module generates the first **grant signal** and this is passed to modules of increasing slot number (**BG0IN-BG3IN, BG0OUT-BG3OUT**)*

Data Transfer bus

*The **data bus** (**D00-D31**) holds the actual data during a transfer*

*The **address** of the register is presented on the address bus (**A01-A31**)*

*The **address modifier lines** (**AM00-AM05**) indicate the length of the address, the kind of data cycle and master identifier*

*The **address strobe** (**AS**) is used to signal the presence of a valid address*

*The **data strobes** (**DS0,DS1**) are used by the master module to signal valid data and the size word to be transferred*

***WRITE** line is used to distinguish between read and write operations*

*The **data transfer acknowledge** (**DTACK**) is used by the slave module to signal the completion of a transfer*

***Errors** in transfer are signaled using the bus error line (**BERR**)*

Address Information Mnemonics

ADO: Devices with ADO (ADdress Only) capability allow masters to generate and slaves to accept address-only cycles. Using ADO cycles can enhance system performance by allowing simultaneous slave and master memory decoding.

A16: VMEbus masters with A16 capability can generate bus cycles using 16-bit addresses (Short addresses). A16 capable slaves can accept these cycles. A16 addresses are often used as an I/O space.

A24: VMEbus masters with A24 capability can generate bus cycles using 24 bit addresses (Standard addresses). A24 capable slaves can accept these cycles.

A32: VMEbus masters with A32 capability can generate bus cycles using 32-bit addresses (Extended addresses). A32 capable slaves can accept these cycles.

A64: VMEbus masters with A64 capability can generate bus cycles using 64-bit addresses (Long addresses). The 32 data lines are used to supplement the normal address lines in this mode. A64 capable slaves can accept these cycles.

Data Transfer Mnemonics

D08(O): D08(O) capable slaves can accept 8-bit data transfers at odd addresses. All masters must generate D08(O) cycles because they are a subset of the D08(EO) capability. Slaves with D08(O) are most often used on I/O devices with 8-bit integrated circuits.

D08(EO): Masters or slaves with D08(EO) capability can generate or accept 8-bit bus cycles at even or odd addresses (but not simultaneously).

D16: Masters and slaves with D16 capability can generate or accept 16-bit transfers.

D32: Masters and slaves with D32 capability can generate or accept 32-bit transfers.

D64: Masters and slaves with D64 capability can generate or accept 64-bit transfers. Unaligned transfers are not permitted. Thirty-one address lines, 32 data lines and LWORD are used to pass the data.

Data Transfer Mnemonics

RMW: Read-Modify-Write (RMW) capable masters can generate RMW cycles. Slaves can accept them. RMW is primarily used in multiprocessing systems to allow arbitration of shared system resources. It guarantees that the value at the slave cannot be modified between the read and the write cycle.

UAT: An UnAligned Transfer (UAT) can be generated by a master and accepted by a slave. It allows 32 bits of data to be transferred at unaligned address boundaries in two bus cycles instead of three.

BLT : BLock Transfer (BLT) allows a block transfer cycle to be generated by a master or accepted by a slave. This cycle can be faster than normal read/write cycles.

MBLT: Multiplexed BLock Transfer (MBLT), allows a block transfer cycle with 64 bits of data to be generated by a master or accepted by a slave. This cycle is a faster version of the BLT cycle.

DMA (BLT)

Direct Memory Access (DMA): data transfer method to transfer data directly to or from System Memory.

DMA does not use a processor to transfer the data, instead it uses a separate DMA controller. The processor can do other tasks while the device transfers data.

Single Cycle Transfer: each address cycle only allows a single data cycle. Single cycle provides efficient random access to resources, however, DMA is the preferred method for transferring large blocks of consecutive data.

VME two special data transfer modes: BLT and MBLT: they allow a single address cycle and multiple data cycles for each data burst, they are more efficient than single cycle transfers.

BLT mode allows up to 32-bits of data to be transferred each cycle in bursts of up to 256 bytes of data.

MBLT mode, part of the VME64 Specification, allows 64-bits of data to be transferred each cycle in bursts of up to 2048 bytes of data. MBLT mode can transfer 64 bits by multiplexing the 31 address lines and LWORD line on the VMEbus for use as the upper 32-bit data lines.

Multiple data transfers: the master is not required to remove the address, rearbitrate for the bus, and then drive the new address on the bus. The bus slave does not need to decode the address between each data transfer to know that it is being accessed.

Using single cycle transfers, the VMEbus is limited to approximately 8 MBytes/sec. BLT allows data rates up to 40 MBytes/sec. MBLT allows data rates up to 80 MBytes/sec.

VMEbus System Controller Module

The VMEbus System Controller Module contains the system clock driver, power monitor, arbiter, IACK daisy-chain driver, bus timer, and backplane interface logic.

The system clock driver provides a stable 16 MHz utility clock (SYSCLK) to all devices on the bus. The VMEbus is asynchronous and the clock provides no other bus timing.

The power monitor generates system reset (asserts SYSRESET) and monitors the system's AC power source (asserts ACFAIL).

The arbiter monitors requests for the bus and grants control of the bus to one master at a time.

The IACK daisy-chain driver initiates activity on the IACKIN/IACKOUT daisy-chain during an interrupt acknowledge cycle. It makes sure only one interrupter responds and provides the correct timing for the daisy-chain.

The bus timer measures the time it takes for each data transfer. If the transfer takes longer than the time allotted, it asserts BERR to terminate the cycle.

VMEbus System Controller Module Arbitration

PRI: PRIority (PRI) applies to bus arbiters that use a priority scheduling algorithm in which bus requesters on level BR3 have the highest priority. Bus requesters on level BR0 have the lowest priority.

ROR: Bus requesters that have the Release-On-Request (ROR) option relinquish the data transfer bus when it is requested by another VMEbus device.

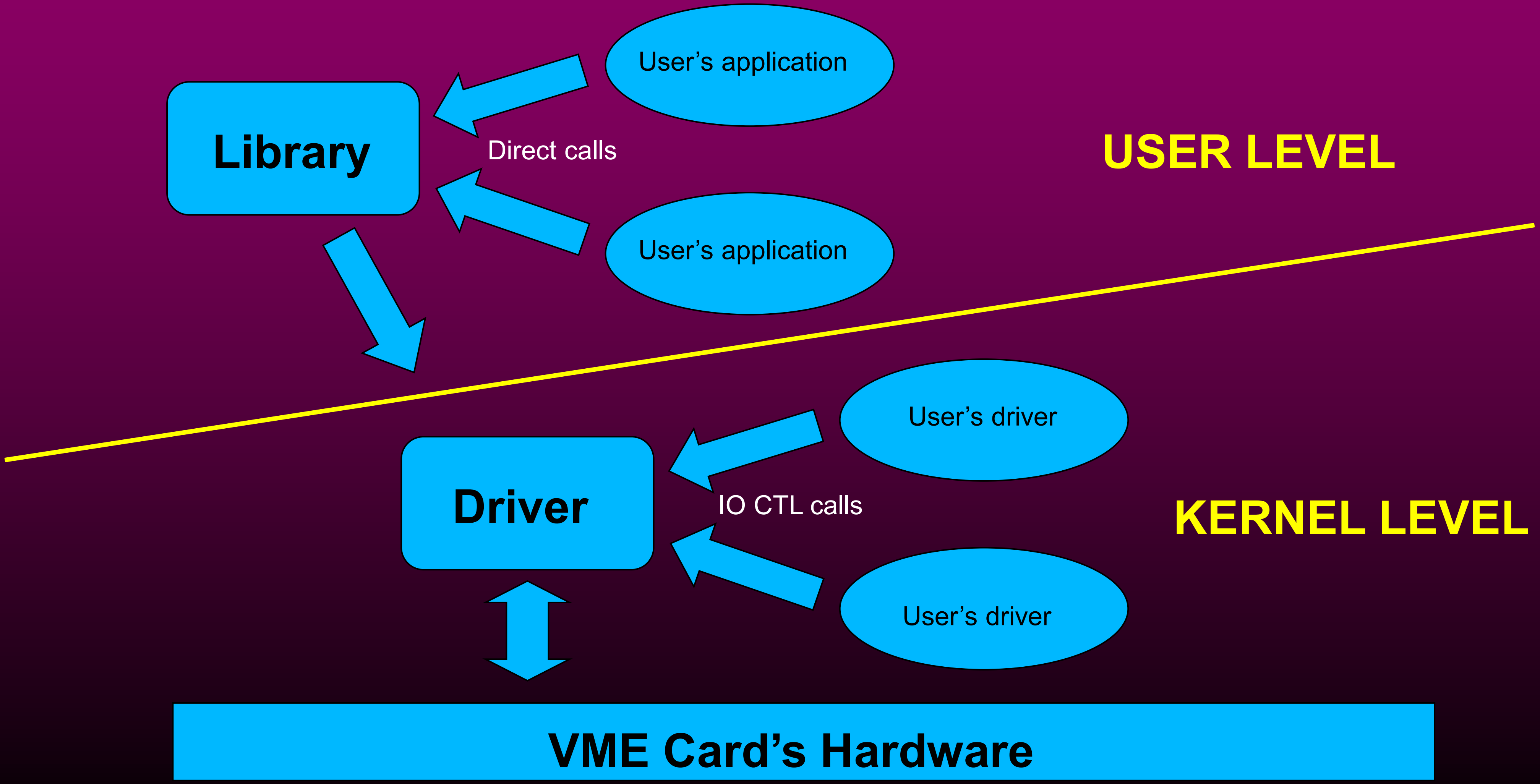
RRS: The Round Robin Select (RRS) option applies to bus arbiters that use a round robin scheduling algorithm in which the bus is granted on a rotating basis. Bus masters and interrupt handlers are granted the bus according to equal priority.

RWD: The Release-When-Done (RWD) option describes a requester that relinquishes the data transfer bus each time it is done using it.

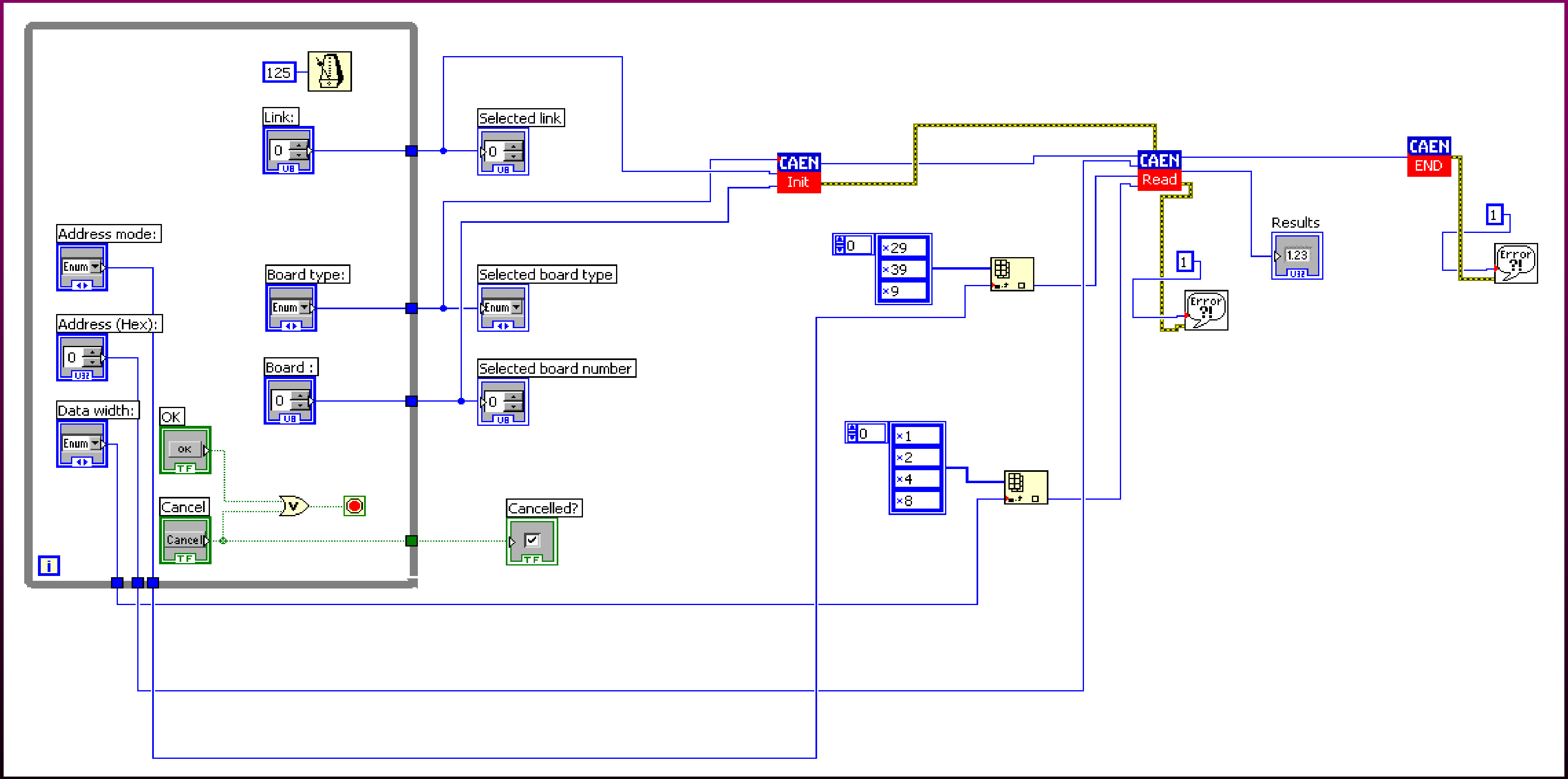
SGL: SinGle-Level (SGL) applies to bus arbiters. SGL arbiters only grant the bus to bus requesters on level three (BR3).

FAIR requester: A requester that provides equal access to all masters requesting the bus on its level. This is done by the requester not requesting the bus again until all other bus masters have released their request.

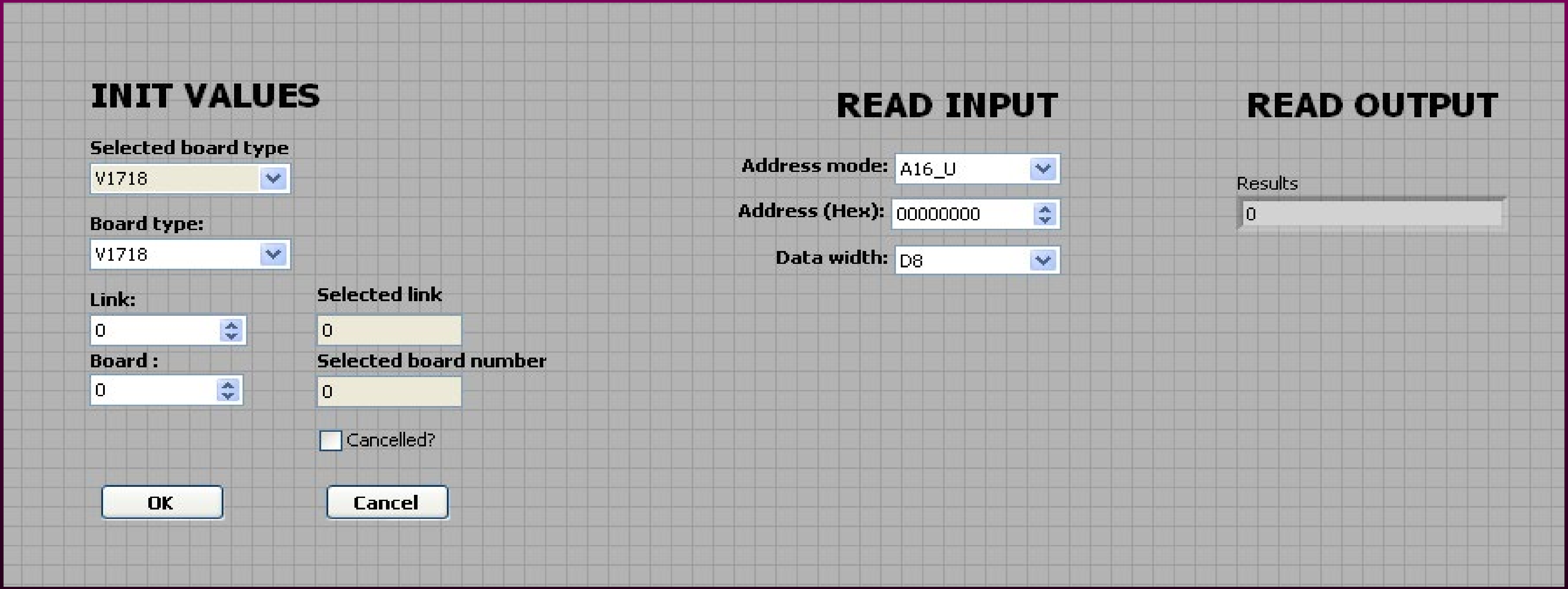
Driver and Library



VME and LabView (read cycle)



VME and LabView (read cycle)



INIT VALUES

Selected board type: V1718

Board type: V1718

Link: 0

Selected link: 0

Board : 0

Selected board number: 0

☐ Cancelled?

READ INPUT

Address mode: A16_U

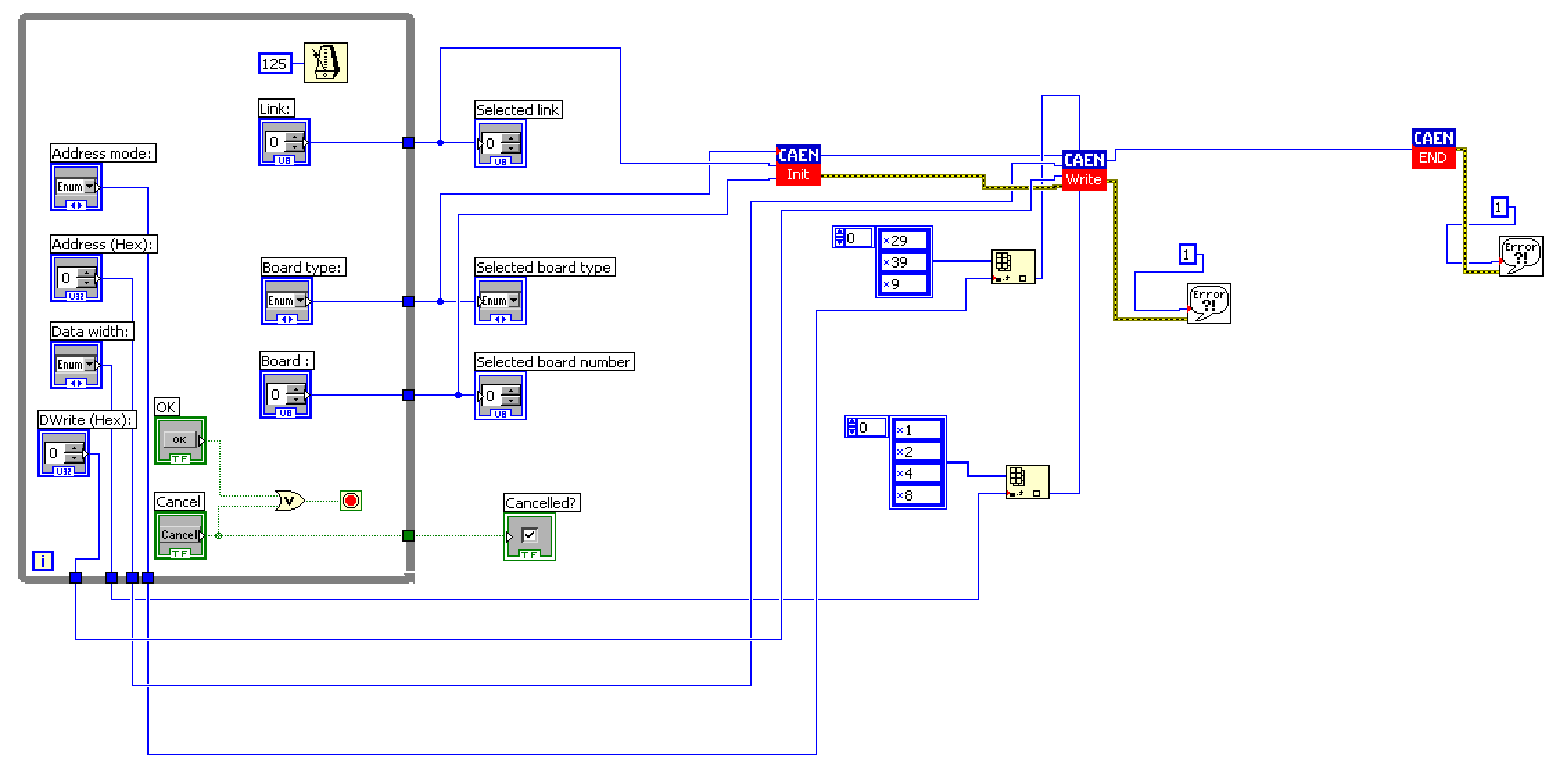
Address (Hex): 00000000

Data width: D8

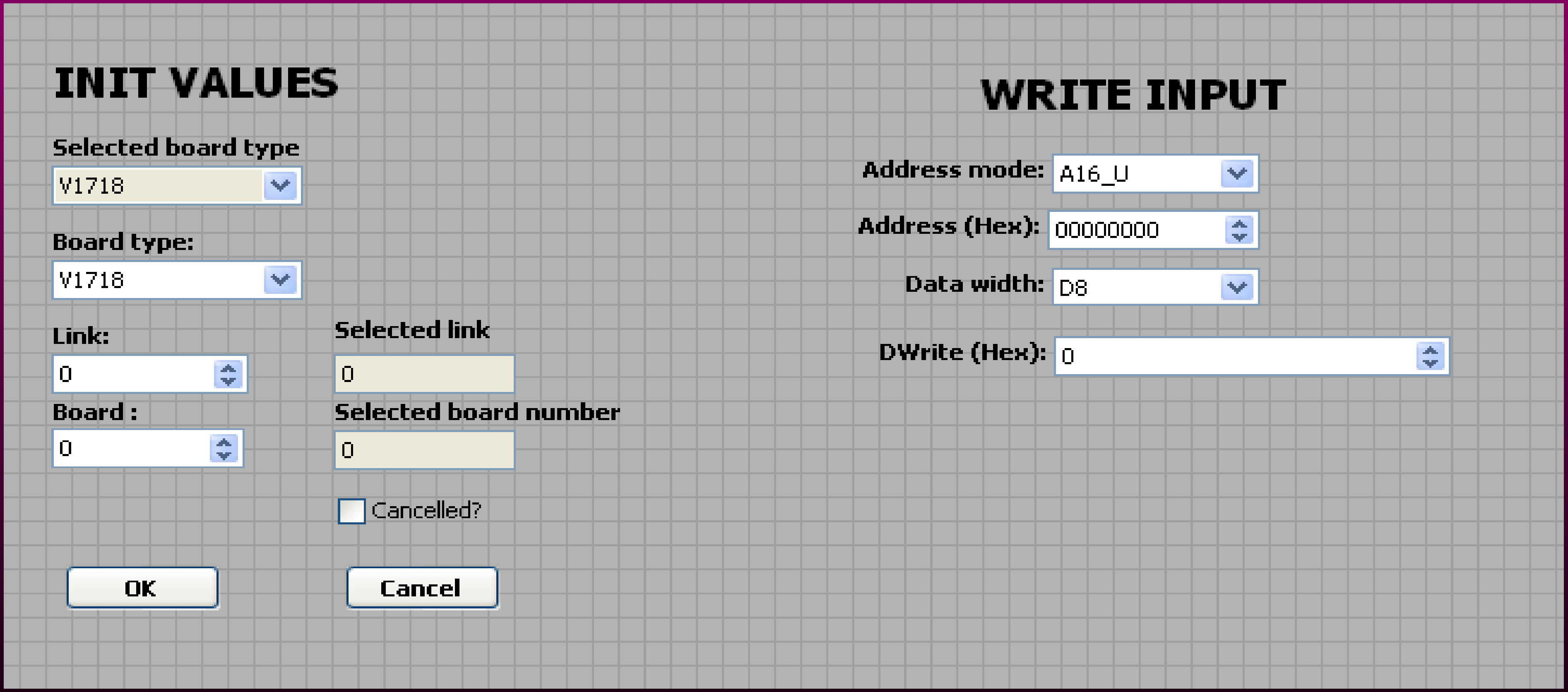
READ OUTPUT

Results: 0

VME and LabView (write cycle)



VME and LabView (write panel)



INIT VALUES

Selected board type: V1718

Board type: V1718

Link: 0

Board : 0

Selected link: 0

Selected board number: 0

□ Cancelled?

WRITE INPUT

Address mode: A16_U

Address (Hex): 00000000

Data width: D8

DWrite (Hex): 0

Laboratory’s PC access

- Username: student
- Password: ST15LACD
- $ cd Studenti2023
- $ mkdir my_dir (“my_dir” should be different for every group)
- $ cd my_dir
- $ cp –r /home/student/Programs .
- $ cp –r /home/student/Exercises .
- $ ls

You should see two directories “Exercises” and “Programs”.

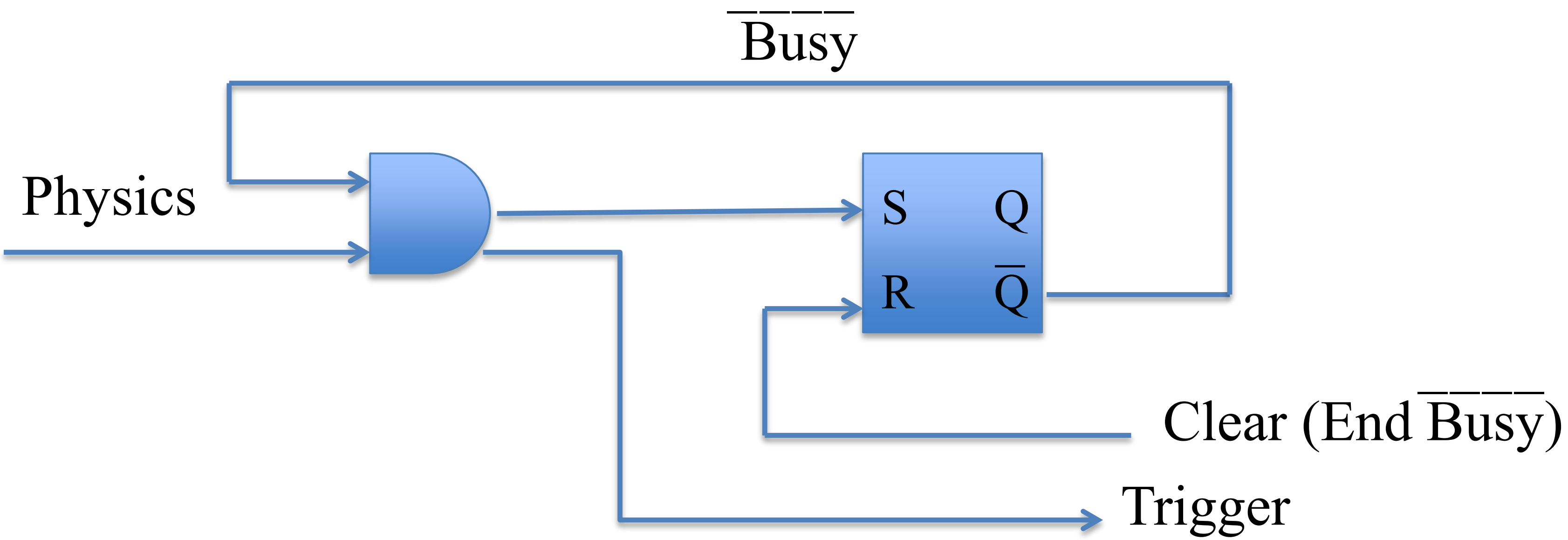
You must use only the programs inside your working directory “Studenti2023/my_dir” (be careful NOT to use other people’s programs)

Labview

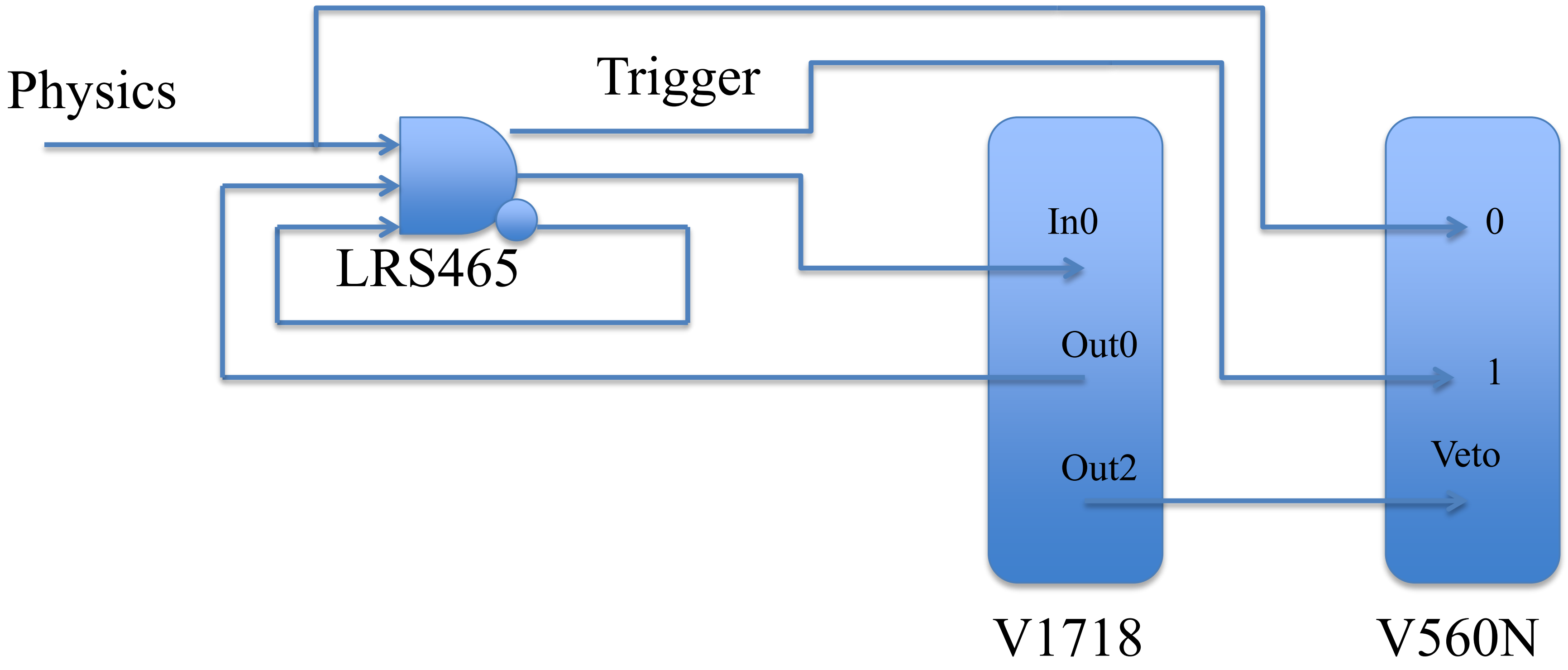
- $ cd Programs
- $ pwd → (you should be in /home/student/Student2023/my_dir/Programs)
- $ ls → (you should see the vi’s; the first is “1101-StartStop.vi”)
- $ dmesg (you should read “/usr/local/caen/v1718_driver... driver”);
- Turn on the VME crate;
- $ dmesg → (you should read “usbcore: registered new driver usbtest”);
- $./version

  ```
  CAENVME library release: 2.41.0
  V1718 firmware release: 2.07
  ```
- $ labview

DO NOT MOVE, RENAME, ANY OF THE FILES IN THE MAIN DIRECTORY!!! ESPECIALLY
/home/student/CAENVME.llb (CAEN library for V1718)
/home/student/CAENVMEtypes.h (parameters descriptor)
/home/student/cbd_8210_CAEN.llb (CAEN library for CBD8210)

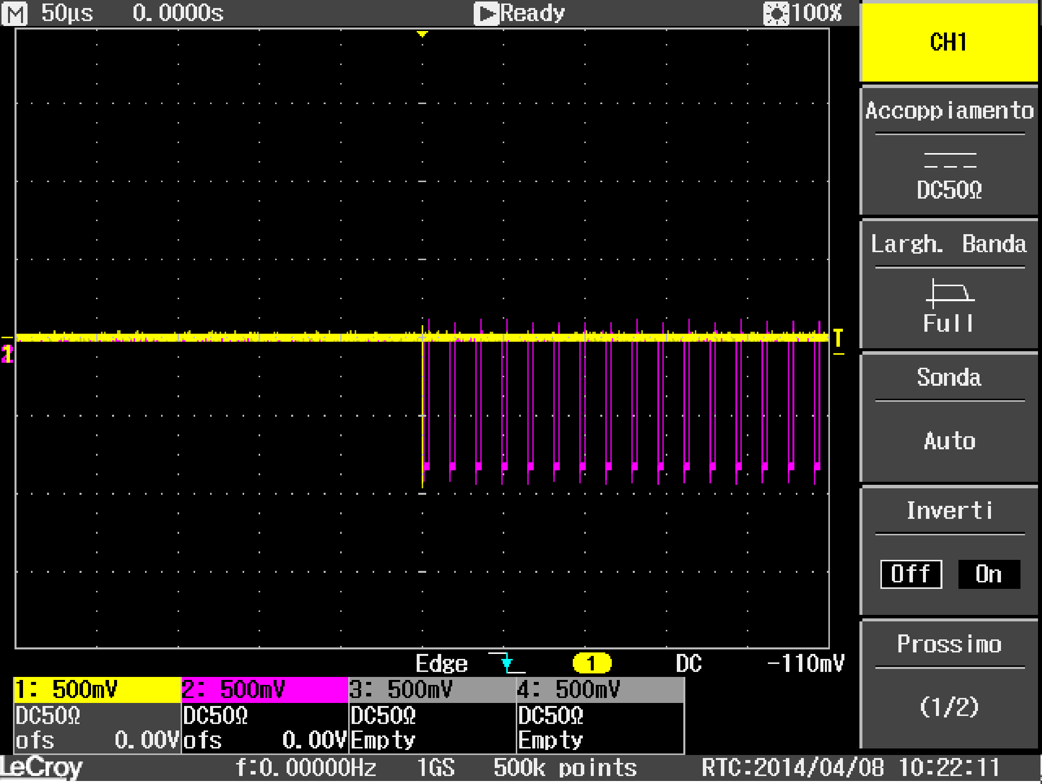


The arrival of a “Physics” event will generate a “Trigger” signal which is sent to the computer. At the same time the Trigger will inhibit the coincidence to future events by setting the “Busy-bar” signal (which will go to “zero”). The coincidence will remain inhibited until a Clear signal is sent by the computer which will end the Busy-bar signal and open the coincidence to future Physics events.



```
Out0 = Busy-bar : Start via SW at Begin Run
                  Reset via In0 at "Physics"
                  Start via SW at End of Read Cycle
Out2 = Veto     : Start via SW at Begin Run [Inv.Pol.]
                  Stop via SW at End of Run

Out0 and Out2 are levels, since width > period
```



M 50µs 0.0000s ▶Ready 100%

CH1

Accoppiamento
DC50Ω

Largh. Banda
Full

Sonda
Auto

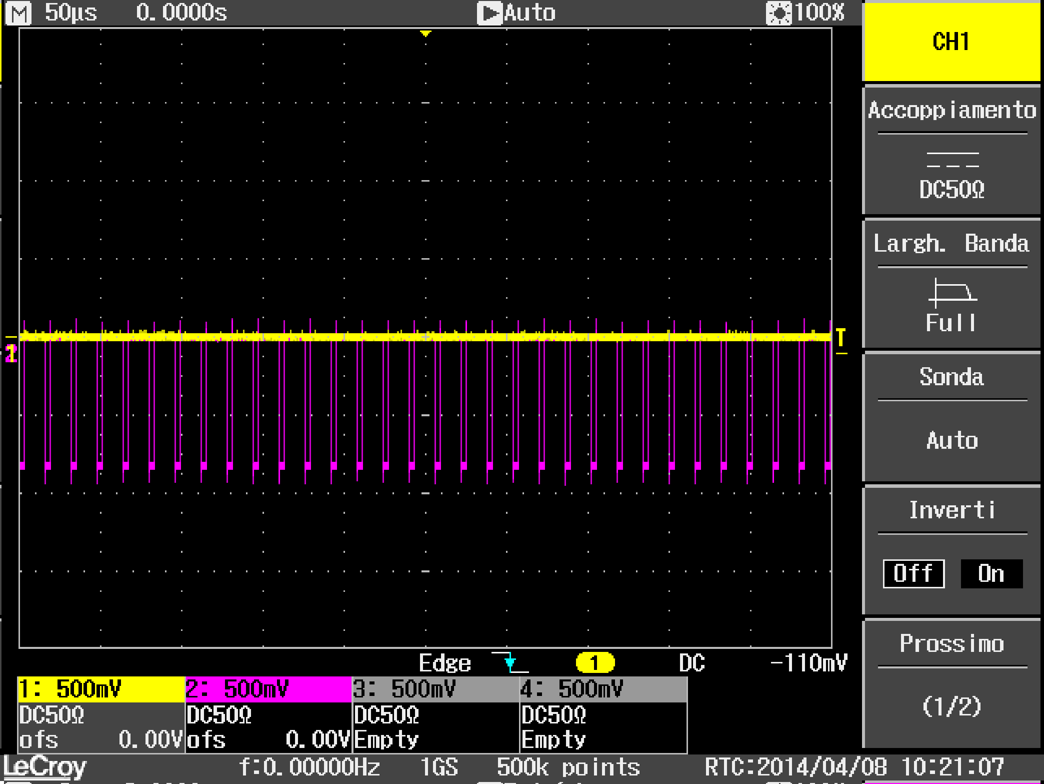
Inverti
Off On

Prossimo
(1/2)

Edge 1 DC −110mV

1: 500mV	2: 500mV	3: 500mV	4: 500mV
DC50Ω	DC50Ω	DC50Ω	DC50Ω
ofs 0.00V	ofs 0.00V	Empty	Empty

LeCroy f:0.00000Hz 1GS 500k points RTC:2014/04/08 10:22:11



M 50µs 0.0000s ▶Auto 100%

CH1

Accoppiamento
DC50Ω

Largh. Banda
Full

Sonda
Auto

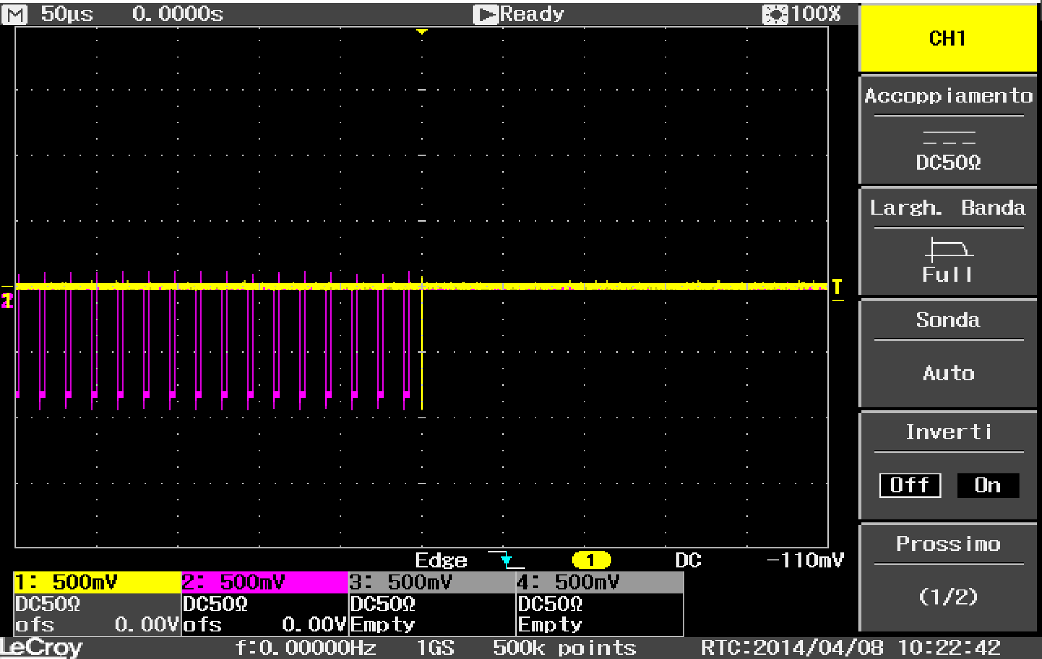
Inverti
Off On

Prossimo
(1/2)

Edge 1 DC −110mV

1: 500mV	2: 500mV	3: 500mV	4: 500mV
DC50Ω	DC50Ω	DC50Ω	DC50Ω
ofs 0.00V	ofs 0.00V	Empty	Empty

LeCroy f:0.00000Hz 1GS 500k points RTC:2014/04/08 10:21:07



M 50µs 0.0000s ▶Ready 100%

CH1

Accoppiamento
DC50Ω

Largh. Banda
Full

Sonda
Auto

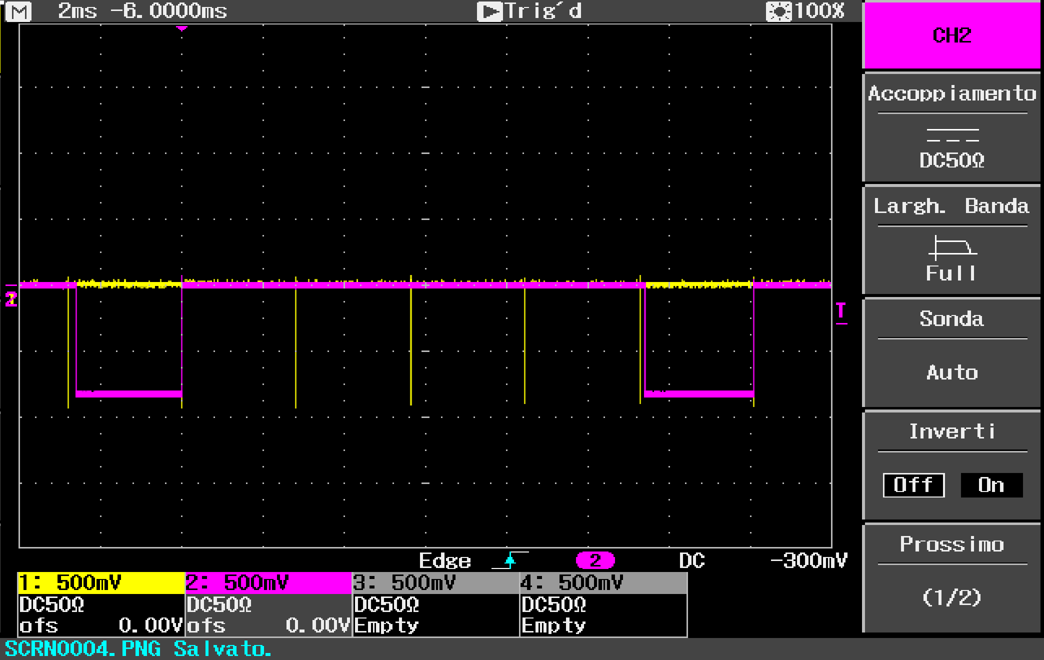
Inverti
Off On

Prossimo
(1/2)

Edge 1 DC −110mV

1: 500mV	2: 500mV	3: 500mV	4: 500mV
DC50Ω	DC50Ω	DC50Ω	DC50Ω
ofs 0.00V	ofs 0.00V	Empty	Empty

LeCroy f:0.00000Hz 1GS 500k points RTC:2014/04/08 10:22:42



M 2ms −6.0000ms ▶Trig'd 100%

CH2

Accoppiamento
DC50Ω

Largh. Banda
Full

Sonda
Auto

Inverti
Off On

Prossimo
(1/2)

Edge 2 DC −300mV

1: 500mV	2: 500mV	3: 500mV	4: 500mV
DC50Ω	DC50Ω	DC50Ω	DC50Ω
ofs 0.00V	ofs 0.00V	Empty	Empty

SCRN0004.PNG Salvato.

CAMAC STANDARD

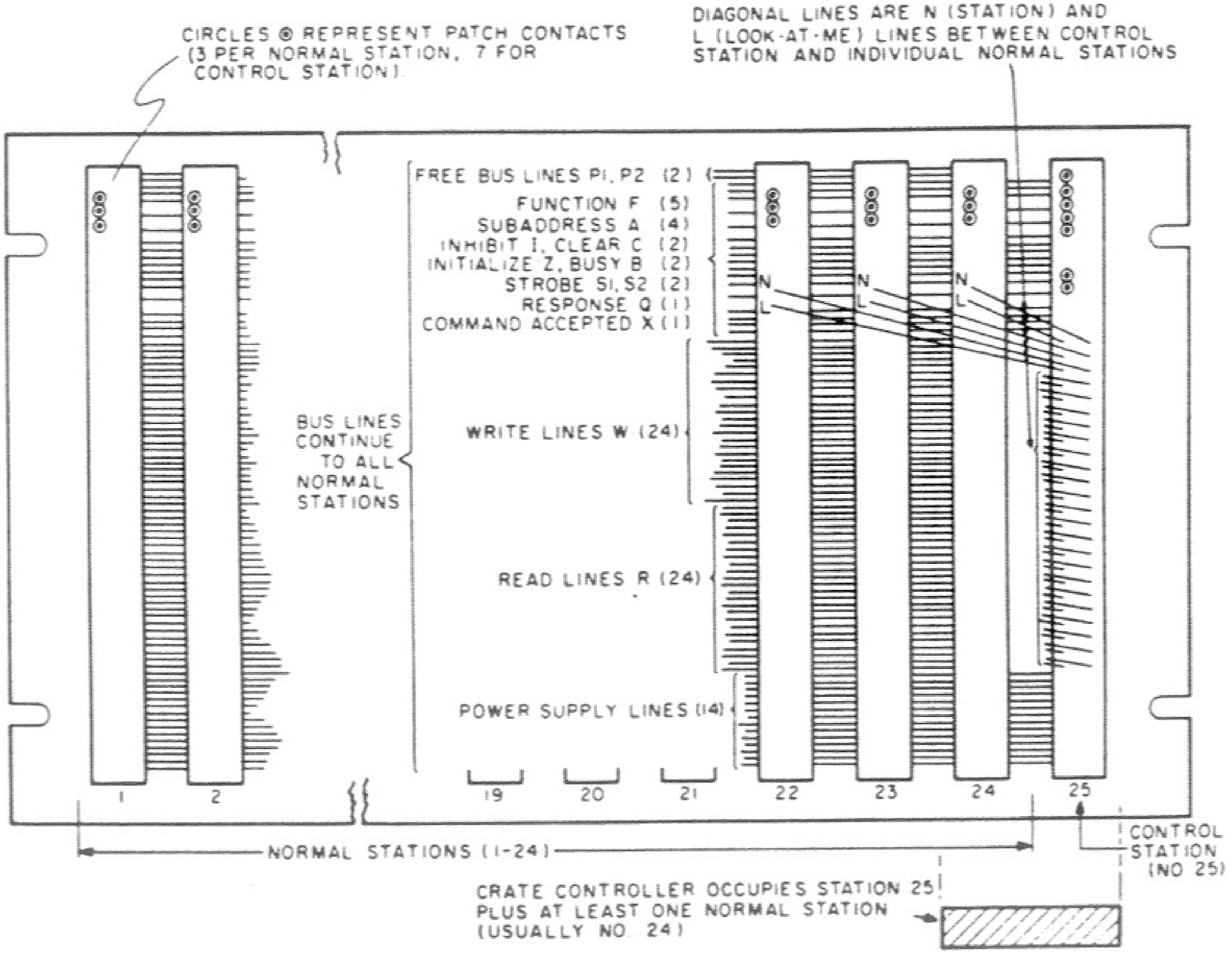
CAMAC is an international standard of modularized. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized bus called a DATAWAY. The DATAWAY is then interfaced to a computer. Thus, CAMAC allows information to be transferred into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC crate which has 25 STATIONS, numbered 1 - 25. Station 25, the rightmost station, is reserved for a CRATE CONTROLLER, whereas Stations 1 - 24 are NORMAL STATIONS used for CAMAC modules (see Block Diagram). Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC COMMANDS to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Module power, address bus, control bus and data bus are provided by the DATAWAY. The DATAWAY lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Table 3 for a pin allocation chart.

In a typical DATAWAY operation, the crate controller issues a CAMAC COMMAND which includes a Crate (C) Station (N), a subAddress (A), and Function (F), (see Table 1). In response, the module may generate valid Command Accepted (X response) and act on the command and generate a Command Issued (Q). If this command requires data transfer, the (R) or write (W) line will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a Read command, the controller reads data contained within a module and the module writes data into the DATAWAY.

CAMAC BUS "DATAWAY" wiring



CIRCLES ⊚ REPRESENT PATCH CONTACTS (3 PER NORMAL STATION, 7 FOR CONTROL STATION).
DIAGONAL LINES ARE N (STATION) AND L (LOOK-AT-ME) LINES BETWEEN CONTROL STATION AND INDIVIDUAL NORMAL STATIONS
FREE BUS LINES P1, P2 (2)
FUNCTION F (5)
SUBADDRESS A (4)
INHIBIT I, CLEAR C (2)
INITIALIZE Z, BUSY B (2)
STROBE S1, S2 (2)
RESPONSE Q (1)
COMMAND ACCEPTED X (1)
BUS LINES CONTINUE TO ALL NORMAL STATIONS
WRITE LINES W (24)
READ LINES R (24)
POWER SUPPLY LINES (14)
N
L
N
L
N
L
1
2
19
20
21
22
23
24
25
NORMAL STATIONS (1-24)
CONTROL STATION (NO 25)
CRATE CONTROLLER OCCUPIES STATION 25 PLUS AT LEAST ONE NORMAL STATION (USUALLY NO. 24)

Contact allocation at Control Station N25

Communication with plug-in units takes place through the DATAWAY. This passive backplane is incorporated in the crate and links the 86-pin sockets to all stations. The bus lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified DATAWAY wiring but can be connected to individual points to which patch leads may be attached.

During a DATAWAY operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus lines to specify a sub-section of the module or modules, and signals on the Function bus lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus line, which is available at all stations to indicate that a DATAWAY operation is in progress.

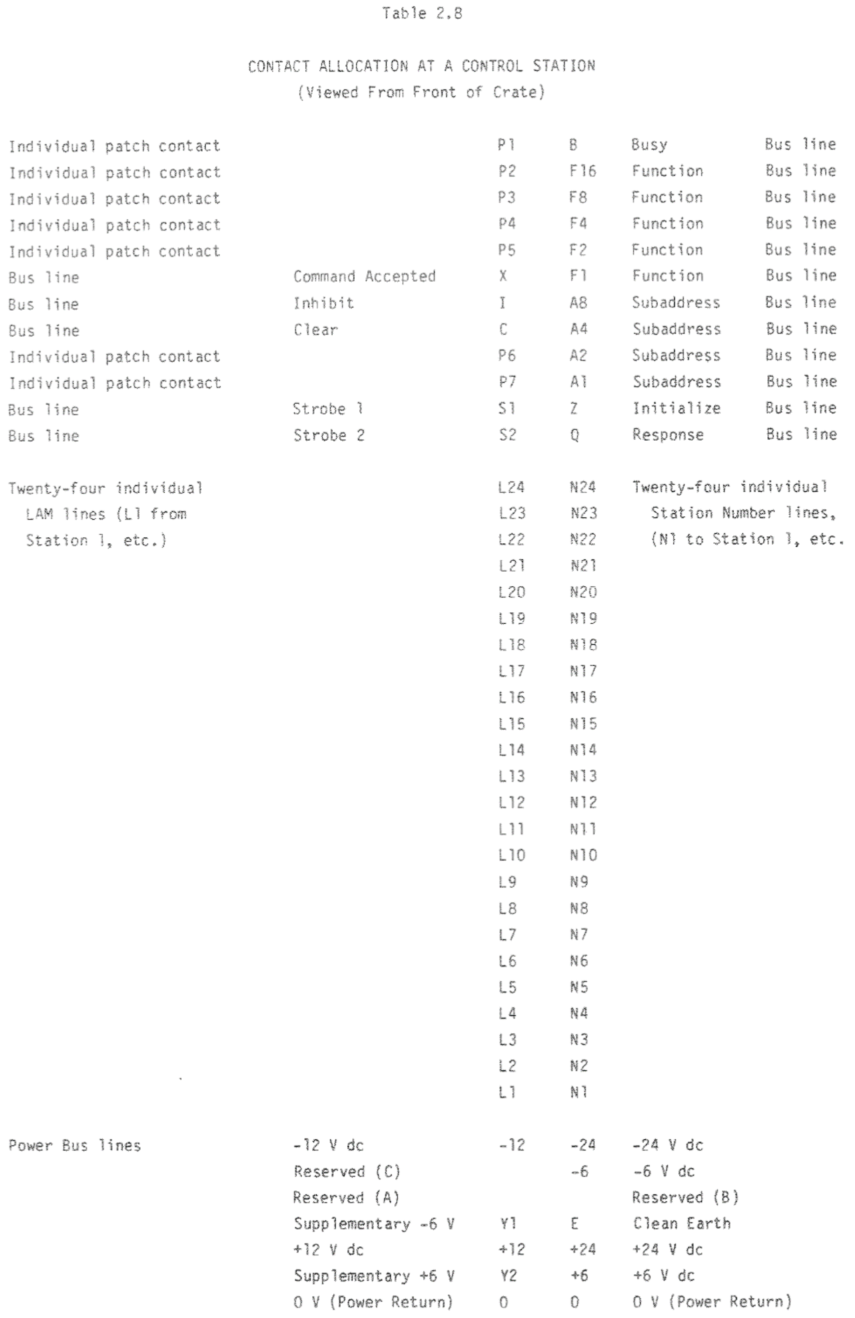


Table 2.8

CONTACT ALLOCATION AT A CONTROL STATION
(Viewed From Front of Crate)

Individual patch contact		P1	B	Busy	Bus line
Individual patch contact		P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual patch contact		P6	A2	Subaddress	Bus line
Individual patch contact		P7	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
Twenty-four individual LAM lines (L1 from Station 1, etc.)		L24	N24	Twenty-four individual Station Number lines, (N1 to Station 1, etc.	
		L23	N23		
		L22	N22		
		L21	N21		
		L20	N20		
		L19	N19		
		L18	N18		
		L17	N17		
		L16	N16		
		L15	N15		
		L14	N14		
		L13	N13		
		L12	N12		
		L11	N11		
		L10	N10		
		L9	N9		
		L8	N8		
		L7	N7		
		L6	N6		
		L5	N5		
		L4	N4		
		L3	N3		
		L2	N2		
		L1	N1		
Power Bus lines	-12 V dc	-12	-24	-24 V dc	
	Reserved (C)		-6	-6 V dc	
	Reserved (A)			Reserved (B)	
	Supplementary -6 V	Y1	E	Clean Earth	
	+12 V dc	+12	+24	+24 V dc	
	Supplementary +6 V	Y2	+6	+6 V dc	
	0 V (Power Return)	0	0	0 V (Power Return)	

Contact allocation at Normal Station N1 - N24

When a module recognizes a Read command calling for a data transfer to the controller, it establishes data signals on the Read bus lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus line.

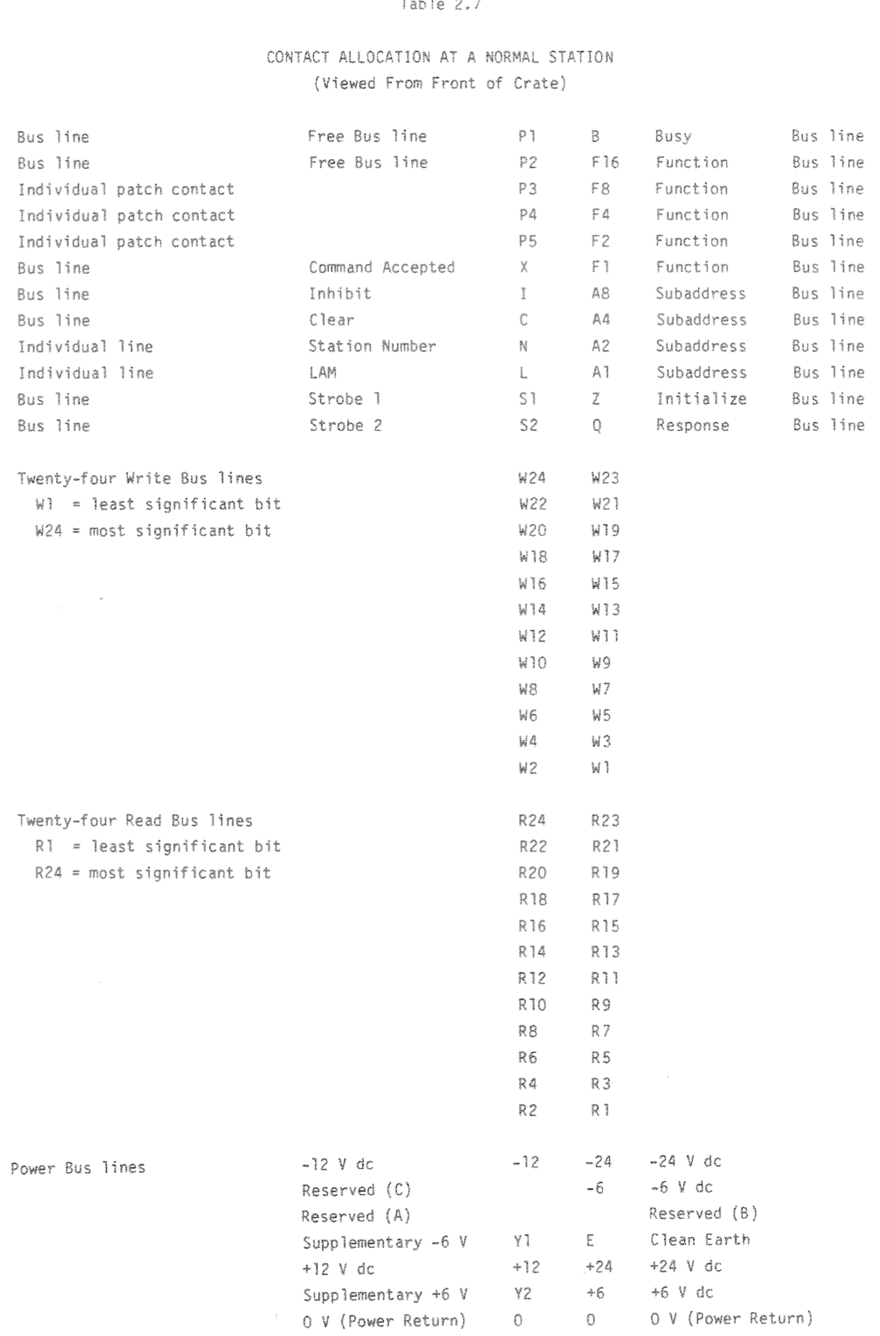


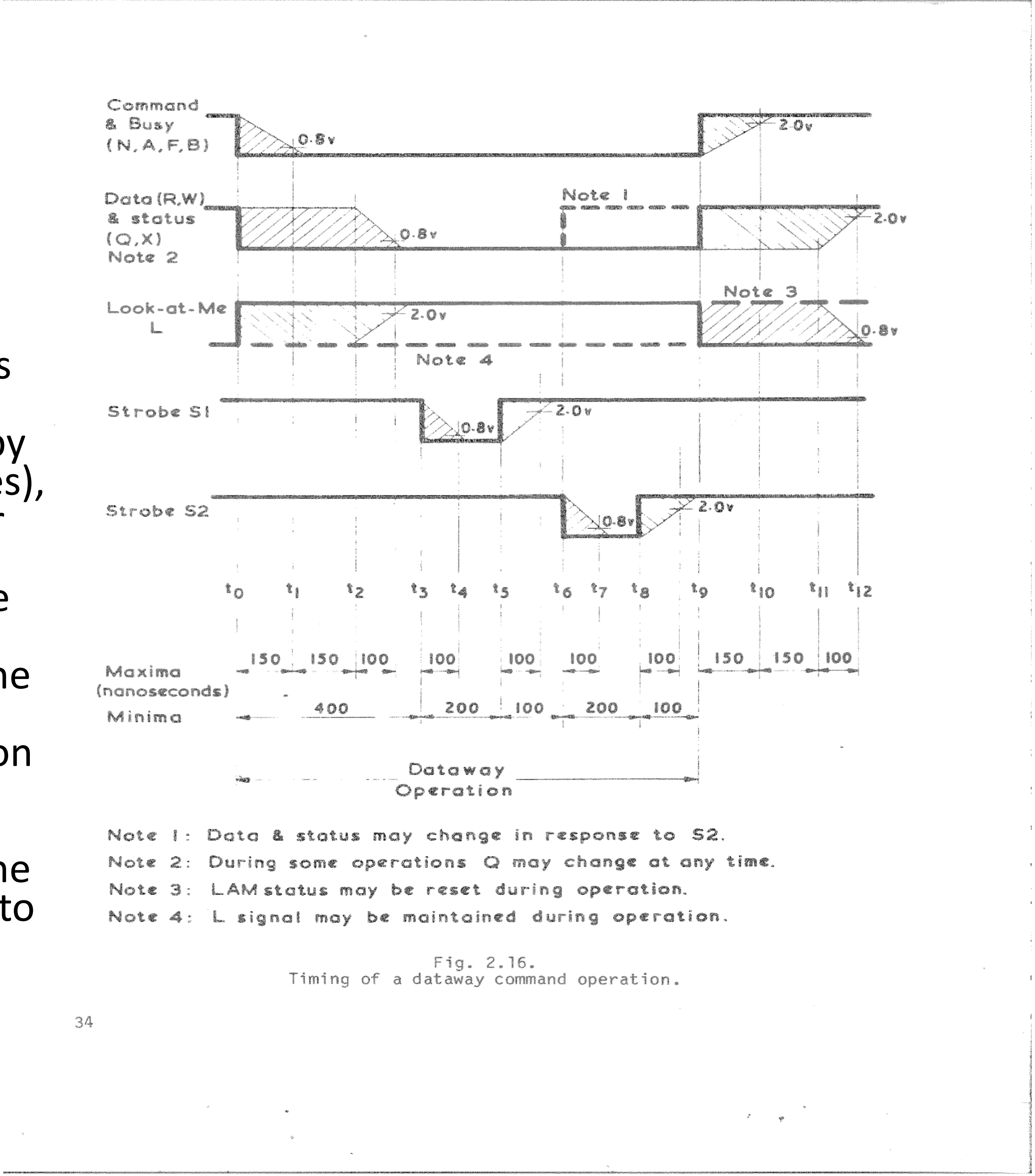
Table 2.7

CONTACT ALLOCATION AT A NORMAL STATION
(Viewed From Front of Crate)

Bus line	Free Bus line	P1	B	Busy	Bus line
Bus line	Free Bus line	P2	F16	Function	Bus line
Individual patch contact		P3	F8	Function	Bus line
Individual patch contact		P4	F4	Function	Bus line
Individual patch contact		P5	F2	Function	Bus line
Bus line	Command Accepted	X	F1	Function	Bus line
Bus line	Inhibit	I	A8	Subaddress	Bus line
Bus line	Clear	C	A4	Subaddress	Bus line
Individual line	Station Number	N	A2	Subaddress	Bus line
Individual line	LAM	L	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	Z	Initialize	Bus line
Bus line	Strobe 2	S2	Q	Response	Bus line
Twenty-four Write Bus lines		W24	W23		
W1 = least significant bit		W22	W21		
W24 = most significant bit		W20	W19		
		W18	W17		
		W16	W15		
		W14	W13		
		W12	W11		
		W10	W9		
		W8	W7		
		W6	W5		
		W4	W3		
		W2	W1		
Twenty-four Read Bus lines		R24	R23		
R1 = least significant bit		R22	R21		
R24 = most significant bit		R20	R19		
		R18	R17		
		R16	R15		
		R14	R13		
		R12	R11		
		R10	R9		
		R8	R7		
		R6	R5		
		R4	R3		
		R2	R1		
Power Bus lines	-12 V dc	-12	-24	-24 V dc	
	Reserved (C)		-6	-6 V dc	
	Reserved (A)			Reserved (B)	
	Supplementary -6 V	Y1	E	Clean Earth	
	+12 V dc	+12	+24	+24 V dc	
	Supplementary +6 V	Y2	+6	+6 V dc	
	0 V (Power Return)	0	0	0 V (Power Return)	

CAMAC DATAWAY timing

A command consists of signals on the DATAWAY lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines), and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the DATAWAY. They are accompanied by a signal on the Busy bus line which indicates to all units that a DATAWAY operation is in progress.



Note 1: Data & status may change in response to S2.

Note 2: During some operations Q may change at any time.

Note 3: LAM status may be reset during operation.

Note 4: L signal may be maintained during operation.

Fig. 2.16.
Timing of a dataway command operation.

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Timing of the Command

STATION NUMBER (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the left-hand end as viewed from the front, beginning with Station 1.

SUBADDRESS (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus lines. These signals are decoded in the module to select one of up to sixteen subaddresses, numbered in decimal from 0 to 15.

FUNCTION (F16, F8, F4, F2, F1)

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the DATAWAY Command Operations section.

STROBE SIGNALS (S1 AND S2)

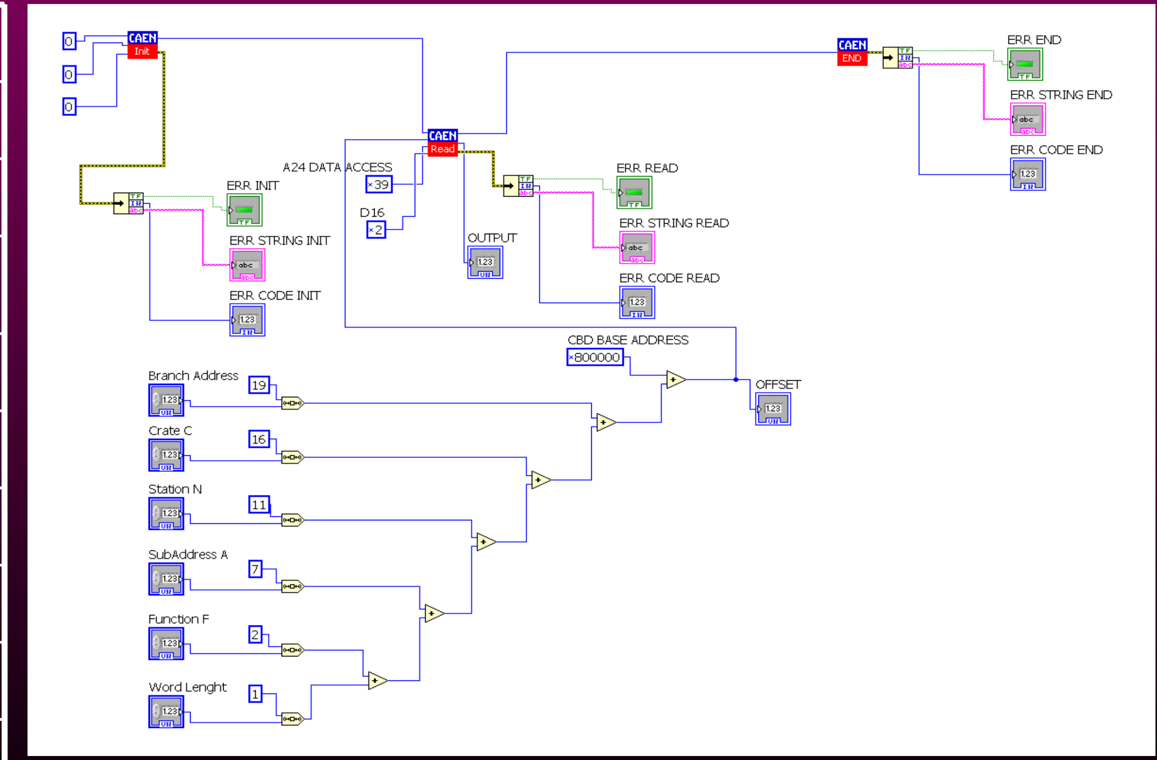
Two strobe signals S1 and S2 are generated in sequence on separate bus lines. These signals are used to transfer information between plug-in units via the DATAWAY or to initiate operations within units. In either case the specific action is determined by the command present on the DATAWAY. Both strobes are generated during each DATAWAY command operation, and all plug-in units which accept information from the DATAWAY do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the DATAWAY lines. All units which accept data from the DATAWAY in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of DATAWAY signals, for example, clearing a register whose output is connected to the DATAWAY.

VME and Camac

VME ADDRESS A24:
0x800000 - 0x87FFFF

***CBD 8210:* Camac Branch Driver**

Bit	Value
23	1
22	0
21 – 19	Branch Addr (0-7)
18 – 16	Crate Addr (1-7)
15 – 11	N Addr (Camac station)
10 – 07	A Addr (Camac sub-addr)
06 – 02	F Code (Camac funct)
01	0 = 24-bit or 1 = 16-bit
00	0



VME and Camac

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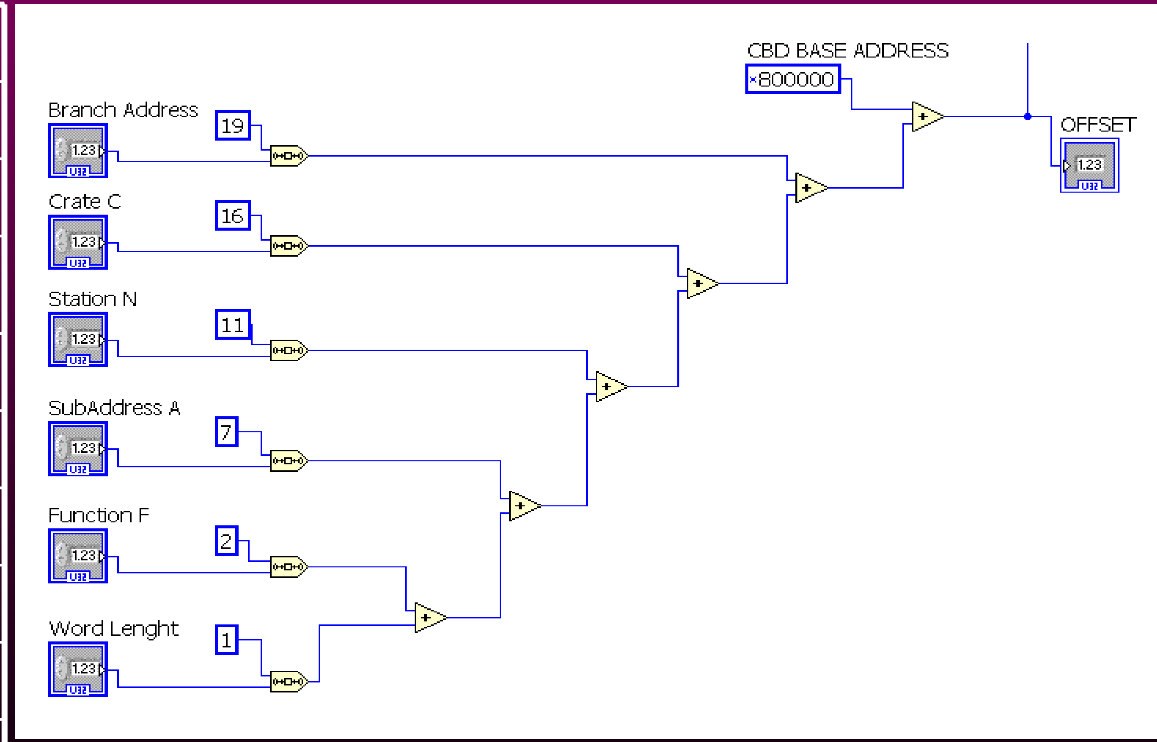
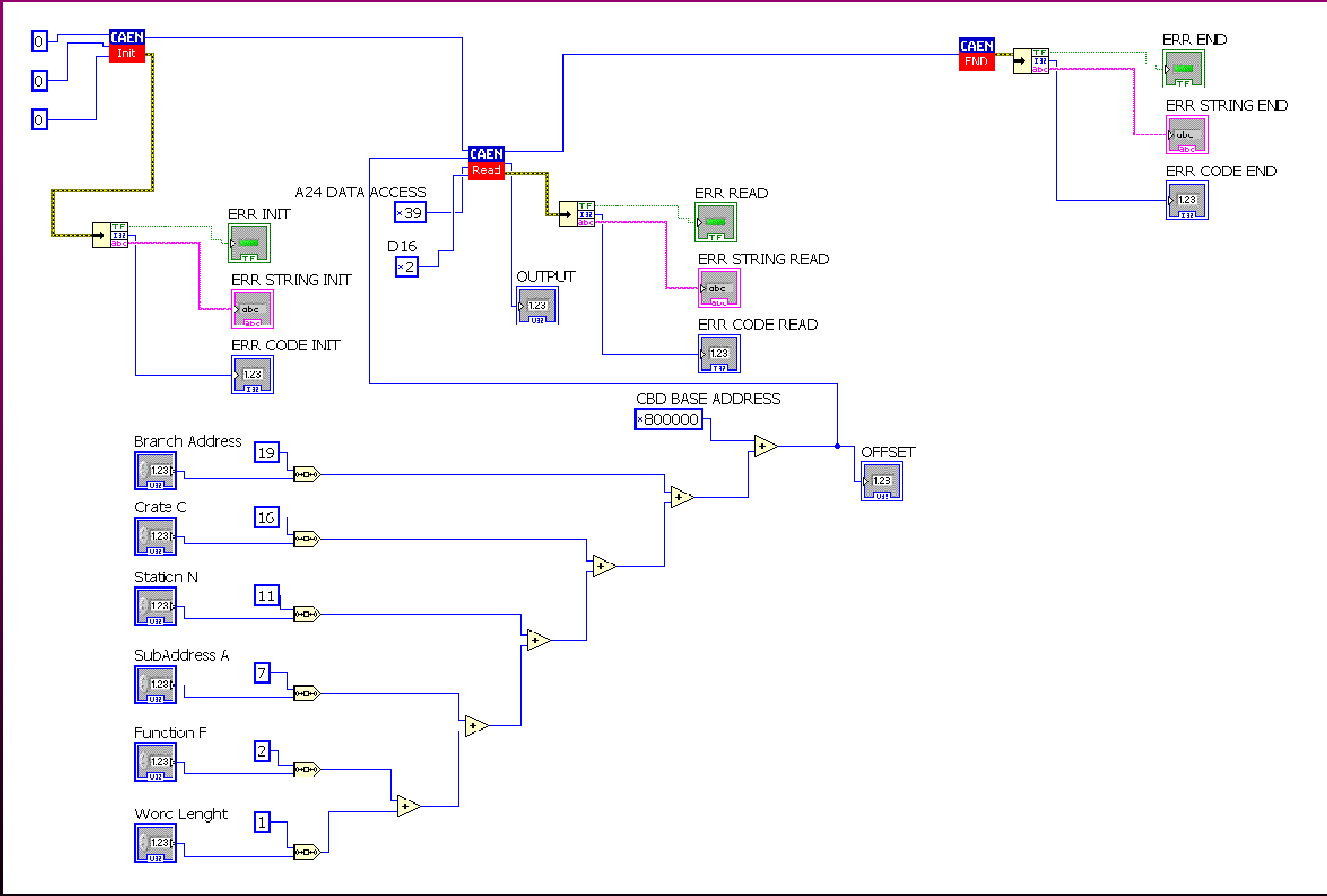



0
0
0
CAEN
Init
CAEN
Read
CAEN
END
ERR INIT
ERR STRING INIT
ERR CODE INIT
A24 DATA ACCESS
x39
D16
x2
OUTPUT
ERR READ
ERR STRING READ
ERR CODE READ
ERR END
ERR STRING END
ERR CODE END
CBD BASE ADDRESS
x800000
OFFSET
Branch Address
19
Crate C
16
Station N
11
SubAddress A
7
Function F
2
Word Lenght
1

VME and Camac

Camac Function Set

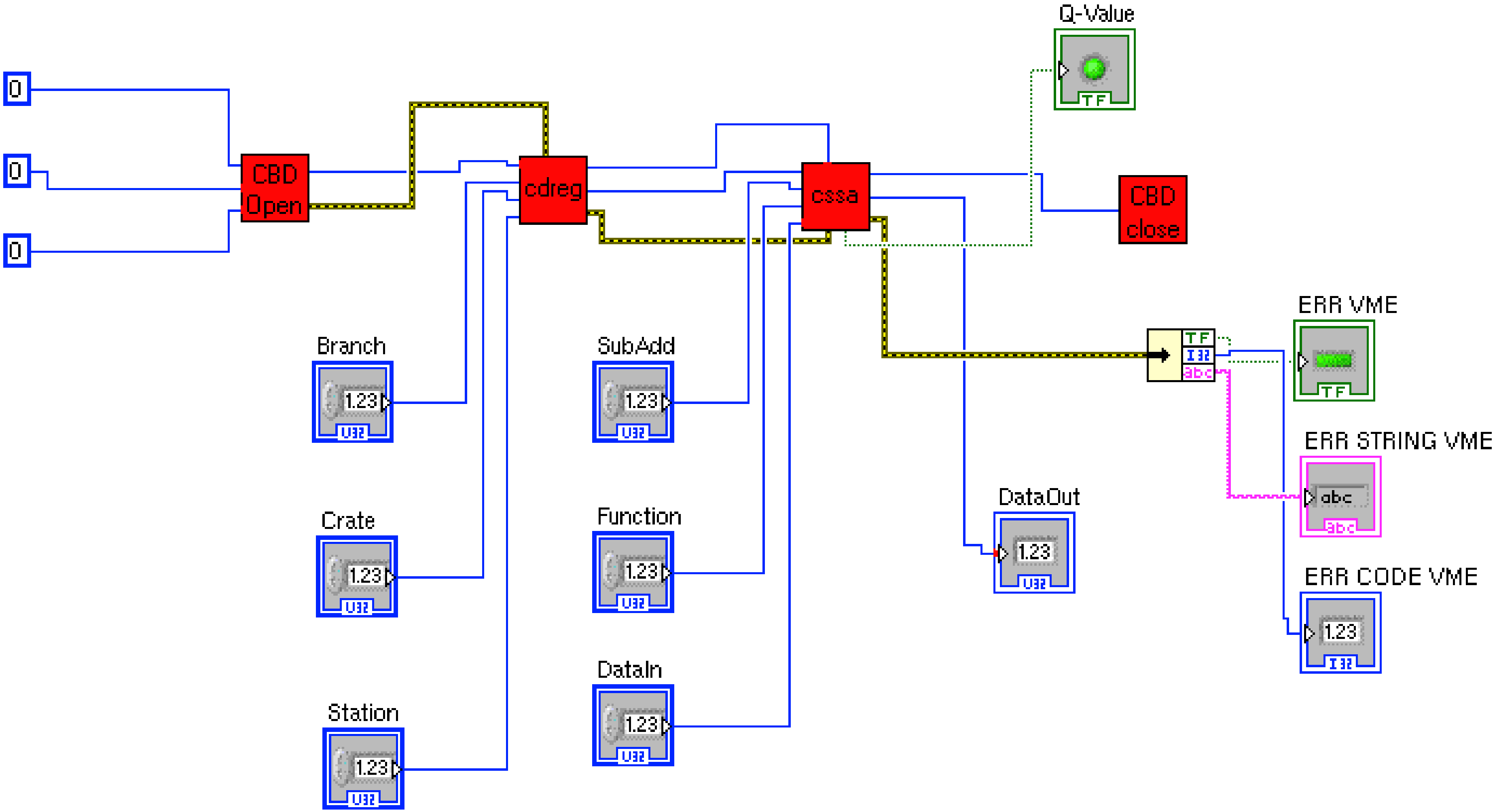
N	A	F	
28	8	26	Generate Z
28	9	26	Generate C
30	8	0	Read GL
30	8	16	Load SNR
30	9	24	Remove I
30	9	26	Generate I
30	9	27	Test I

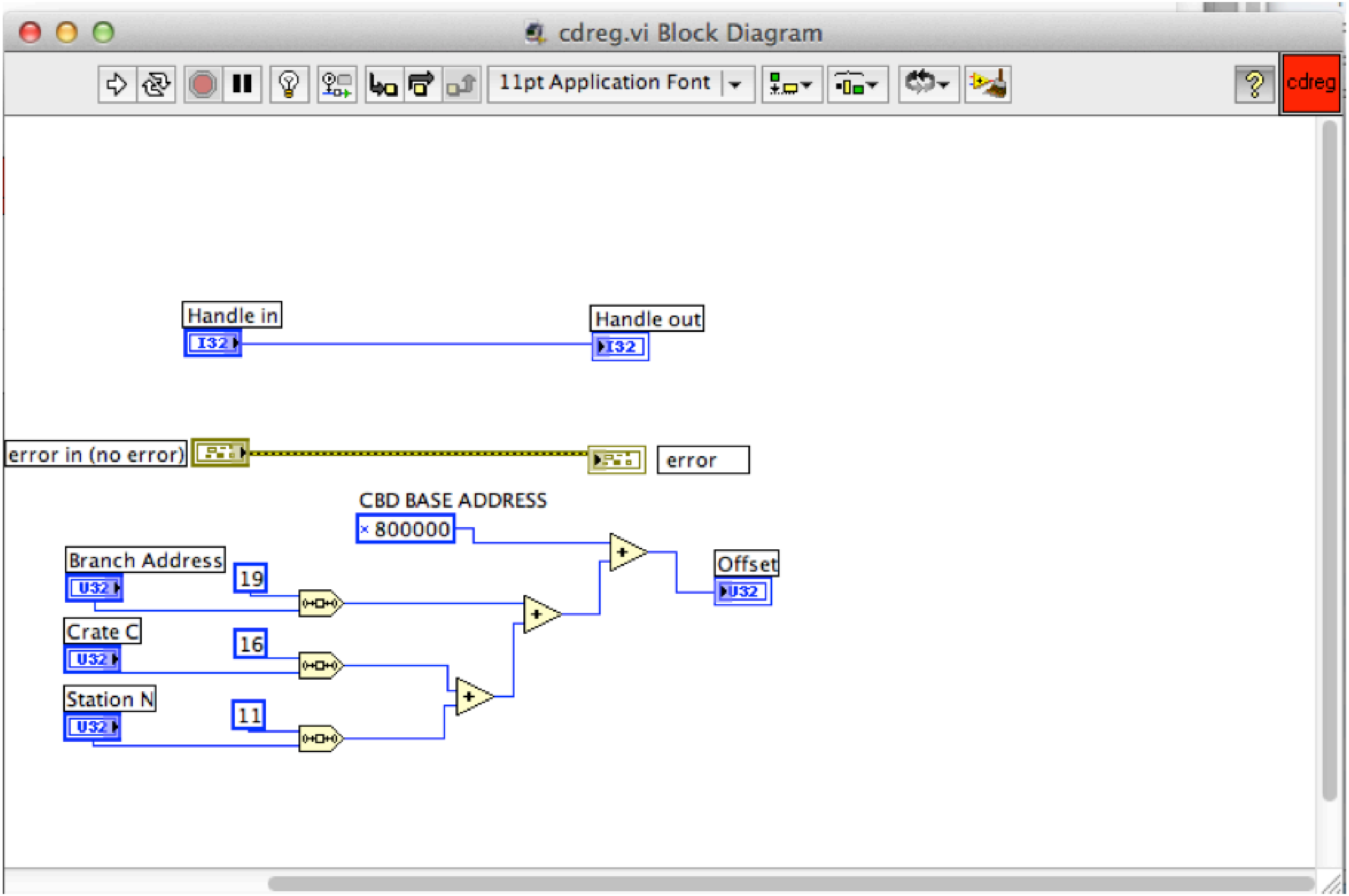
Selection of CBD 8210 Internal Register

CR	N	A	F	
0	29	0	0	CSR (Read/Write) 16 bit

↓

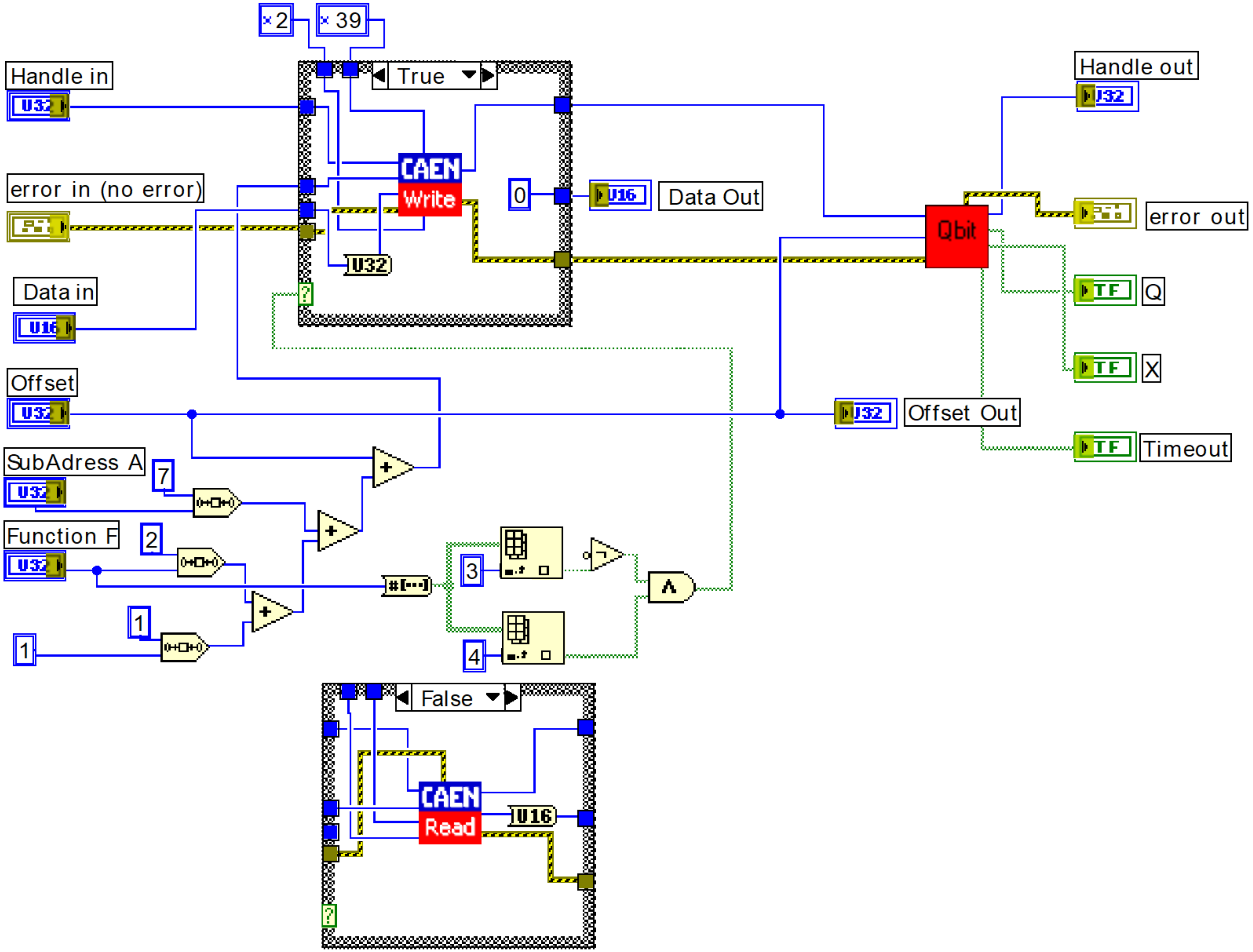
Bit	Value
15	Status of Q during the last Camac Cycle
14	Status of X during the last Camac Cycle
13	Time-Out Flag of last Camac Cycle

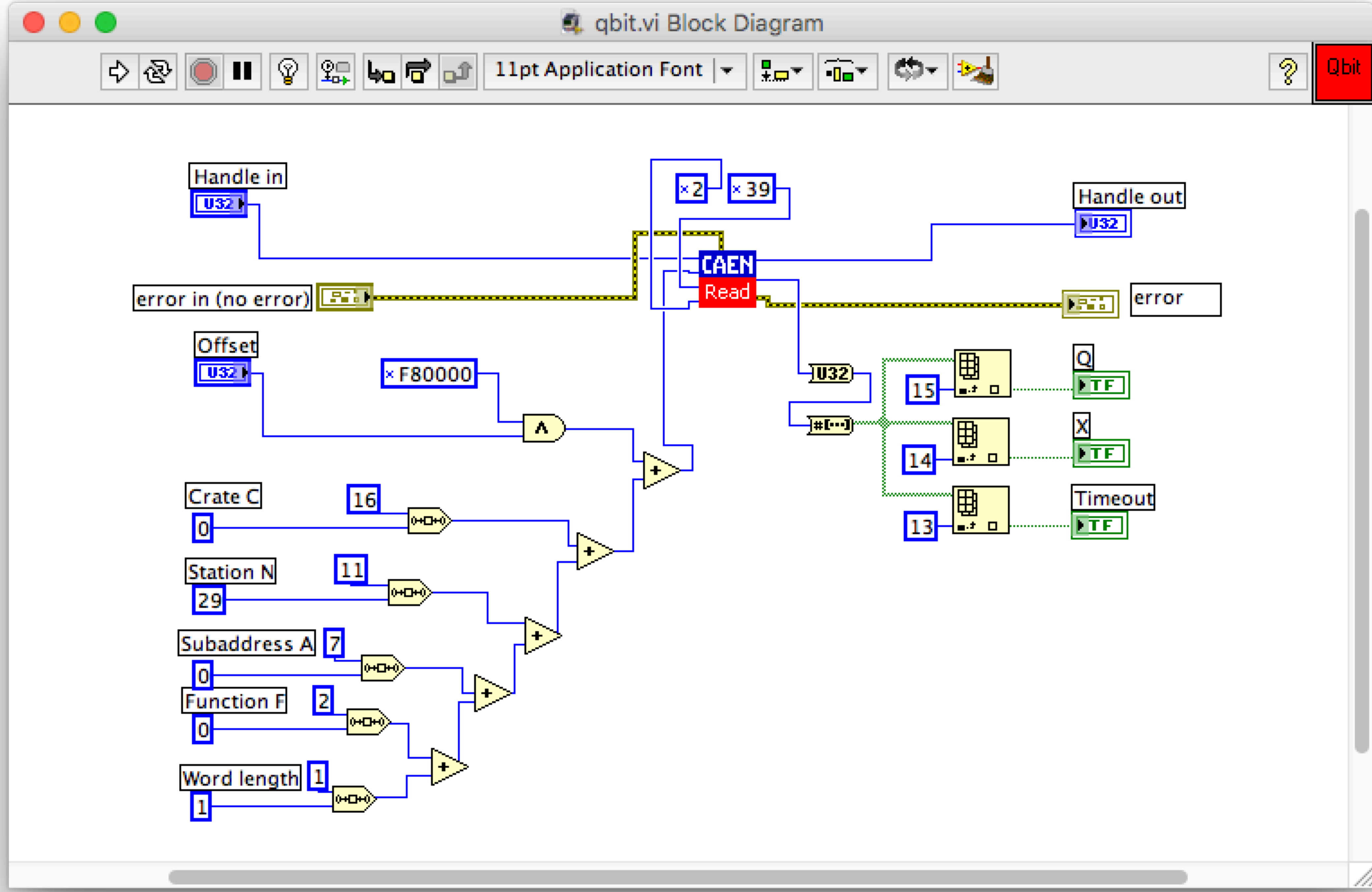

Q-Value
TF
0
0
0
CBD Open
cdreg
cssa
CBD close
ERR VME
TF
I32
abc
Branch
1.23
U32
SubAdd
1.23
U32
ERR STRING VME
abc
abc
DataOut
1.23
U32
Crate
1.23
U32
Function
1.23
U32
ERR CODE VME
1.23
I32
DataIn
1.23
U32
Station
1.23
U32


cdreg.vi Block Diagram
11pt Application Font
cdreg
Handle in
I32
Handle out
I32
error in (no error)
error
CBD BASE ADDRESS
x 800000
Branch Address
U32
19
Crate C
U32
16
Station N
U32
11
Offset
U32

cssa

cssa.vi
Macintosh HD:Users:rui:labview:VME:dummy libraries:LabVIEWUserLib:cbd_8210_CAEN.llb:cssa.vi
Last modified on 11-04-2014 at 17:21
Printed on 14-04-2014 at 10:41




qbit.vi Block Diagram
11pt Application Font
Qbit
Handle in
U32
error in (no error)
Offset
U32
F80000
2
39
CAEN
Read
Handle out
U32
error
U32
15
14
13
Q
TF
X
TF
Timeout
TF
Crate C
0
16
Station N
29
11
Subaddress A
7
0
Function F
2
0
Word length
1
1