Technical Information Manual

MOD. C 414

8 CHANNEL TIME-TO-DIGITAL CONVERTER

27th January 1993

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CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

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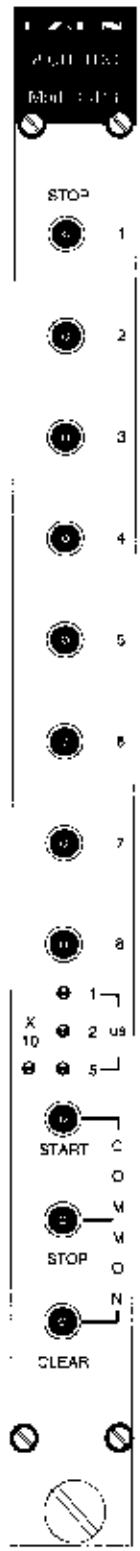

FRONT PANEL

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1. FUNCTIONAL DESCRIPTION

The CAEN Model C 414 "8 channel Time-To-Digital Converter" is housed in a one unit wide CAMAC module. This module has 8 independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Moreover, it disregards any stop pulses received before a start signal and will accept one stop for every start. Conversion begins upon receipt of the start signal and proceeds until either a stop signal is received or the cycle is terminated by the application of a clear signal or until time-to-digital conversion reaches full scale. LAM is generated at the end of the conversion time, if it is enabled and at least one channel has a significant value (valid).

On line testing is facilitated by using F(25), which internally generates starts and stops for each channel, allowing accurate testing of the module except for the external input signal.

By using the Fast Clear Input, excessive system dead time due to false starts may be eliminated. Accepting NIM level signals, Fast Clear Input allows the time-to-digital conversion to be cleared at any time without the necessity for any dataway operation.

The time-to-digital conversion is accomplished in two steps :

1. Time to voltage conversion

2. Voltage to digital conversion

1.1 TIME TO VOLTAGE CONVERSION

An integrating capacitor begins charging up upon receipt of the Common Start Pulse by a constant current source and it is terminated by the Stop Pulse. For channels which receive no Stop Pulse, an automatic internal Stop Pulse is generated at about 1.2 times the full scale time range setting after the Common Start Pulse. The total charge delivered to the capacitor is an analog representation of the time interval to be measured and this charge has a direct relationship to the voltage (V=Q/C) across the capacitor. The above process is common for all 8 channels (FIG. 1.1).

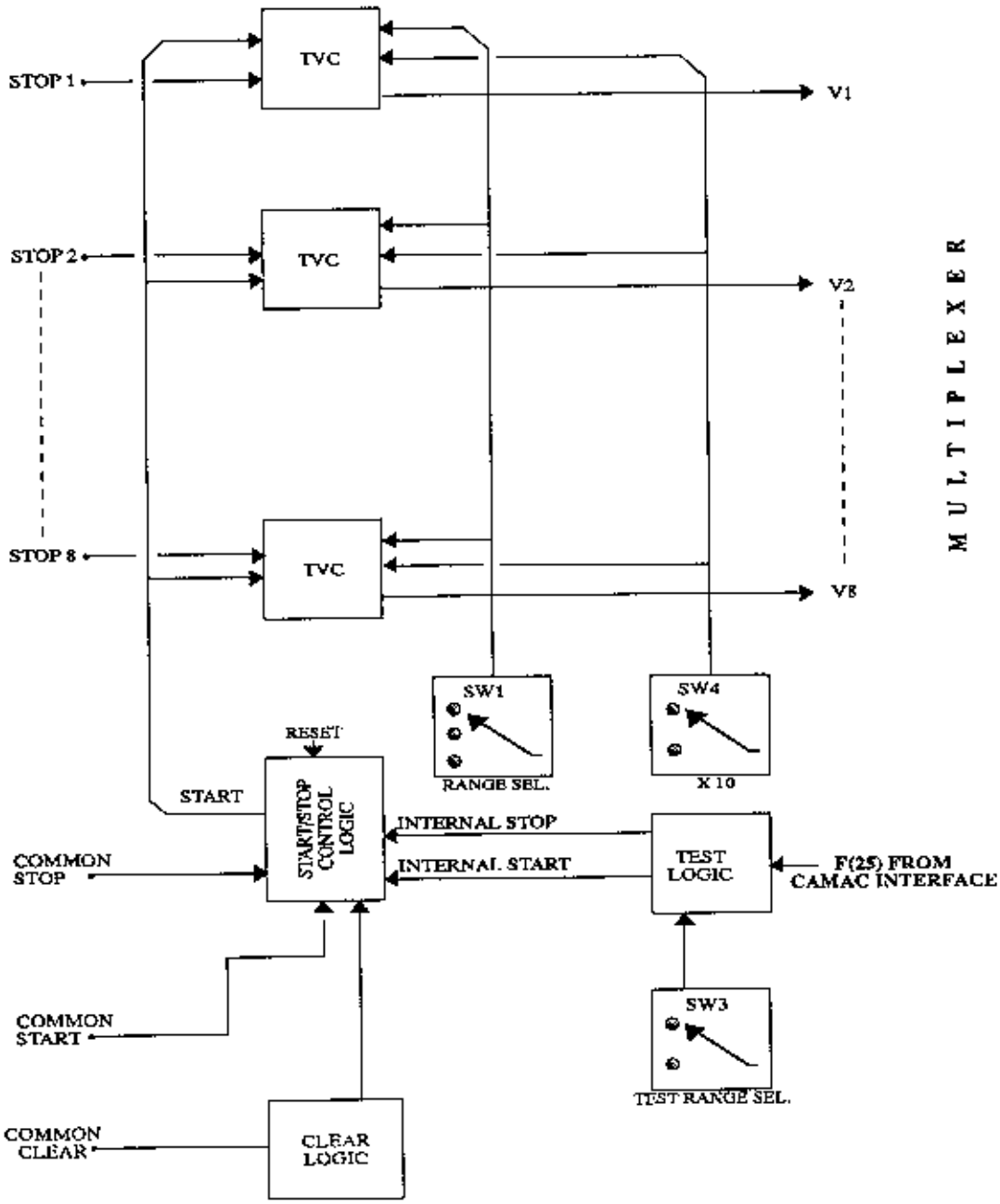

Figure 1.1 Block Diagram for the Time-to-Voltage Converter (TVC)

1.2 VOLTAGE TO DIGITAL CONVERSION

Voltage to digital conversion is performed by using SLIDING-SCALE method in order to reduce the differential non-linearity. The Control Logic Unit generates 8 bit random data (X) distributed uniformly in the interval range from 0 to 255. The signal coming from the Multiplexer, summed at the signal A(X) generated by the DAC, is sent to the ADC. After the conversion, the X signal, coming from the CLU, is subtracted from the 12 bit data coming from the ADC and is stored in an 8x12 bit static memory. In this way the A/D Conversion of the signal coming from the Multiplexer is obtained with a differential non-linearity better than one obtained by using only an ADC. The use of the Sliding Scale method limits the maximum digital number which can be read to $2^{12} - 2^{8} = 3840$. In order to avoid going over this value the time ranges are further limited to about 92% of the theoretical time ranges.

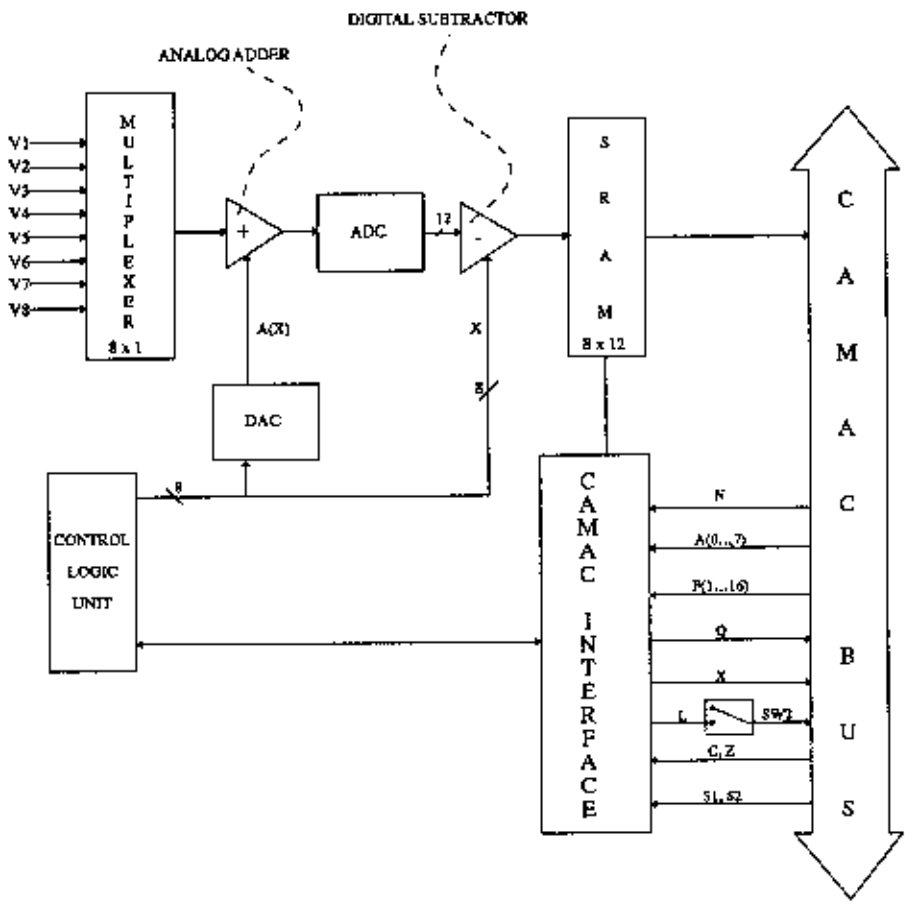

Figure 1.2 Block Diagram for V/D Conversion (Sliding Scale method)

The conversion time for every valid channel is 2.5 µs and for the channels in overflow the conversion time is 1.5 µs. The total time from the start pulse to the end of conversion can be calculated by using the following formula :

$$T_{tot} = 2.5 * N_c + 1.5 * (8 - N_c) + 1.2 * T_{f.s.} \quad \mu s$$

where T_{tot} is the total time, N_c is the number of valid channels, (8 - N_c) is the number of channels in overflow and $T_{f.s.}$ is the full scale selected time (expressed in µs).

There are three trimmers P6, P7, P8. Each one can control two values for the resolution, P8 for 25 ps and 250 ps, P7 for 50 ps and 500 ps, P6 for 125 ps and 1.25 ns. These trimmers are housed on the printed board inside the module and they are laterally accessible.

The Model C 414 has a 3-position switch (SW1) through which 100, 200 and 500 ns range can be selected and provide 25, 50 and 125 ps resolutions respectively when the dip switch SW4 is in position 1. Longer time ranges 1, 2 and 5 µs can be provided by adjusting the dip switch SW4 to position 2, which provide 250 ps, 500 ps and 1.25 ns resolutions respectively (FIG. 1.3). This module can generate a START/STOP signal, common for all channels, for test purposes: the interval between the START and STOP can either be 400ns or 4µs. This interval can be adjusted by using the SW3 switch (FIG. 1.3).

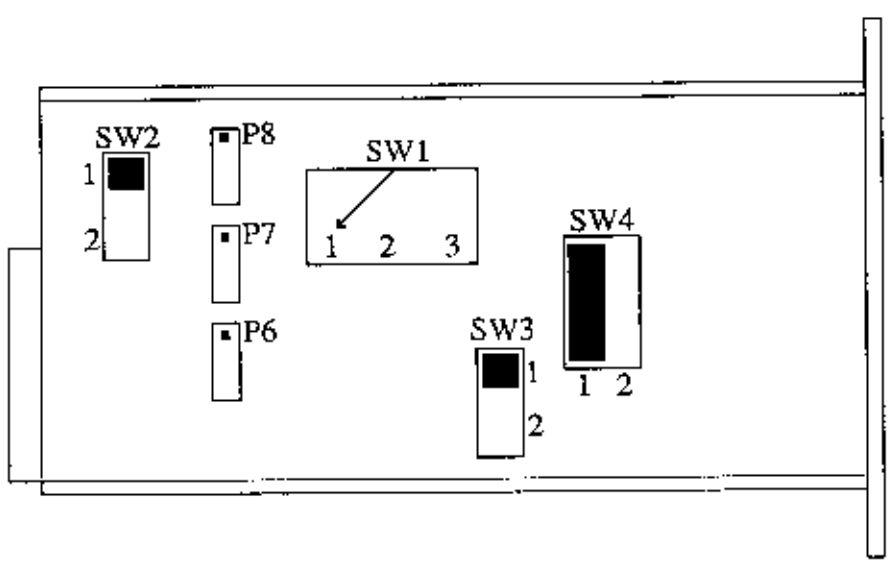

Figure 1.3 Dip switches and Pols

TIME RANGE	RESOLUTION	CORRESPONDING POT
0 to 100 ns	25 ps	P8
0 to 200 ns	50 ps	P7
0 to 500 ns	125 ps	P6
0 to 1 µs	250 ps	P8
0 to 2 µs	500 ps	P7
0 to 5 µs	1.25 ns	P6

SW1Settings			
	1	2	3
SW4 Setting 1	100 ns	200 ns	500 ns
SW4 Setting 2	1 µs	2 µs	5 µs

SW3 Settings	
1	2
400 ns	4 µs

SW2 Settings	
1	2
LAM Disable	LAM Enable

2.SPECIFICATIONS

2.1 GENERAL

Number of channels:	8
Resolution:	12 bits
Number of ranges:	6
Time Range and Time Resolution:	
0 to 100 ns	25 ps
0 to 200 ns	50 ps
0 to 500 ns	125 ps
0 to 1 µs	250 ps
0 to 2 µs	500 ps
0 to 5 µs	1.25 ns
Conversion Time:	2.5 µs per each valid input channel
Usable Time Range (FULL SCALE):	92% of the time range
Integral Non-Linearity:	±4 counts for worst case (from 20 ns to full scale)
Differential Non-Linearity:	±1.5% (from 20 ns to full scale)
Rejects STOPS before STARTS	
Internal Test Capability:	(F(25))
LAM suppression.	
Fast Clear Input:	minimum 10 ns (active after 800 ns)
Min. input pulse width:	10 ns
Time Resolution Temperature:	400ppm/°C - 0 to 60°C
Time Resolution Channel Dispersion:	<5%

2.2 EXTERNAL COMPONENTS

2.2.1 STOP INPUTS

There are 8 Stop Inputs: standard NIM levels on 50 Ω impedance; LEMO 00 type connectors.

Pulses at these inputs define the end of timing intervals for the channels. They are ineffective unless preceded by a start input. Minimum Stop Input pulse width is 10 ns.

2.2.2 COMMON START INPUT

There is one Common Start Input: common to all channels, standard NIM level on 50 Ω impedance; LEMO 00 type connector.

A pulse applied to the start input begins the timing measurement. Minimum Common Start Input pulse width is 10 ns.

2.2.3 COMMON STOP INPUT

There is one Common Stop Input: common to all channels, standard NIM level on 50 Ω impedance; LEMO 00 type connector.

A pulse applied to the Common Stop Input will stop all channels. It is intended for test use. It is important to note that this common stop pulse will terminate the timing interval of a few ns later than if the same pulse were applied to the separate stop inputs. Minimum Common Stop Input pulse width is 10 ns.

2.2.4 FAST CLEAR INPUT

There is one Fast Clear Input: common to all channels, standard NIM level on 50 Ω impedance; LEMO 00 type connector.

The Fast Clear signal forces all 8 channels of the unit to cease their conversions and be clear and ready to accept another start pulse after 800 ns. The Fast Clear feature allows time-to-digital conversion to be initiated by a fast trigger and completed only if the event satisfies a complete trigger requirement. Minimum Fast Clear Input pulse width is 10 ns.

2.3 POWER REQUIREMENT

- 24 V 250 mA

+24 V 200 mA

+6 V 900 mA

-6 V 800 mA

3.CAMAC FUNCTIONS

F(0)NA(0..7)	Reads the data register of channels 0 to 7 on the Read Lines R1 to R12 of the CAMAC dataway. If R1 to R12=(11...1) the selected channel is in overflow. If Q=0 all the input channels are invalid.
F(2)NA(0...7)	Same as F(0) but with F(2)NA(7) also effecting a module clear.
F(8)NA(0)	Tests LAM. Q=1 if the LAM is enabled and present.
F(9)NA(0)	Clears the module. Clears and disables the LAM.
F(10)NA(0)	Clears the LAM.
F(24)NA(0)	Disables the LAM.
F(25)NA(0)	Tests the module. Internally generates a start and stop.
F(26)NA(0)	Enables LAM. Remains enabled until a Clear module or an F(24) are performed.

4.CAMAC COMMANDS

Z or C	Clear all the registers simultaneously. Disable the LAM.
Q	A Q=1 response is generated in recognition of an F(0) and F(2) read function, if there is at least one valid input channel. Otherwise Q=0. Q=1 response is generated in recognition to F(8) if LAM is enabled and present. Otherwise Q=O.
X	An X=1 (command accepted) response is generated when a valid F and N command is generated.
L	LAM signal is generated at the end of conversion when at least one channel is not in overflow and until a module Clear or a LAM Clear or a LAM disable is performed. LAM can be enabled by F(26) or disabled by F(24) and can be tested by F(8). It can also be permanently disabled via a dip switch (SW2) which is housed on the printed circuit board.

5. TEST PROCEDURE

5.1 INTRODUCTION

The following is intended to be a guide for the user. CAEN do not claim it to be exhaustive and therefore the module may be tested in various other ways.

Each procedural step contains the operation to be performed and the corresponding effect or the verification to be performed.

5.2 SUGGESTED INSTRUMENTS

-No. 1 CAMAC crate

-No. 2 Mod. N 93B Dual Timer

-No.1 Mod. N 146A Programmable Delay Unit

-No.1 CAEN Model C 249 CAMAC Manual Crate Controller

-No.1 Oscilloscope (bandwidth: min. 150 MHz)

5.3 PROCEDURE

CAUTION: Turn Off the CAMAC crate before inserting or removing the module.

NOTE: In the following instructions the groups of dip switches to be adjusted are named as they are labelled on the printed circuit lay-out: SW1, SW2, SW3, SW4 (FIG. 1.3).

1. Set SW2 to position 2 to enable the LAM.
2. Set the TDC in the range 0 to 500 ns with SW1 and SW4, and set the test one-shot in the range of 400 ns with SW3.
3. In sequence perform an F(9)NA(0), an F(25)NA(0) and an F(0)NA(0...7). The read values of all the channels must be in the range 3200±700 counts.
4. Verify that the dataway LAM line is not active.
5. Perform an F(0)NA(0...7) to verify that Q=1.
6. Perform an F(8)NA(0) to verify that Q=0.

7. Perform an F(26)NA(0) to verify that Q=1.

8. Perform an F(8)NA(0) to verify that Q=1.

9. Verify that CAMAC dataway LAM line is active.

10. Perform an F(24)NA(0) to verify that Q=1.

11. Verify that CAMAC dataway LAM line is not active.

12. Perform an F(8)NA(0...7) to verify that Q=0.

13. Perform an F(9)NA(0) to verify that Q=1.

14. Perform an F(0)NA(0...7) to verify that all the readouts are 0 and Q=0.

15. Set the TDC in the range of 0 to 5 μs with SW1 and SW4, and set the test one-shot in the range of 4 μs with SW3.

16. Perform in sequence an F(9)NA(0), an F(25)NA(0) and an F(0)NA(0...7). The read values of all the channels must be in the range 3200±700 counts.

17. Perform an F(0)NA(0...7) to verify that Q=1.

18. Perform an F(2)NA(0...6) to verify that Q=1. Then perform an F(2)NA(7) to verify that it clears the module.

19. Set the Dual Timer to generate a minimum width pulse. Then connect one output of the Dual Timer to the Common Start Input and the other output of the Dual Timer to the input of the variable delay unit (for example: Mod. N146A Programmable Delay Unit). Then connect the output of this variable delay unit, programmed with any delay value, to the Common Stop Input.

20. Perform an F(9)NA(0) to clear the module.

21. Generate a pulse with the Dual-Timer.

22. Perform an F(0)NA(0...7) to verify Q=1.

23. Set the module in the range of 0 to 100 ns with SW1 and SW4.

24. Connect the output of the delay unit to the Stop Input of Channel 1.

25. Perform an F(9)NA(0) to clear the module.

26. Generate a pulse with the Dual-Timer.

27. Perform an F(0)NA(0...7) to verify that Q=1.

28. Connect the output of the delay unit to the Fast Clear Input and generate a pulse with the Dual-Timer.

29. Perform an F(0)NA(0...7) to verify that Q=0.

30. Connect the output of the delay unit to the Stop Input of Channel 2 and generate a pulse with the Dual-Timer.

31. Perform an F(0)NA(0...7) to verify that Q=1.

32. Verify that all the channels except the one connected to the delay unit are in overflow.

33 Perform an F(9)NA(0) to clear the module.

34. Repeat the above four steps for all the 8 channels (steps 30-33).

35. Generate a pulse with the Dual-Timer.

36. Adjust the delay to be 60 ns by using the Delay Unit and measure it with the oscilloscope.

37. Read this time with the Mod. C 414 channels, by means of a CAMAC Manual Crate Controller, and verify that it is about the same as the measured time with the oscilloscope.

38. For other ranges set the dip switches SW1, SW3 and SW4 respectively for the selected range, and repeat steps 36-39 in the same sequence except substitute the Delay Unit with another Dual Timer for higher ranges.