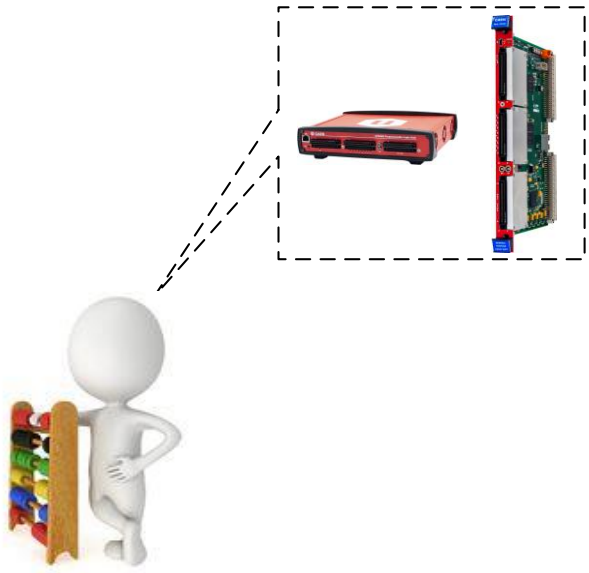
Rev. 4 - October 23rd, 2024

FW2495SC

Scaler Firmware for CAEN DT5495/V2495 Boards



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User Manual
UM5175

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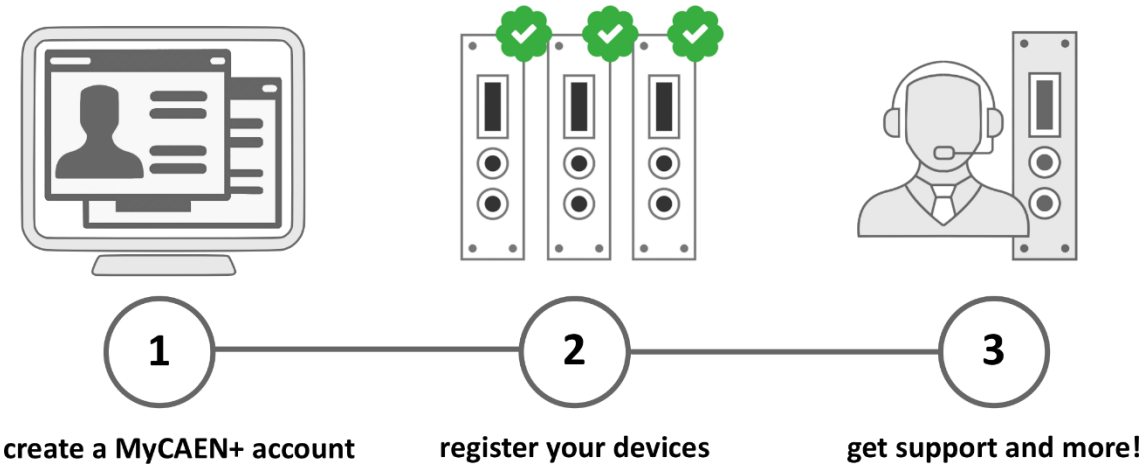

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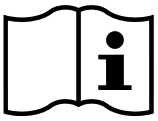
Purpose of this User Manual



This document contains the description of the FW2495SC Scaler firmware for V2495/DT5495 boards. Please, refer to the board user manual for full details about the hardware **[RD1][RD2]**.

Change Document Record

Date	Revision	Changes
November 2nd, 2016	00	Initial release
April 11th, 2019	01	Revised the entire document adding the support to the DT5495 board and describing the new PLUscaler_daq software based on the PLULib library, supported by DT5495/V2495 and back compatible with V1495.
August 29th, 2019	02	Added Sec. **TIME_BOMB** and Sec. **DB_ID**.
September 23rd, 2021	03	Added FIFO occupancy bits in Sec. **STATUS**. Updated Sec. **V2495/DT5495 CONNECTION** and Sec. **CONNECTION PARAMETERS**. Inserted DBInputType parameter description in Sec. **PLUscaler_Config FILE**.
October 23rd, 2024	04	Reviewed document layout and index. Added Sec. **4.9**. Updated Chap. **2**, Chap **6**, and Chap. **8**.

Symbols, Abbreviated Terms, and Notations

CONET	Chainable Optical NETwork
DB	Daughter Board
FPGA	Field Programmable Gate Array
MEB	Multi Event Buffer
PLU	Programmable Logic Unit

Reference Document

[RD1] UM5175 - V2495/VX2495 User Manual

[RD2] UM6508 – DT5495 User Manual

[RD3] UM11111-CAEN Toolbox User Manual

[RD4] UM3185 – CAENDPPLib User Manual

All CAEN documents can be downloaded at:

https://www.caen.it/support-services/documentation-area/ (**login required**)

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List of Figures

1 Functional Description

The FW2495SC FPGA firmware allows using the V2495 and the DT5495 as Multievent latching scalers featuring up to 160 independent counting channels, each one with a 64-bit counting depth and a maximum input frequency of 200 MHz. Each connector in slots A and B (type P50E-068-P1-SR1-TG) accepts 32 LVDS/ECL/PECL differential input channels; to implement up to 160 channels, the expansion boards Mod. A395A or A395D must be plugged in the D, E, or F slots. The Mod. A395A board features 32 differential inputs of the same type as those in slots A and B, while the Mod. A395D expansion board features 8 NIM/TTL single-ended input signals.

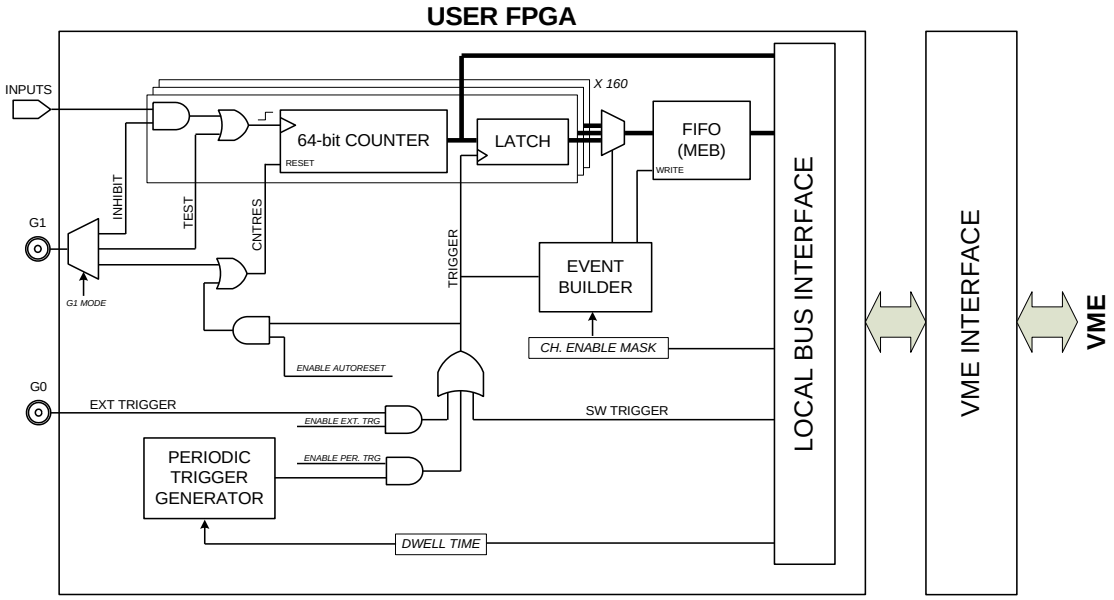

Fig. 1.1: Block diagram

Each counter is incremented at the leading edge of the input signal. As a trigger arrives, all counters are latched simultaneously and independently from the counting operations, that continue unaffected. Thanks to a synchronization technique, the counter value is significant even when it is incremented during the readout.

After the latched counter values have been made available for readout, the FPGA writes them into a FIFO memory (Multi-Event Buffer or MEB) together with a data header and, optionally, the active channel mask. Events written in the MEB can be read out via VME and USB (Ethernet link for DT5495 is not allowed for the event readout).

Once an event has been written, the Scaler can accept another trigger even if the previous event has not been read out yet, provided that the FIFO memory has enough space left for other data.

The trigger signal can be either fed to the G0 connector (NIM or TTL) or internally generated by the FPGA, with a certain trigger period (DWELL TIME) ranging from 1 µs to 4000 s in 1-µs steps. The trigger can also be sent via VME/USB, by a write access to a specific register.

The lowest 32 bits of the counter values can be also read via VME/USB on the fly, independently from the counting, trigger, and event recording operations.

The G1 connector can be used in three ways:

1. counting inhibit
2. test signal, to allow all channels counting in parallel
3. counters reset

The counters reset can be also asserted every time a trigger is sent (auto-reset option); in this way, the read values represent the counting values between two consecutive triggers instead of the absolute counting values since the board switch-on (or its last reset). The counters can also be reset via VME/USB command (see Chap. **6**).

2 Getting Started

To operate the V2495 or DT5495 with the Scaler firmware by CAEN, it is necessary to upgrade the PLU board with the latest RPD file version that is available on the FW2495SC web page.

CAEN Toolbox software must be used to upgrade the firmware (the detailed prodedure is described in the User Manual **[RD3]**).

The main steps are:

- Download the scaler firmware package and unpack it; the file format is V2495_Scaler_X.Y.rpd, where X is the major release number and Y is the minor release number.
- Launch CAEN Toolbox.
- In the main GUI:
  - select the *Programmable Logic Unit (V2495, DT5495)* option
  - Connect to the target PLU board
  - Select the destination Flash Memory page (USER_1, etc.); note that the only admitted page for DT5495 is USER_1
  - Press the *Upgrade Firmware* option
  - Browse for the RPD file on your disk and start the upgrade

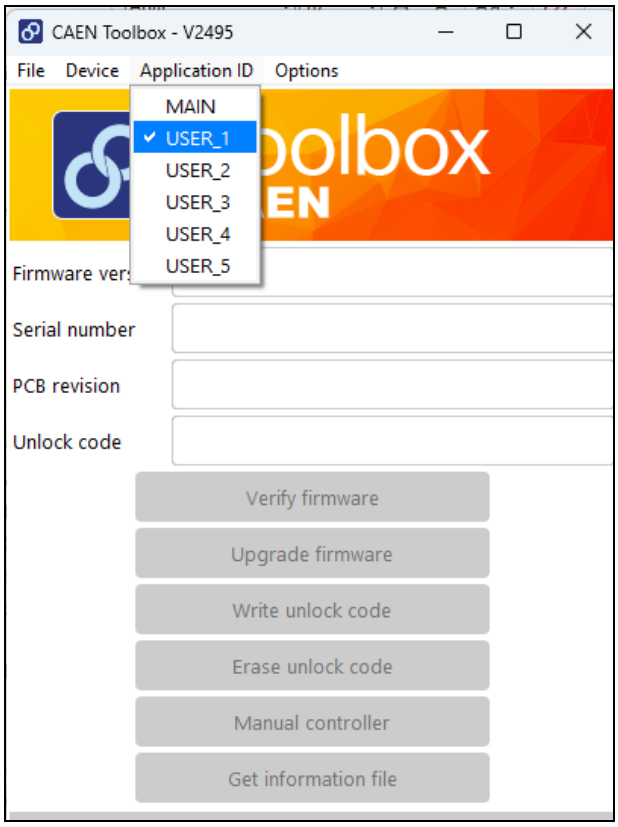

Fig. 2.1: CAEN Toolbox window

The FW2495SC is a pay firmware requiring a lincese to run without time limitation:

- Without license, the RPD file downloadable from the web page will run in trial mode for User evaluation
- In trial mode, all the firmware functions are open in a DAQ time frame of 30 minutes. Giving a power cycle (Power off/power on), another 30-minute slot begins.
- For a full-time use mode, the User must put an order for the firmware License.

The license can be purchased ex-post and the User must then write the received unlock code on the PLU board through the CAEN Toolbox. When the V2495/DT5495 board and the FW2495SC firmware are purchased by a unique order, the the Scaler firmware will be unlocked by CAEN before delivery.

3 Registers and VME Interface

All the registers of the board can be accessed in D32 USB and VME mode; for the VME, either A32 or A24 addressing can be used in any mode (USER/SUPERVISOR, DATA/PROGRAM, CR/CSR, etc.). The data space (MEB) readout can be done either via D32 single cycle or via Block Transfer (32-bit BLT). The following table reports the FPGA USER address offsets, to be added to the module's base address; the FPGA VME address offsets are the same as those reported in the V2495 and DT5495 User Manuals **[RD1][RD2]**.

Register Name	Description	Address	Mode
MEB	Multi Event Buffer	0x0000(*)	R
ACQ_CTRL	Control Register	0x1000	R/W
ACQ_CTRL_SET	Control Register BitSet	0x1004	R/W
ACQ_CTRL_CLR	Control Register BitClear	0x1008	R/W
FWREV	Firmware Revision	0x100C	R
STATUS	Status Register	0x1010	R
COMMANDS	Commands Register	0x1014	W
CHEN_A	Channel Enable Mask for the group A	0x1020	R/W
CHEN_B	Channel Enable Mask for the group B	0x1024	R/W
CHEN_D	Channel Enable Mask for the group D	0x1028	R/W
CHEN_E	Channel Enable Mask for the group E	0x102C	R/W
DWELL_TIME	Dwell Time (period of the internal trigger)	0x1030	R/W
CHEN_F	Channel Enable Mask for the group F	0x1034	R/W
DB_ID	IDs of the daughterboards in D, E, F (if any)	0x1038	R
TIME_BOMB	Time Bomb counter	0x1040	R
CONTROL_C	Port C Control	0x1044	R/W
COUNTERS_A	Direct read access to the counters of the group A (lower 32 bits)	0x1100 – 0x117C	R
COUNTERS_B	Direct read access to the counters of the group B (lower 32 bits)	0x1180 – 0x11FC	R
COUNTERS_D	Direct read access to the counters of the group D (lower 32 bits)	0x1200 – 0x127C	R
COUNTERS_E	Direct read access to the counters of the group E (lower 32 bits)	0x1280 – 0x12FC	R
COUNTERS_F	Direct read access to the counters of the group F (lower 32 bits)	0x1300 – 0x137C	R

Fig. 3.1: Registers map

(*) any address between 0x0000 and 0xFFFC is mapped onto the MEB

4 Registers Description

4.1 ACQ_CTRL

address 0x1000, 0x1004, 0x1008; mode R/W

Bit	Name	Description
[0]	EN_EXTTRG	0 => External Trigger Disabled 1 => External Trigger Enabled
[1]	EN_INTTRG	0 => Internal Trigger Disabled 1 => Internal Trigger Enabled
[2]	G_PORT_TYPE	0 => G ports input signal type is NIM 1 => G ports input signal type is TTL
[3]	AUTO_RESET	0 => AutoReset Disabled 1 => The counters are reset with the trigger
[5:4]	G1_MODE	[00] => G1 is used as INHIBIT [01] => G1 is used to reset the counters [10] => G1 is used as TEST SIGNAL [11] => *reserved*
[6]	EN_TIMETAG	0 => Time Tag not reported in the event data 1 => Time Tag reported in the event data
[7]	EN_MASK	1 => The channel mask of a specific group is written at the beginning of the group data block if at least one channel of the mask is active
[8]	EN_64BITCNT	1 => The upper 32 bits of the event counters are written in the data stream (in addition to the lower 32)
[9]	EN_64BITTIME	1 => The upper 32 bits of the timestamp are written in the data stream (in addition to the lower 32)
[10]	EN_V2495_FORMAT	0 => The data format used by the V1495 module is used (see below). In this format only bit [6] (time tag enabling) is meaningful 1 => The new V2495/DT5495 data format is used (see below)
[11]	TEST_CLK	0 => Test Clock disabled 1 => The board clock is provided on the C port and can be used as a test for counters if fed as input to the board itself
[14:12]	INPUT_LEVEL	0 => The input signal to the A395D in slot [D-E-F] is NIM 1 => The input signal to the A395D in slot [D-E-F] is TTL This setting is meaningless for other mezzanine board types
[31:15]	*RESERVED*	*reserved*

4.2 FWREV

address 0x100C; mode R Only

This read-only register reports the FPGA USER firmware revision with the following format (32-bit):

YMDDMMmm (each letter corresponds to one nibble)

Y = year (e.g. 0 stands for 2016)

M = month (1 =JAN, C = DEC)

DD = day (decimal; e.g. '12' stands for 12)

MM = major number = 0x81 (129 decimal code corresponding to Scaler)

mm = minor number (example: if mm = 2, version is 129.2)

4.3 STATUS

address 0x1010, mode R Only

Bit	Name	Description
[0]	MEB FULL	When 1, the MEB is full and no more triggers can be accepted until the MEB is read and there is enough space to write an event
[3:1]	RESERVED	*reserved*
[15:4]	MEB OCCUP	MEB occupancy (in 32-bit words)
[31:16]	RESERVED	*reserved*

4.4 COMMANDS

address 0x1014; mode W Only

Write access to this register allows the FPGA to execute one or more commands; bit must be set to one to perform the corresponding function. It is not necessary to write 0 to reset the bit as each bit automatically resets.

Bit	Name	Description
[0]	SWTRG	Generates a software trigger (not maskable)
[1]	SWCNTRES	Reset to 0 all counters
[2]	SWCLR	Clear MEB
[3]	BDRESET	Board reset
[31:4]	SWTRG	Generates a software trigger (not maskable)

4.5 CHEN_X

address 0x1020, 0x1024, 0x1028, 0x102C, 0x1034; mode R/W

This register allows to enable the channels of A (*0x1020)*, B (*0x1024)*, D (*0x1028)*, E (*0x102C)* and F (0x1034) connectors; the 32 bits of each register correspond to the relevant channel on the connector (1 = ch enabled).

4.6 DWELL_TIME

address 0x1030; mode R/W

This register allows setting the internal trigger period: T_{TRG} = N * 1µs.

With N = register value (32 bit); the internal trigger can be enabled by setting bit 1 of the Control Register.

4.7 DB_ID

address 0x1038; mode R

This register contains the information on which A395x mezzanine board is possibly mounted on the board.

Bit	Name	Description
[2:0]	IDx	Mezzanine Board Identifier: 000 => A395A 001 => A395B 010 => A395C 011 => A395D 100 => A395E 111 => No mezzanine board is present
[31:3]	RESERVED	*reserved*

4.8 TIME_BOMB

address 0x1040; mode R

This is the register of the count-down counter of the FW2495SC and can be used to check whether the Scaler firmware is licensed or not. The 32-bit default value of 0x0708 remains constant in the case of licensed firmware, while start decreasing after the power-on of the V2495/DT5495 if the firmware is not licensed.

4.9 CONTROL_C

Address 0x1044; mode R/W

This register allows setting the logic level of each output of the C port. The status of these outputs is controlled by default by this register.

Alternatively, it is possible to send the same clock signal on all the outputs by register ACQ_CTRL (see Sec**. 4.1**).

Bit	Name	Description
[31:0]	-	Each bit sets the logic level of the relevant C output. 0 => logic level low 1 => logic level high

4.10 COUNTERS_X

address from 0x1100 to 0x137C; mode R Only

Read access to one of these addresses allows reading “on the fly” the value of the 32 LSBs of the corresponding counter. The address of each channel is given by 0x1100 + 32*C + N*4, where C is the connector index (from 0 to 5, corresponding to connectors A, B, D, E, F) and N is the channel index within a specific connector.

5 Event Data Format

If bit[10] = 0 of ACQ_CTRL register, the event payload is organized as shown in **Fig. 5.1**.

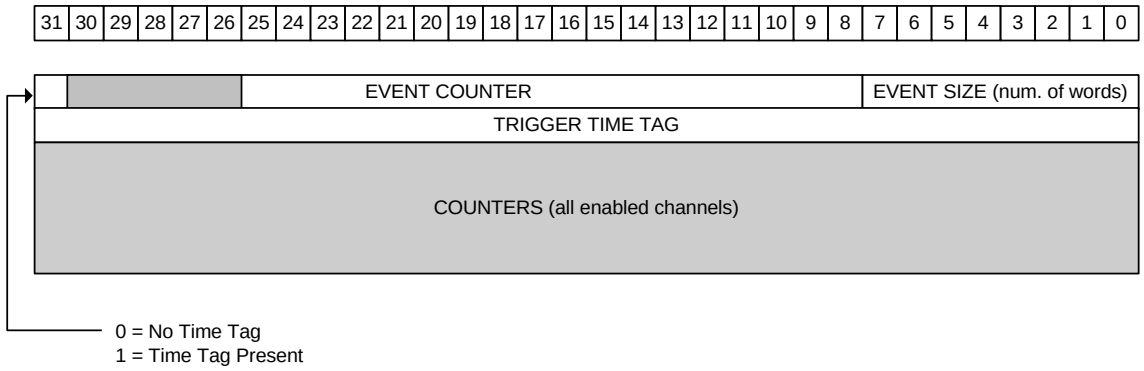

Fig. 5.1: Event data format compliant to V1495

This data format replicates the payload of the scaler firmware developed for the V1495 CAEN board, so that acquisition systems developed for the V1495 should be compatible with the V2495 scaler firmware when this bit is set to 0.

The Trigger Time Tag can be optionally included in the event structure by setting bit[6] of the ACQ_CTRL register; if enabled, it represents the arrival time of the trigger (µs) from the latest board reset. The MSB of the first word indicates whether the Trigger Time Tag information has been added (1) or not (0) to the event.

Counter values are in sequential order; no channel mask is foreseen in the packet so that the information on which channels are present can be obtained only by accessing the CHEN_X registers.

Setting bit[10] = 1 of ACQ_CTRL register, produces a new event payload whose structure is described below.

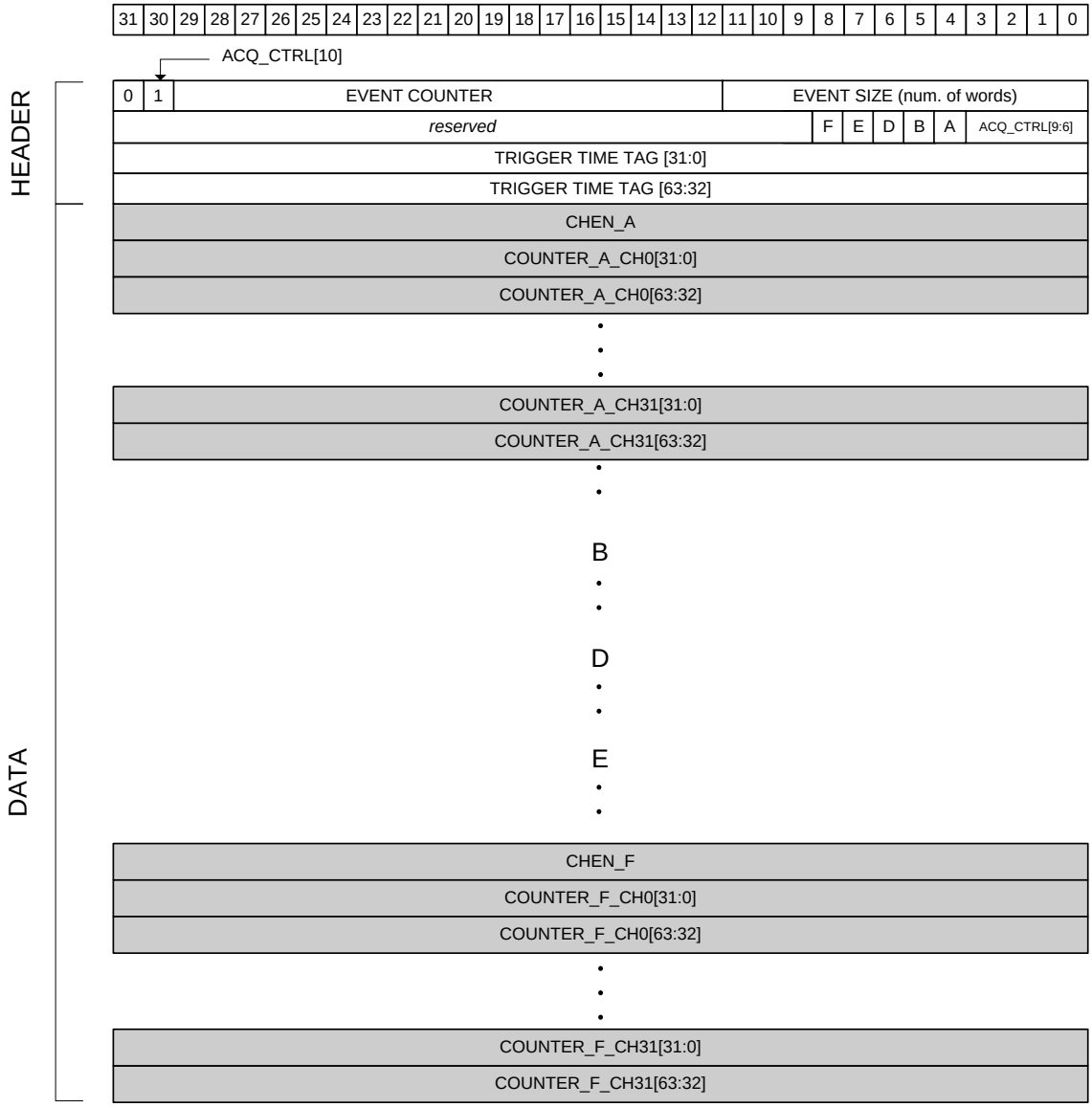

Fig. 5.2: Event data format compliant to V2495/DT5495

In the new V2495/DT5495 data format, the event is made by a HEADER and a DATA block.

5.1 HEADER

The HEADER block includes from 2 to 4 32-bit words, according to the Trigger Time Tag information is set or not to be added to the event.

- The 1st word includes the Packet Type Flag (bit[30]), i.e. bit[10] of the ACQ_CTRL register, the Event Size (12 bits), i.e. the size of the event expressed in number of 32-bit words, and the Event Counter (18 bits).
- The 2nd word includes the value of the four enable bits of the ACQ_CTRL register (ACQ_CTRL bit[9:6]) and the five bits (A, B, D, E, F): the bit X is 1 only if the CHAN_X register is non-zero, i.e. only if port X has at least one active channel. Please, refer to Chap. **3** for the detailed description.
- The 3rd word represents the lower 32 bits of the Trigger Time Tag counter. It is added to the event only if bit[6] of the ACQ_CTRL register is set to 1.
- The 4th word represents the upper 32 bits of the Trigger Time Tag counter. It is added to the event only if bit[6] and bit[9] of the ACQ_CTRL register are both set to 1.

5.2 DATA

This block of the event is the data stream structure, which can be of variable size and includes the information on the channel enable masks, CHEN_X, and the channel counter data, COUNTER_X_CHY.

The channel enable mask word of group X (X = A, B, D, E, F) is added to the event only if:

- CHEN_X register ≠ 0 (i.e. at least one channel of group X is enabled)
- ACQ_CTRL bit[7] = 1 (see Chap **3**)

The 32 LSBs of the Yth channel counter are added to the data block of group X if:

- The Yth bit of the correspondent group mask is set to 1.

The 32 MSBs of the Yth channel counter are added to the data block of group X if:

- The Yth bit of the correspondent group mask is set to 1 and ACQ_CTRL bit[8] = 1 (see Chap.**3**).

6 PLUscaler_daq Software

PLUscaler_daq is a CAEN software available for Windows® and Linux® that allows managing data acquisition with the FW2495SC firmware. The package includes the source code as a base for the user development of customized applications.

To set the Scaler firmware, the software uses a configuration text file which is parsed at the run (see Chap. **7**).

System requirements:

- CAENComm library (latest official version recommended)
- PLULib library rev. 1.4.1 or higher **[RD4]**
- Microsoft Windows OS or Linux OS
- Gnuplot 4.2 or higher (www.gnuplot.info)

6.1 PLUscaler_daq INSTALLATION

To install the PLUscaler_daq software:

- Make sure that the USER FPGA is upgraded with the FW2495SC firmware (Chap. **2**)
- Go to www.caen.it and browse for the **FW2495SC** web page
- Download the PLUscaler_daq installation package in the Downloads -> Software area
- For Linux® and Windows®, unpack and follow the installation instructions in the README or INSTALL file
- For Linux® only, issue the commands /configure, *mak"*, and *sudo make install* in sequence to compile the software package

Windows default destination path is *C:\Program Files\CAEN\PLULibrary*

6.2 V2495/DT5495 CONNECTION

To run the PLUscaler_daq software on Windows OS:

- Open the DOS command line (*cmd*)
- Go to *\PLULibrary\PLUscaler_daq\bin*
- Issue the command *PLUscaler_daq* followed by the required connection parameters
- To check which is the required syntax, issue the command *PLUscaler_daq -h* and the following message will be displayed:

  PLUscaler_daq [config file path](default: ./PLUScaler_Config.txt) [-h] [-c usb-direct|eth-direct|usb-V1718|usb-V3718|opt-V2718|opt-V3718|opt-V4718][eth-V4718][usb-V4718][usb-A4818] [-b vme base address] [-ip ipaddress] [-sn serial number]

To run the PLUscaler_daq software on Linux OS:

- Go to */PLUScaler_daq/build/*
- Issue *./PLUscaler_daq* followed by the configuration file path and the connection parameters according to the same syntax as described for Windows®. A copy of the configuration file is stored in */etc/pluscaler_daq/*.

Refer to Chap. **7** for a practical example.

6.3 CONNECTION PARAMETERS

The connection parameters to be used with the PLUscaler_daq software are described below:

- "c": connection type -> the identifier of the active communication link

  The possible values can be:

  - *usb-direct* = USB direct link
  - *eth-direct* = Ethernet direct link
  - *usb-V1718* = USB-to-VME through the V1718 CAEN Bridge
  - *usb-V3718* = USB-to-VME through the V3718 CAEN Bridge
  - *opt-V2718* = CONET-to-VME through the V2718 CAEN Bridge
  - *opt-V3718* = CONET-to-VME through the V3718 CAEN Bridge
  - *opt-V4718* = CONET-to-VME through the V4718 CAEN Bridge
  - *eth-V4718* = Ethernet-to-VME through the V4718 CAEN Bridge
  - *usb-V4718* = USB-to-VME through the V4718 CAEN Bridge
  - *usb-A4818* = CONET-to-VME through the A4818 CAEN USB3-to-CONET adapter
- "sn": device serial number -> the serial number (or the PID) of the target board (or of the A4818 or V4718, see **Tab. 6.1**); the software accepts only serial number values on 4 digits (example: 1204 and 0023 are correct serial number values). In the case of devices associated with a PID number (instead of the old serial number), the user should write down the PID, i.e. a 5-digit numerical value.
- "ip": IP address -> the IP address of the target board (or of the V4718, see **Tab. 6.1**).
- "b": VME base address -> the VME Base Address of the target board; this parameter is meaningful only in case of connecting to the V2495 board through a CAEN Bridge (V4718/V3718/V2718/V1718).

In **Tab. 6.1**, the available connection chains are presented together with the corresponding values to be inserted for the connection parameters.

Connection chain	Conn. Type	Serial Num.	IP Addr.	VME Base Addr.
PC –> **USB** –> V2495/DT5495	usb-direct	SN/PID (*)	/	/
PC –> **ETH** –> DT5495	eth-direct	/	IP (**)	/
PC –> **USB** –> V1718 –> **VME** –> V2495	usb-V1718	/	/	VBA (***)
PC –> **USB** –> V3718 –> **VME** –> V2495	usb-V3718	/	/	VBA (***)
PC –> **PCI/PCIe** –> A2818/A3818 –> **CONET** –> V2718 –> **VME** –> V2495	opt-V2718	/	/	VBA (***)
PC –> **PCI/PCIe** –> A2818/A3818 –> **CONET** –> V3718 –> **VME** –> V2495	opt-V3718	/	/	VBA (***)
PC –> **PCI/PCIe** –> A2818/A3818 –> **CONET** –> V4718 –> **VME** –> V2495	opt-V4718	/	/	VBA (***)
PC –> **ETH** –> V4718 –> **VME** –> V2495	eth-V4718	/	IP (+)	VBA (***)
PC –> **USB** –> V4718 –> **VME** –> V2495	usb-V4718	PID (++)	/	VBA (***)
PC –> **USB** –> A4818 –> **CONET** –> V2718/V3718/V4718 –> **VME** –> V2495	usb-A4818	PID (+++)	/	VBA (***)

Tab. 6.1: Available connections to the V2495/DT5495 via the PLUscaler_daq software and corresponding connection parameters.

(*) The serial number or PID of the V2495/DT5495 board (e.g. 15741).
(**) The IP address of the DT5495 board (e.g. 192.168.0.90).
(***) The VME Base Address of the V2495 board (e.g. 32100000).
(+) The IP address of the V4718 bridge.
(++) The PID of the V4718 bridge.
(+++) The PID of the A4818 USB-to-CONET adapter.

Example: If the user wants to communicate with the V2495 via VME bus through a V2718 and an A4818, the following command should be used (Windows):

PLUscaler_daq -c usb-A4818 -b 32100000 -sn 15105

Being 32100000 the VME base address of the V2495 and 15105 the A4818 PID.

6.4 OFFLINE MODE

The PLUscaler_daq software can work offline. The user can import previously saved output binary files for offline analysis (see Chap. **7**).

To run the PLUscaler_daq software offline, optionally:

- run the executable file by DOS command line or Linux shell without parameters
- double click on the software desktop shortcut (Windows® only), if any
- double click on the executable file in *PLULibrary**PLUscaler_daq**bin*\ (Windows® only)

6.5 PLUscaler_Config FILE

```
# ------------------------------------------------------------------------------
ChEnableA         FFFFFFFF
ChEnableB         FFFFFFFF
ChEnableD         00000000
ChEnableE         00000000
ChEnableF         00000000
```

ChEnableX hexadecimal value represents the 32-bit mask to enable the presence of the channel counters of the X connector (X = A, B, D, E, F) inside the data packet. The bit position in the mask corresponds to the channel number.

Example: set `ChEnableA  0000A000` to enable only channel 15 and channel 13 of the A connector.

If the mezzanine type plugged onto the V2495/DT5495 hosts less than 32 channels (e.g. the 8-channel A395D), the unsupported channels will be masked.

```
# ------------------------------------------------------------------------------
# Counters are reset each time they are readout (0=disabled, 1=enabled)
# ------------------------------------------------------------------------------
AutoReset         1
```

This flag allows enabling the auto-reset option. The counters will be reset at each trigger arrival so that each counter reading represents the counting between two consecutive triggers.

```
# ------------------------------------------------------------------------------
# Trigger Source
# 0 = SW only
# 1 = External + SW
# 2 = Internal + SW
# 3 = External + Internal + SW
# ------------------------------------------------------------------------------
TriggerMode       2
```

This parameter selects the source or combination (OR) of sources providing the trigger for the acquisition.

```
# ------------------------------------------------------------------------------
# Dwell Time (period of the internal trigger) in usec
# ------------------------------------------------------------------------------
DwellTime         100000
```

If the internal trigger source is selected through the *TriggerMode* parameter, this parameter sets the period of the internal trigger (in units of µs).

```
# ------------------------------------------------------------------------
# Save time tag in the event data (0=disabled, 1=enabled)
# Ch_Mask, TimeTag_64 and CVcounter_64 are meaningful only when V2495_Payload is set to 1
# ------------------------------------------------------------------------
TimeTag          1
Ch_Mask          1
TimeTag_64       0
Counter_64       0
V2495_Payload    1
```

This is a set of information regarding the event format.

- *TimeTag* = 1 makes the time tag information to be added to the event structure
- *Ch_Mask* = 1 makes the mask of the enabled channels to be added to the event structure

Note: Ch_Mask must be set to 1 to save a binary file for further offline analysis (see Chap. **7**).

- *TimeTag_64* = 1 makes the 64-bit time tag information to be added to the event structure
- *Counter_64* = 1 makes the 64-bit counter information to be added to the event structure

Note: *Ch_Mask*, *TimeTag_64* and *Counter_64* are meaningful only if *V2495_payload* = 1.

- *V2495_Payload* configures the legacy, V1495 compliant event format (value = 0) or the V2495 new event format (value = 1)

Note: *V2495_Payload* must be set to 0 if running the program when connected to a V1495.

```
# ------------------------------------------------------------------------
# Input Port G1:
# 0 = inhibit
# 1 = counter reset
# 2 = test
# ------------------------------------------------------------------------
G1Mode           0
```

G1Mode parameter must be used to set the function of the G1 front panel port.

```
# ------------------------------------------------------------------------
# G Ports type:
# 0 = NIM
# 1 = TTL
# ------------------------------------------------------------------------
GPortType        0
```

GportType sets the logic level of G0 and G1 front panel ports: NIM/TTL.

```
# ------------------------------------------------------------------------
# Daughterboard Input type (only relevant for A395D)
# All 3 DBs are set to the same input type (each can be set independently using bits [14:12] of the control register)
# 0 = NIM
```

```
# 1 = TTL
# ------------------------------------------------------------------------------
DBInputType       0
```

DBInputType sets the logic level of the LEMO front panel connectors of all the A395D piggybacks mounted on the board: NIM/TTL. The user can set a different logic level for each A395D piggyback via register access (see Sec. **4.1**).

```
# ------------------------------------------------------------------------------
# Enable saving to output File. The file can be chosen at runtime
# ------------------------------------------------------------------------------
SaveToFile        0
```

This is the output file saving enable. By setting *SaveToFile* to 1 before running the software, the output stream from the V2495 is saved in binary format. The user will be runtime asked to enter the file name (see Chap. **7**).

```
# ------------------------------------------------------------------------------
# Enable 50 MHz clock output on port C (all channels, can be used to test
counters)
# ------------------------------------------------------------------------------
TestClock         1
```

When *TestClock* is enabled (parameter value = 1), the C connector provides out a 50-MHz test clock on all the channels. These signals can be used as test inputs for the A and B ports and the A395A connector (see Chap. **7**).

```
# ------------------------------------------------------------------------------
# Plot Options
# OpenPlot:   0 = plot disabled;   1 = plot enabled
# PlotChan: channel to be plotted in the count vs time graph
# PlotPoints: number of points on the X axis of the plot
# SWTrigTime: Seconds between two consecutive SW triggers when periodic SW
trigger is active (hit 'T' at runtime)
# PrintCounters: activate the on-screen counter display after each VME access
(with "ReadingTime" frequency)
# ReadingTime: Seconds between two consecutive event data printouts (minimum 1)
#   ------------------------------------------------------------------------------
OpenPlot          0
PlotChan          1
PlotPoints        100
SWTrigTime        1
PrintCounters     1
ReadingTime       1
```

In this section of the configuration file, it is possible to enable (*OpenPlot* = 1) the simultaneous counter histogram and Counts-vs-Time plot of *PlotChan* (ranging from 0 up to 159; the related channel in the output stream must be activated), the maximum number of points to be collected in the Counts-vs-Time plot (*PlotPoints*), the time in seconds (*SWTrigTime*) between two consecutive counter readings when the loop mode is enabled (periodic software trigger by Windows DOS command line / Linux shell), the possibility to display the readout data (*PrintCounters*) in the Windows DOS command line / Linux shell, and the refresh time (*ReadingTime*) of the readout data being displayed (*PrintCounters* = 1).

7 PLUscaler_daq Example

This chapter describes a practical use of the PLUscaler_daq software with a DT5495 in a simple test.

7.1 DWELL TIME TEST

The internal 50-MHz test clock signal out on the C port is used as input for all the channels of the A port of the DT5495. By enabling the counter autoreset function, the counter of each channel is reset to zero each time that a trigger arrives. In this way, the readout of the counter value represents the count between two consecutive triggers. Setting the DwellTime parameter to 1.000.000 (i.e. 1 s), the readout count must be equal to 50.000.000, that is the 50-MHz input test clock.

Fig. 7.1: A and C ports of the DT5495 shortcircuited by a Robinson-Robinson cable

The user should perform the following steps with the PLUscaler_daq software:

1. In the PLUscaler_Config file, set the most significant parameters for the test:

```
AutoReset       1        # autoreset function is enabled
TriggerMode     2        # trigger source is internal OR software
DwellTime       1000000  # time between two internal triggers is 1 s
TestClock       1        # the 50-MHz test clock on the C port is enabled
```

   Save the file after the modifications.

2. Run the software executable file followed by the connection parameters (USB link in this example):

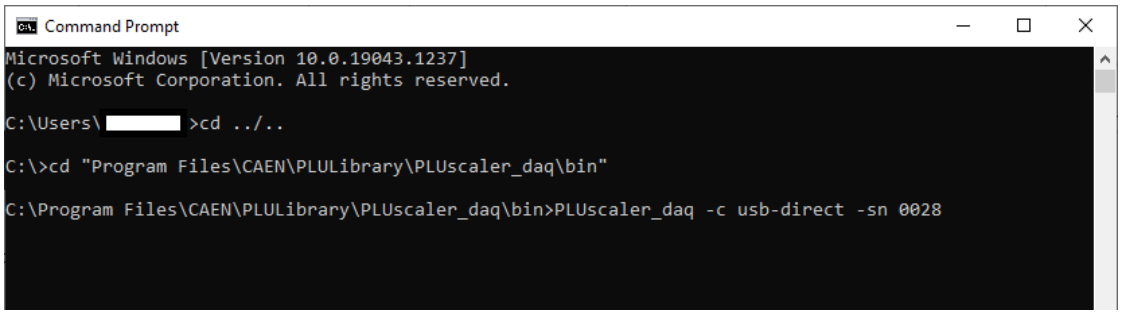

Fig. 7.2: PLUscaler_daq launched in Windows Command Prompt

3. The software connects to the target board and automatically starts to acquire data that are displayed in the Windows Command Prompt window. Two plots open automatically as well, the count-vs-time curve and the count-vs-channel histogram, which are related to the channel enabled in the PLUscaler_Config file (channel 0 by default).

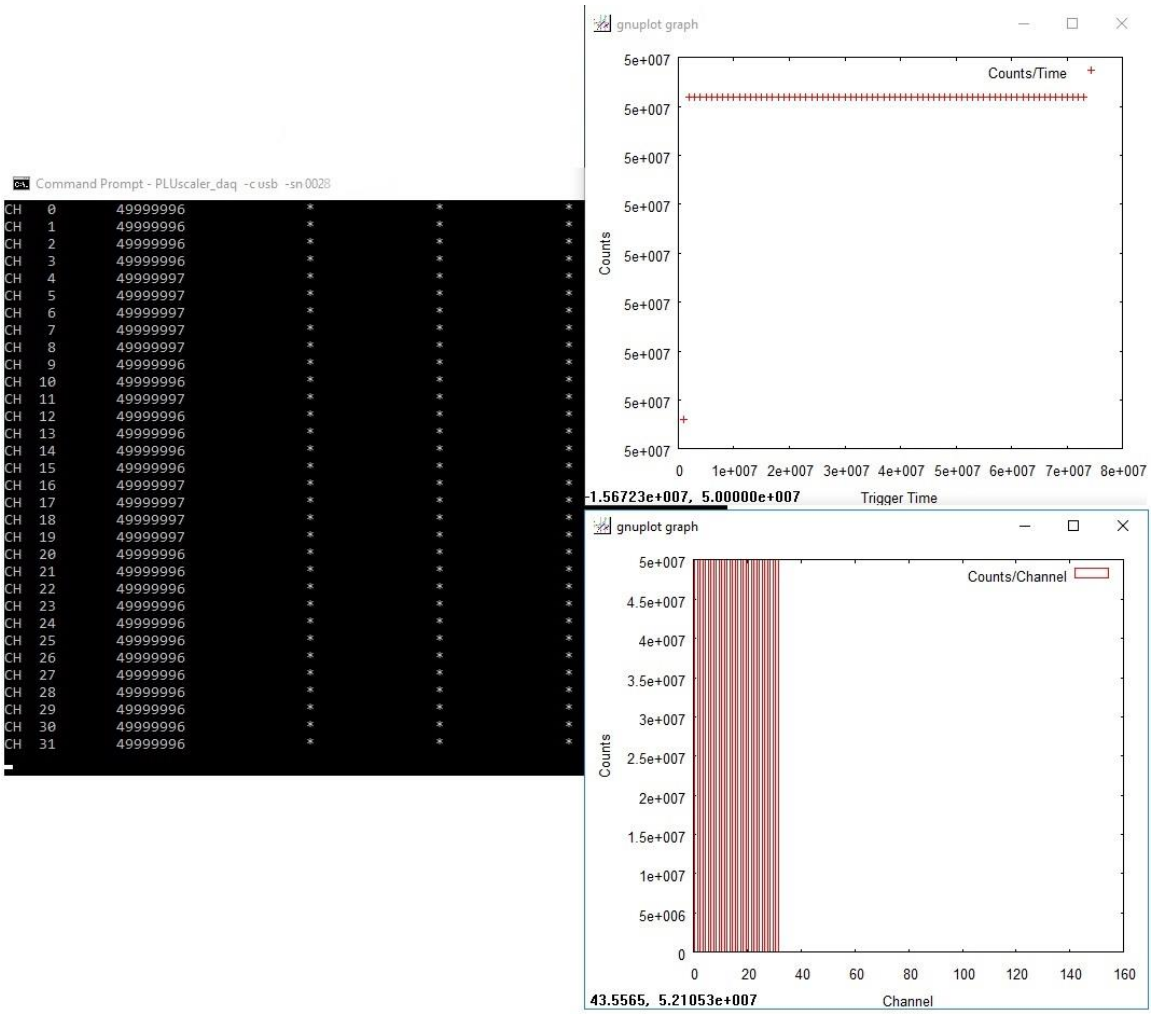

Fig. 7.3: PLUscaler_daq displayed data and plots

In **Fig. 7.3**, the second column in the Command Prompt displays the counter readings per channel within two consecutive triggers, which is essentially 50.000.000 as expected. Aside up, the count-vs-time plot reports correctly a series of points that are substantially at the same value of 50.000.000 as expected. Aside from down, the count-vs-channel histogram reports the same value of 50.000.000 counts per each of the 32 channels, as expected.

8 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

https://www.caen.it/support-services/getting-started-with-mycaen-portal/

All the instructions for use the Support platform are in the document:

A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

https://www.caen.it/safety-information-product-support

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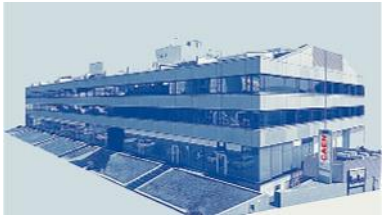

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