



Rev. 5 - October 8th, 2024

V2495

VME Programmable Logic Unit



Register your device

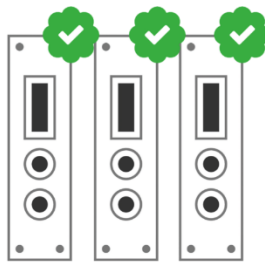
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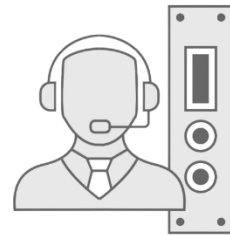
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Purpose of this Manual



This document contains the full hardware and software description of the V2495 VME Programmable Logic Unit.

Change Document Record

Date	Revision	Changes
August 01 st , 2016	00	Initial release
October 11 th , 2018	01	Removed "Coming Soon" from the User Firmware FW2495SC in Tab. 1.2 . Corrected caption in Fig. 13.2 . Removed Sec. "CAENComm Demo" and added Sec. PLULib Library in Sec. Software Tools . Updated Sec. Reference Documents , Sec. Flash Configuration (0x8500-0x8AFF) , Sec. Introduction , Chap. 15 .
May 30 th , 2019	02	Added Sec. PLUscaler_daq and Chap. 15 . Updated Sec. Direct USB Driver and Sec. Technical Support Service .
August 29 th , 2019	03	Removed "Preliminary" from the document and "Product Code" column from Tab. 1.2 . Updated Tab. 6.5 with impedance information and instructions on the A395D channel impedance selection. Removed Sec. 14.1 and Sec. 14.2 and renamed Chap. Errore. L'origine riferimento non è stata trovata.
March 31 st , 2023	04	Added Sec. 13.1 , Sec. 13.1.1 , and Sec. 13.3.1
October 8 th , 2024	05	Removed the obsolete VME64X model (VX2495). Added Chap. 7 , Chap. 8 . Updated Sec. 9.3 . Updated Sec. 11.1.2 . Replaced CAEN Upgrader description (obsolete) with CAEN Toolbox in Sec. 11.2 . Updated the PID description in Sec. 12.3.9 . Updated LAD signal width in Tab. 13.8 . Updated Chap. 1 .

Symbols, Abbreviated Terms and Notation

AM	Address Modifier
FPGA	Field Programmable Gate Array
GA	Geographical Address
GDG	Gate and Delay Generator
LB	Local Bus
LBM	Local Bus Master
LBS	Local Bus Slave
LED	Light Emitting Diode
MFPGA	Main FPGA
SPI	Serial Peripheral Interface
SW	Switch
UFPGA	User FPGA
USB	Universal Serial Bus
VBA	VME Base Address
VME	Versa Module Europa

Reference Documents

[RD1] UM11111 – CAEN Toolbox User Manual Guide

[RD2] UM3181 – V1495 General Purpose VME Board

[RD3] A967 Adapter for P50E – 068S 68 Pin Connectors

[RD4] UM6510 – CAEN PLULib Library User Manual

[RD5] UM5175 – FW2495SC - DT5495 V2495 Scaler Firmware User Manual

All documents can be downloaded at: <https://www.caen.it/support-services/documentation-area/>

Manufacturer Contacts



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Limitation of Responsibility

If the warnings contained in this manual are not followed, CAEN will not be responsible for damage caused by improper use of the device. The manufacturer declines all responsibility for damage resulting from failure to comply with the instructions for use of the product. The equipment must be used as described in the user manual, with particular regard to the intended use, using only accessories as specified by the manufacturer. No modification or repair can be performed.

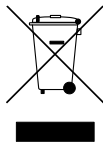
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Made in Italy

We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (this is true for the boards marked "MADE IN ITALY", while we cannot guarantee for third-party manufactures).



Index

Purpose of this Manual	2
Change Document Record	2
Symbols, Abbreviated Terms and Notation	2
Reference Documents.....	2
Manufacturer Contacts	3
Limitation of Responsibility	3
Disclaimer.....	3
Made in Italy.....	3
Index	4
List of Figures.....	5
List of Tables	6
Safety Notices.....	7
1 Introduction.....	10
2 Block Diagram	12
3 Main Components and Interconnections.....	13
3.1 USB Interface.....	14
3.2 VME Interface	14
3.3 Main FPGA.....	14
3.4 User FPGA	14
3.5 Gate and Delay Generator.....	14
3.6 Clock Distribution	14
4 Front Panel Connectors, LEDs and Labels	15
5 Internal Connectors and LEDs	18
6 Technical Specifications	21
7 Packaging and Compliancy	23
8 PID (Product Identifier).....	25
9 Getting Started with V2495	26
9.1 Expansion Mezzanines	26
9.2 Mezzanine Boards Installation	26
9.3 Front Panel Connector Cabling.....	27
9.4 Setting the VME Base Address.....	28
9.5 Selecting the User FPGA Firmware	28
10 Power-on Configuration Sequence.....	29
10.1.1 Boot Mode Selection	29
11 Driver and Software Installation.....	30
11.1 Drivers.....	30
11.1.1 Direct USB Driver.....	30
11.1.2 VME Access.....	33
11.2 Software Tools.....	34
11.2.1 CAEN Toolbox.....	34
11.2.2 PLULib Library.....	35
11.2.3 PLUscaler_daq.....	35
12 Communication Interfaces.....	36
12.1 VME Bus.....	36
12.2 USB.....	36
12.3 Address Map.....	36
12.3.1 User FPGA Data Access (0x0000-0x0FFF).....	36
12.3.2 User FPGA Register Access (0x1000-0x7FFF).....	37
12.3.3 VME Interface Registers (0x8000-0x80FF).....	37
12.3.4 VME Control Register.....	37
12.3.5 VME Interrupt Level Register	37
12.3.6 VME Interrupt Status ID Register	37
12.3.7 Scratch Register.....	37
12.3.8 VME Base Address Register.....	38

12.3.9	Configuration ROM (0x8100-0x81FF).....	38
12.3.10	Configuration and Status Registers (0x8200-0x83FF)	39
12.3.11	MFPGA Firmware Revision Register	39
12.3.12	Software Reset Register	39
12.3.13	Scratch Register.....	39
12.3.14	Flash Configuration (0x8500-0x8AFF).....	39
12.3.15	Internal Scratch SRAM(0x8C00-0x8FFF).....	39
13	Firmware Development.....	40
13.1	Introduction.....	40
13.1.1	Safety Notice	40
13.2	User FPGA I/O Ports	41
13.2.1	Preventing from User FPGA Input Conflicts.....	44
13.3	Local Bus Interface	45
13.4	Gate and Delay Controller	47
13.4.1	General Description.....	47
13.4.2	Register Description	48
13.4.3	Example Procedures	49
13.5	Porting V1495 to V2495	50
14	Demo Firmware	51
14.1	Introduction.....	51
14.2	Demo Structure	51
14.3	Demo Setup	51
14.4	Gate Pattern Demo Description	52
14.4.1	Introduction	52
14.4.2	Register Map	52
14.4.3	Register Description	52
14.5	Pattern Recorder Demo Description	55
14.5.1	Introduction	55
14.5.2	Register Map	55
14.5.3	Register Description	55
14.6	DAC Demo Description	57
14.6.1	Introduction	57
14.6.2	Register Map	57
14.6.3	Register Description	57
14.7	Gate and Delay Demo Description	59
14.7.1	Introduction	59
14.7.2	Register Map	59
14.7.3	Register Description	59
15	FW2495SC Pay Firmware.....	62
16	Software Development	63
17	Technical Support.....	64

List of Figures

Fig. 2.1:	Block diagram	12
Fig. 3.1:	Main components and interconnections.....	13
Fig. 3.2:	The UFPGA and GDG interface.....	14
Fig. 4.1:	Front panels view	15
Fig. 5.1:	On-board internal connectors and LEDs.....	18
Fig. 8.1:	PID location on the device (the number and board model in the pictures are purely indicative)	25
Fig. 9.1:	Mezzanine boards for the V2495	26
Fig. 9.2:	V2495 motherboard hosting the mezzanine boards.....	26
Fig. 9.3:	Multi-pin connector pin assignment	27
Fig. 9.4:	CAEN A967 Cable Adapter.....	27
Fig. 9.5:	Base Address on-board rotary switches	28
Fig. 9.6:	User Firmware rotary switch	28
Fig. 10.1:	Boot mode jumper for the Main FPGA	29
Fig. 11.1:	V2495 hardware detection	30
Fig. 11.2:	USB driver manual installation: Step1	31
Fig. 11.3:	USB driver manual installation: Step2.....	31
Fig. 11.4:	USB driver manual installation: Step3.....	32

Fig. 11.5: USB driver manual installation: Step432
 Fig. 11.6: USB driver manual installation: Step533
 Fig. 11.7: CAEN Toolbox Graphical User Interface34
 Fig. 11.8: CAEN PLULib Demo application prompt35
 Fig. 11.9: PLUscaler_daq prompt.....35
 Fig. 13.1: A395 jumpers for the channel impedance selection42
 Fig. 13.2: Simplified scheme related to Tab. 13.5.....43
 Fig. 13.3: Local bus signals at a write access (x8BADF00D is written on register x1800)45
 Fig. 13.4: Local bus signal at a read access (x8BADF00D is read from register x1800)45
 Fig. 13.5: Prefetch mechanism46
 Fig. 13.6: Gate and Delay parameters representation47







List of Tables

Tab. 1.1: Comparison table between V1495 and V249510
 Tab. 1.2: Table of models and related items.....11
 Tab. 6.1: V2495 specifications table21
 Tab. 6.2: A395A Mezzanine specifications table.....21
 Tab. 6.3: A395B Mezzanine specifications table.....22
 Tab. 6.4: A395C Mezzanine specifications table22
 Tab. 6.5: A395D Mezzanine specifications table22
 Tab. 6.6: A395E Mezzanine specifications table.....22
 Tab. 7.1: Delivered kit content23
 Tab. 12.1: V2495 register address map36
 Tab. 12.2: VME interface registers.....37
 Tab. 12.3: ROM Address Map of the V2495.....38
 Tab. 12.4: CSR registers39
 Tab. 13.1: Clock ports description table41
 Tab. 13.2: Mainboard Robinson-Nugent connector description table41
 Tab. 13.3: LEMO G ports description table.....41
 Tab. 13.4: Expansion I/O ports description table42
 Tab. 13.5: A395D mapping.....43
 Tab. 13.6: LED ports description table43
 Tab. 13.7: Gate and Delay Generator ports description table.....43
 Tab. 13.8: Local Bus ports description table.....44
 Tab. 13.9: Main parameters of the Gate and Delay Generator.....47
 Tab. 13.10: Local Bus registers description for the Gate and Delay Generator configuration48

Safety Notices

N.B. Read carefully the “Precautions for Handling, Storage and Installation” document provided with the product before starting any operation.

The following HAZARD SYMBOLS may be reported on the unit:

	Caution, refer to the product manual
	Caution, risk of electrical shock
	Protective conductor terminal
	Earth (Ground) Terminal
	Alternating Current
	Three-Phase Alternating Current

The following symbol may be reported in the present manual:



General warning statement

The symbol could be followed by the following terms:

- **DANGER:** Indicates a hazardous situation that, if not avoided, will result in serious injury or death.
- **WARNING:** Indicates a hazardous situation that, if not avoided, could result in death or serious injury.
- **CAUTION:** Indicates a situation or condition that, if not avoided, could cause physical injury, or damage the product and/or its environment.

CAUTION: Avoid potential hazards.



USE THE PRODUCT ONLY AS SPECIFIED.

ONLY QUALIFIED PERSONNEL SHOULD PERFORM SERVICE PROCEDURES

CAUTION: Avoid Electric Overload.



TO AVOID ELECTRIC SHOCK OR FIRE HAZARD, DO NOT POWER A LOAD OUTSIDE OF ITS SPECIFIED RANGE

CAUTION: Avoid Electric Shock.



TO AVOID INJURY OR LOSS OF LIFE, DO NOT CONNECT OR DISCONNECT CABLES WHILE THEY ARE CONNECTED TO A VOLTAGE SOURCE

CAUTION: Do Not Operate in Wet/Damp Conditions.



TO AVOID ELECTRIC SHOCK, DO NOT OPERATE THIS PRODUCT IN WET OR DAMP CONDITIONS

CAUTION: Do Not Operate in an Explosive Atmosphere.



TO AVOID INJURY OR FIRE HAZARD, DO NOT OPERATE THIS PRODUCT IN AN EXPLOSIVE ATMOSPHERE



THIS DEVICE SHOULD BE INSTALLED AND USED BY A SKILLED TECHNICIAN ONLY OR UNDER HIS SUPERVISION



DO NOT OPERATE WITH SUSPECTED FAILURES. IF YOU SUSPECT THIS PRODUCT TO BE DAMAGED, PLEASE CONTACT THE TECHNICAL SUPPORT

CAUTION: this product needs proper cooling.



USING V2495 WITH MEZZANINES REQUIRES CRATE WITH FORCED COOLING AIR FLOW SINCE OVERHEATING MAY DAMAGE THE MODULE (refer to Chap. 6)



THE V2495 CANNOT BE OPERATED WITH VME8001 CAEN CRATES

CAUTION: this product needs proper handling.



V2495 DOES NOT SUPPORT LIVE INSERTION (HOT SWAP)!
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF!



ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

1 Introduction

The V2495 is a general-purpose programmable FPGA and I/O unit housed in a 1-unit wide VME 6U module. The board is a suitable solution for the implementation of digital functions such as Coincidence, Trigger Logic, Gate and Delay Generator, Input/Output Register and more.

The programmable architecture is based on the User FPGA (hereafter UFPGA). The UFPGA is directly interfaced to the front panel I/Os and to an onboard Gate and Delay Generator, that allows to delay and gate up to 32 signals. A second FPGA, the Main FPGA (hereafter MFPGA), is responsible for USB and VME interface management. The MFPGA communicates with the UFPGA through an internal local bus.

The presence of three expansion slots interfaced to the UFPGA allows to extend the channel interface of the V2495 by adding up to three independent mezzanine boards. Five mezzanine board types are available: A395A, A395B, A395C, A395D, A395E (see **Tab. 1.2**). The V2495 can reach a maximum of 194 I/O channels.

The board can be controlled and programmed through either the VME or the USB interface. The custom firmware can be developed either with VHDL tools or the new SCI-Compiler application (Chap. 13). The firmware is then loaded on the User FPGA by a dedicated JTAG connector, allowing for in-system JTAG configuration and debugging (e.g. using Altera SignalTap).

The V2495 is also available in desktop form factor, called DT5495.

The V2495 can be considered as an evolution of CAEN V1495 board with which it bears several analogies (e.g. the front panel connectors have the same function and nomenclature with respect to the V1495). In addition, it provides enhanced logic resources, features and interfaces.

The following **Tab. 1.1** is a comparison table between the two modules.



	V1495	V2495
User FPGA	Altera Cyclone EPI1C20, 20k LEs	Altera Cyclone V GX, 50k LEs
Front Panel I/O	Sections A and B (2 x 68-pin Robinson Nugent connector; 32 input channel each) Section C (1 x 68-pin Robinson Nugent connector; 32 output channels) Section G (2 X LEMO connector; input/output channels)	
On-board Delay Generator	4 Delay lines	32 Gate and Delay lines
Local Bus	16-bit 50 MHz parallel interface	
VME Bus	Addressing spaces: A24, A32 Data transfer modes: D16, D32, BLT32	
USB Interface	Not Supported	USB2.0
Mezzanine Boards	A395A, A395B, A395C, A395D, A395E	

Tab. 1.1: Comparison table between V1495 and V2495

Tab. 1.2 lists the board models, the firmware and hardware related products as well as the ordering option information.

Board Models		Description
V2495	VME64 Programmable Logic Unit	
2495KITPRO	V2495 + SW555PRO - Programmable Logic Unit & Sci-Compiler PRO Bundle Kit	
User Firmware		Description
FW2495SC(*)	Channel Latching Scaler for V2495 and DT5495	
Related Products		Description
A3818A	A3818A – PCIe 1 Optical Link	
A3818B	A3818B – PCIe 2 Optical Link	
A3818C	A3818C – PCIe 4 Optical Link	
A5818	A5818 – PCIe 4 Optical Link (Gen 3)	
V3718	V3718 – VME64-USB Bridge	
VX3718	VX3718 – VME64X-USB Bridge	
V4718	V4718 - VME64-USB 3.0, Ethernet and Optical Link Bridge	
VX4718	VX4718 - VME64X-USB 3.0, Ethernet and Optical Link Bridge	
Accessories		Description
A395A	Mezzanine: 32 LVDS/ECL/PECL input channels	
A395B	Mezzanine: 32 LVDS output channels	
A395C	Mezzanine: 32 ECL output channels	
A395D	Mezzanine: 8 NIM/TTL input/output channels	
A395E	Mezzanine: 8 Channel 16Bit $\pm 5V$ DAC	
A967	Cable assembly: 32 Channel Cable Adapter (1x32 to 2x16)	

Tab. 1.2: Table of models and related items

(*) Pay firmware. Unlocking license needed. Please, refer to the FW2495SC web page for details.

2 Block Diagram

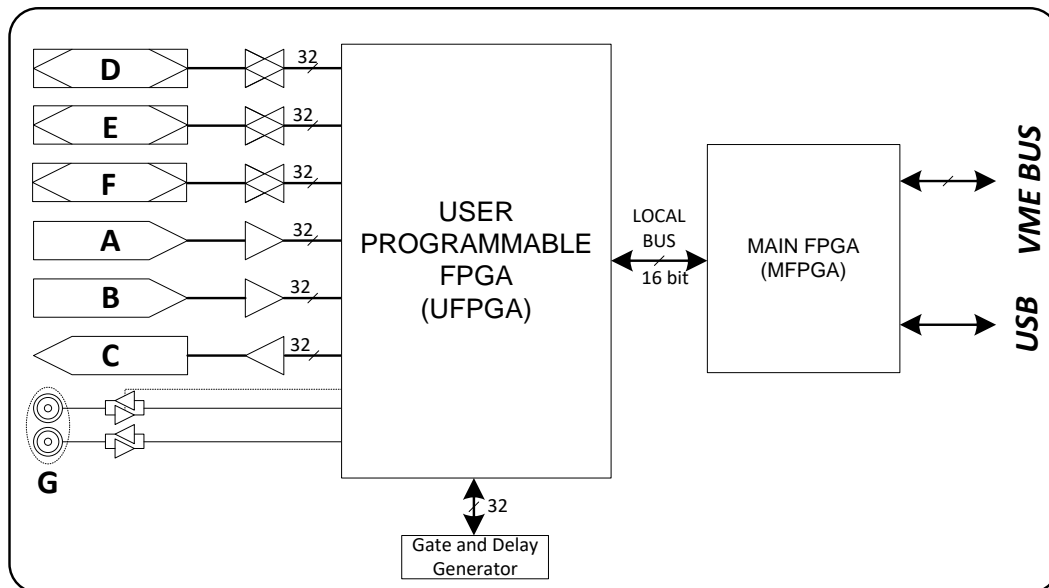


Fig. 2.1: Block diagram

3 Main Components and Interconnections

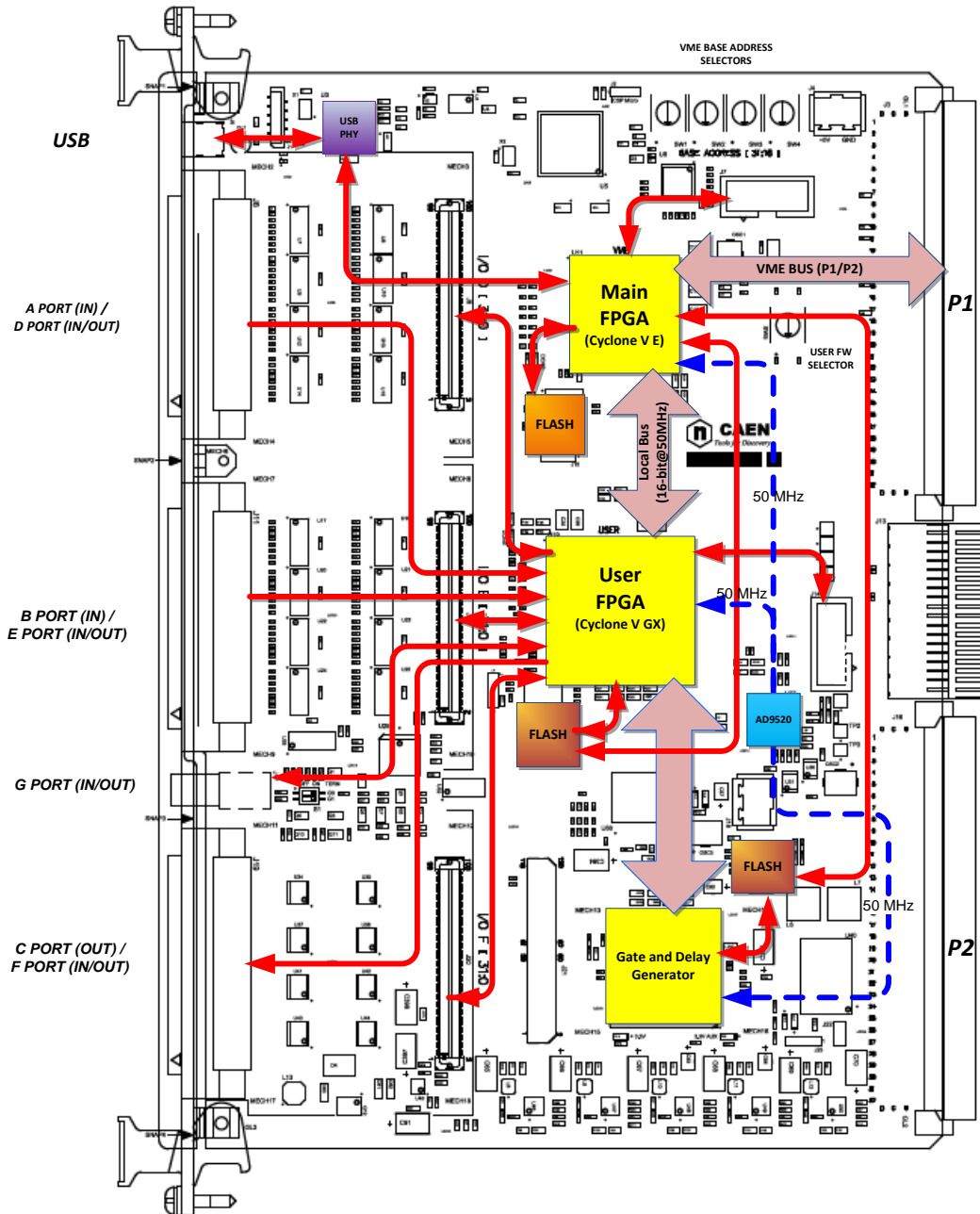


Fig. 3.1: Main components and interconnections

3.1 USB Interface

The V2495 is equipped with a USB2.0 interface. The USB physical layer is managed by a high-speed (480 Mb/s) transceiver controlled by the Main FPGA.

3.2 VME Interface

The P1 and P2 are the standard VME connectors both interfaced with the Main FPGA.

3.3 Main FPGA

The MFPGA (Altera Cyclone V E) manages the VME and USB interfaces and the connection with the UFPGA through a proprietary 16-bit@50 MHz local bus. The MFPGA has a dedicated external flash memory for configuration purposes. It also pilots the flash memories dedicated to loading the firmware on the UFPGA and on the GDG.

3.4 User FPGA

The User FPGA (Altera Cyclone V GX) manages the I/O peripherals (A/D, B/E, G, C/F ports) and communicates with the GDG. A dedicated external flash memory can store a set of firmware images to be loaded on the User FPGA. A dedicated JTAG connector allows to program the UFPGA “on-the-fly” for fast firmware prototyping and debugging.

3.5 Gate and Delay Generator

The V2495 hosts a Gate and Delay Generator (see Fig. 3.2) able to provide up to 32 gated and delayed signals (“delayed signals”) triggered by 32 inputs (“start signals”). The gate width and delay value are user programmable. The GDG is an external component implemented in a Xilinx Spartan-6 FPGA. It is connected through a serial bus (SPI) to the User FPGA for gate and delay register programming (refer to Sec. 3.5 for detailed information). The GDG configuration is stored in a dedicated flash memory. The GDG firmware cannot be modified by the user.

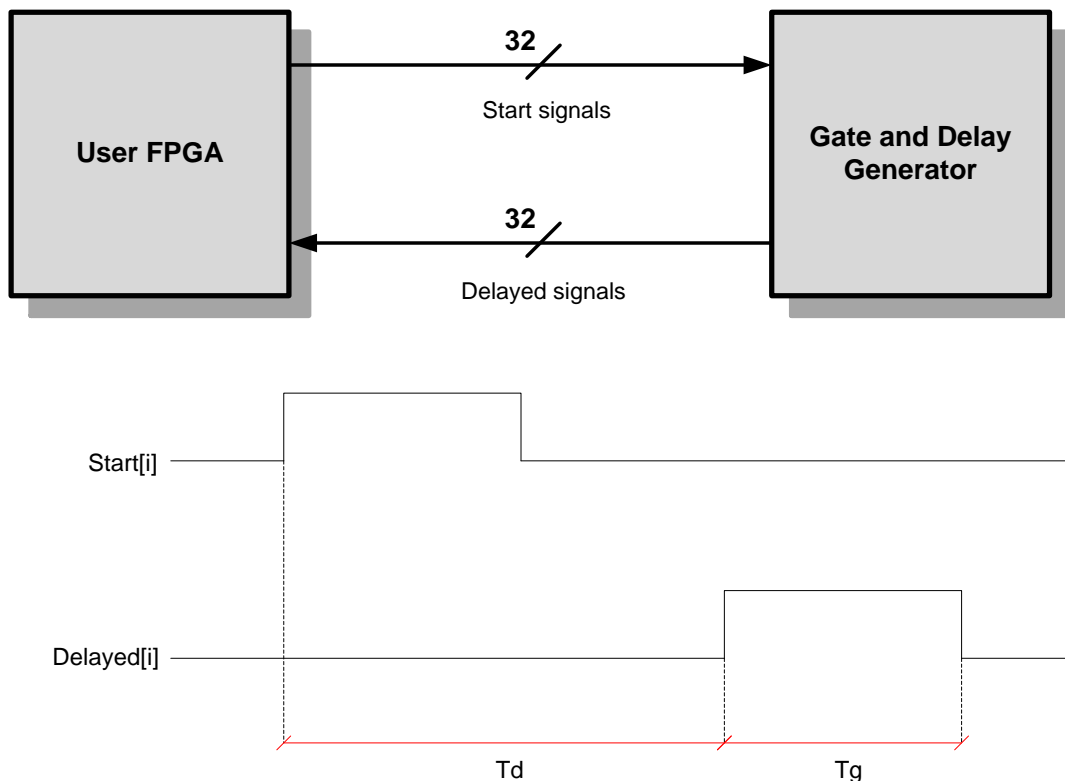


Fig. 3.2: The UFPGA and GDG interface.

3.6 Clock Distribution

Each FPGA receives the same 50-MHz system clock generated by a common on-board oscillator.

4 Front Panel Connectors, LEDs and Labels

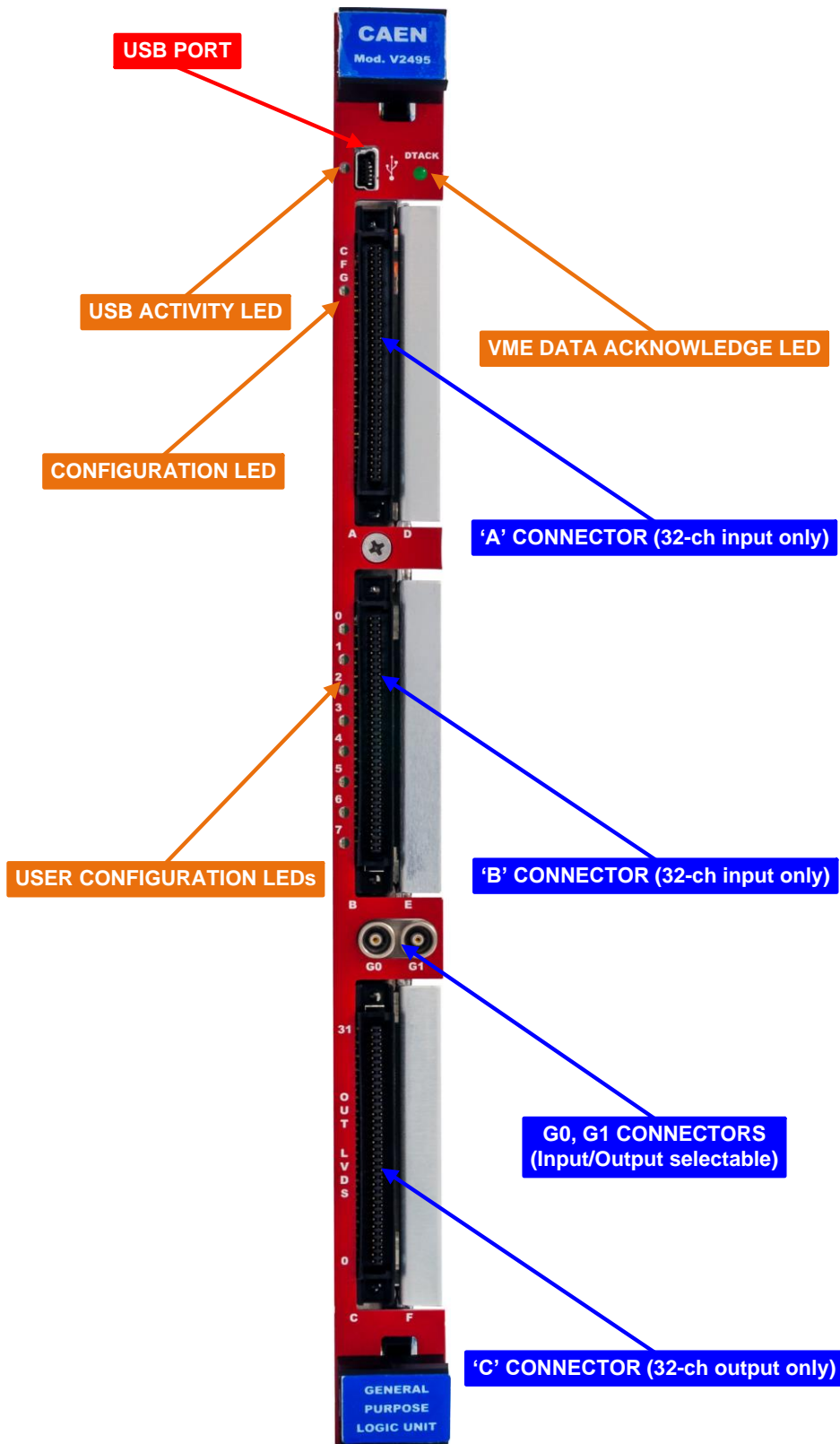




Fig. 4.1: Front panels view

USB PORT


	<p>FUNCTION</p> <p>MiniUSB connector to communicate with the V2495 by USB link for board configuration and firmware upgrade.</p> <p>ELECTRICAL SPECS</p> <p>N.A.</p>	<p>MECHANICAL SPECS</p> <p>Series: miniUSB connectors. Type: SD-54819-026 (B-type). Manufacturer: Molex Inc.</p> <p>CABLES</p> <p>A 1-m USB standard cable is included with the V2495 (USB A-type to miniUSB B-type).</p>
---	--	---

USB LED (GREEN): driven by the Main PFGA, this LED lights up if a USB read/write access to the board is performed.


DTACK LED

	<p>FUNCTION</p> <p>This LED lights up whenever a VME read/write access to the board is performed.</p>	<p>COLOR</p> <p>Green.</p>
---	--	-----------------------------------

A, B, C CONNECTORS

	<p>FUNCTION</p> <p>Motherboard I/O 34+34 pin connectors:</p> <ul style="list-style-type: none"> - A/B are inputs - C is an output <p>ELECTRICAL SPECS</p> <p>See Tab. 6.1.</p>	<p>MECHANICAL SPECS</p> <p>Series: 80-0009-0666-1. Type: P50E-068-P1-SR1-TG. Manufacturer: 3M.</p>
---	---	---

CFG LED

	<p>FUNCTION</p> <p>This LED is constantly on when all the on-board FPGAs are configured by the application firmware on their relevant flash memory (it is the OR of the internal configuration LEDs described in Chap. 5). The LED blinks if the MFPGA is in Factory mode.</p>	<p>COLOR</p> <p>Green.</p>
---	---	-----------------------------------

G0, G1 CONNECTORS

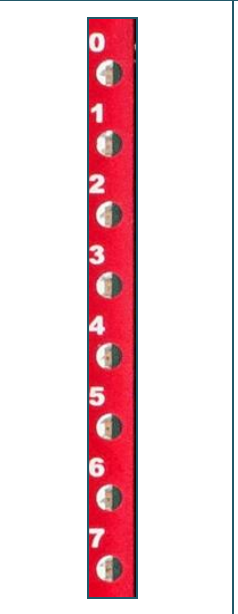


FUNCTION
 Bidirectional single-ended connectors. Terminations can be activated/deactivated by dedicated on-board switches (see Chap. 5).

ELECTRICAL SPECS
 See **Tab. 6.1**.

MECHANICAL SPECS
 Series: 00 LEMO Connectors.
 Type: EPY.00.250.NTN.
 Manufacturer: LEMO

0, 1, 2, ..., 7 LEDs



FUNCTION
 The status of these LEDs is user-programmable
 NOTE: when the UFGA is in Factory mode, odd and even LEDs alternatively blink.

COLOR
 Green.

LABELS



Two blue labels on each insertion/extraction handle of the VME front panel report:

- Manufacturer name and board’s model
- Brief functional description

5 Internal Connectors and LEDs

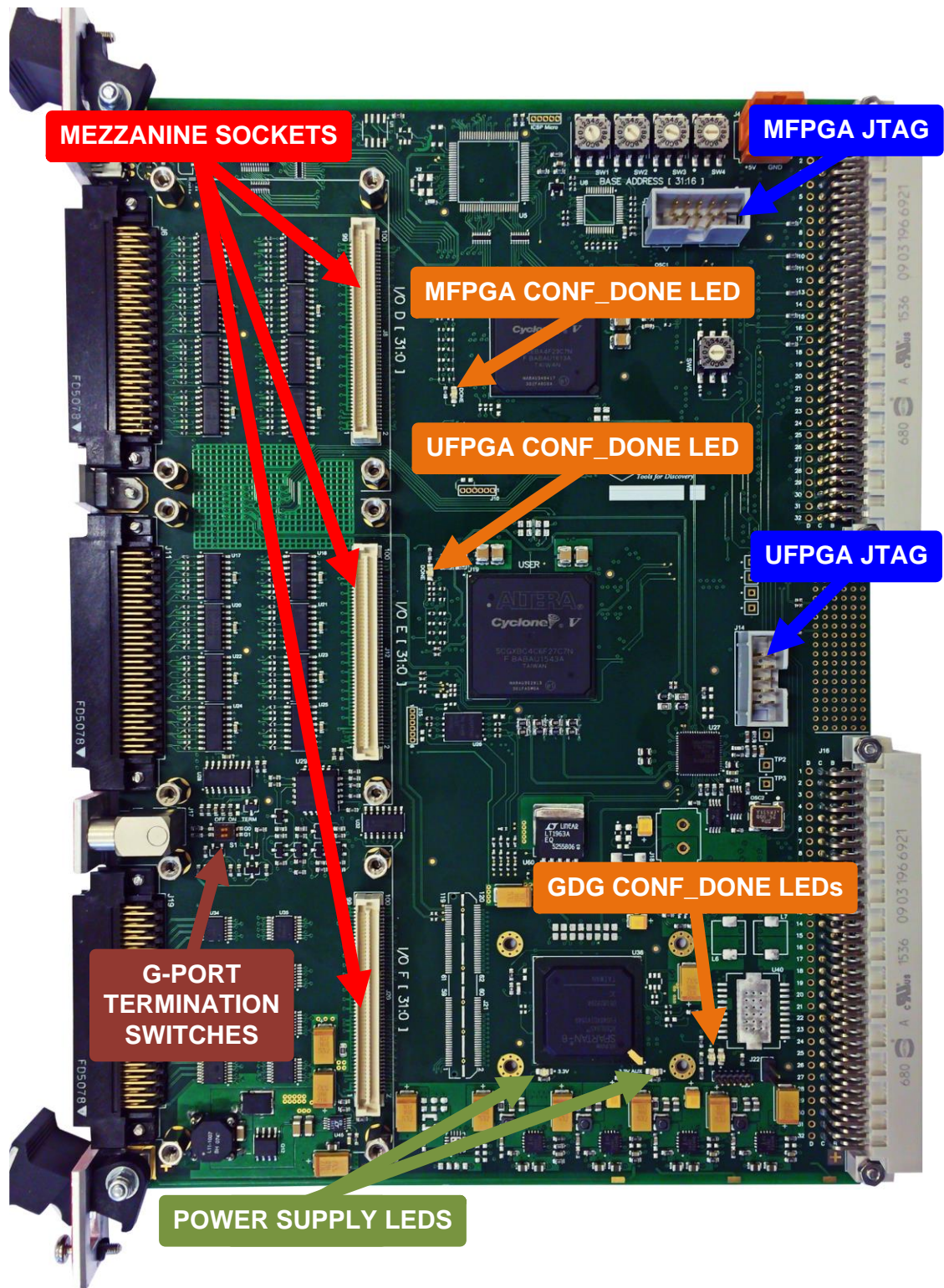
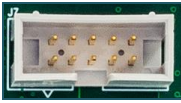


Fig. 5.1: On-board internal connectors and LEDs

MAIN FPGA JTAG



FUNCTION

MFPGA-dedicated JTAG connector.

ELECTRICAL SPECS

N. A.

MECHANICAL SPECS

Series: 7610-6002 Board Connector.

Type: 7610-6002-5+5-DR.

Manufacturer: 3M.

USER FPGA JTAG



FUNCTION

UFPGA-dedicated JTAG connector.

ELECTRICAL SPECS

N. A.

MECHANICAL SPECS

Series: 7610-6002 Board Connector.

Type: 7610-6002-5+5-DR.

Manufacturer: 3M.

MEZZANINE SOCKET



FUNCTION

Mezzanine board expansion connector (x3)

ELECTRICAL SPECS

N. A.

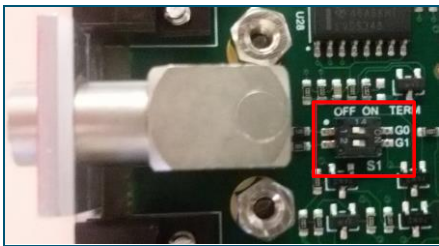
MECHANICAL SPECS

Series: Stacking Board Connectors.

Type: 61083-104400LF

Manufacturer: AMPHENOL FCI.

G-PORTS TERMINATION SWITCHES

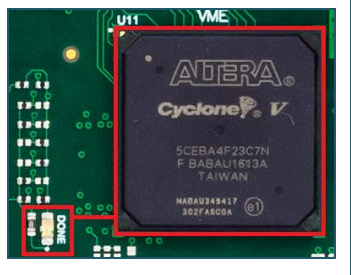


FUNCTION

Two switches, one for each G connector, enable or disable the 50-Ω termination according to the input or output direction and the NIM or TTL configuration of the relevant connector.

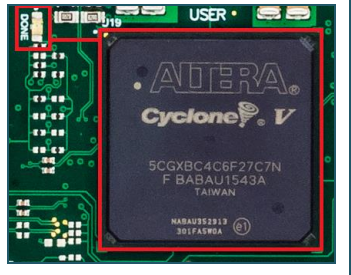
- Position “ON” = 50 Ω termination enabled
- Position “OFF” = termination disabled

MFPGA CONF_DONE LED



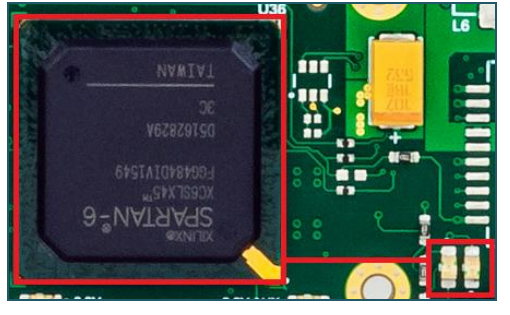
FUNCTION	COLOR
This led lights up when the Main FPGA is properly programmed.	Green.

UFPGA CONF_DONE LED



FUNCTION	COLOR
This LED lights up when the User FPGA is properly programmed.	Green.

GDG CONF_DONE LEDs



FUNCTION	COLOR
Two LEDs indicate the status of the Gate and Delay Generator:	SX LED: Orange.
<ul style="list-style-type: none"> • DX LED on (green): FPGA programmed. • SX LED on (orange): FPGA not programmed. 	DX LED: Green.

POWER SUPPLY LEDs



FUNCTION	COLOR
Two LEDs, placed under the Gate and Delay Generator, light up if the 3.3V power supply for the digital circuitry is provided.	Green.

6 Technical Specifications

V2495 Motherboard					
FORM FACTOR	1-unit wide, 6U high VME64				
	I/O SECTIONS A and B	Nr. of Channels 32	Logic Direct	Bandwidth 200 MHz	
Direction Input		Signal Differential LVDS/ECL/PECL (single ended TTL optional) Z_{diff} : 100 Ω Extended Common Mode Input range: -4V to +5V Fail Safe input feature		Front Panel Connector Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins	
I/O SECTION C	Nr. of Channels 32 channels	Logic Direct	Bandwidth 250 MHz		
	Direction Output	Signal Differential LVDS Require 100 Ω termination		Front Panel Connector Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins	
I/O SECTION G	Nr. of Channels 2	Logic TTL IN = Direct TTL OUT = Direct NIM IN = Invert NIM OUT = Direct	Bandwidth 250 MHz		
	Direction I/O selectable	Signal Single ended NIM/TTL selectable Open/50 Ω termination selectable		Front Panel Connector LEMO 00	
GATE and DELAY GENERATOR	Minimum Delay/Gate	Min. 9.6 ns	Typ. 10.7 ns	Max. 11.8 ns	
	Maximum Delay/Gate	631 μ s	701.2 μ s	771.5 μ s	
	Maximum channel-to-channel spread: 20%				
COMMUNICATION INTERFACE	VME VME64X compliant Addressing space: A24, A32 Data Transfer mode: D16, D32, BLT32 Multicast commands			USB USB 2.0 compliant	
POWER REQUIREMENTS	1.0A (max.) @ +5V +12V and -12V rails are not used				

Tab. 6.1: V2495 specifications table

A395A Mezzanine Board				
I/O SECTION	Nr. Of Channels 32	Logic Direct	Bandwidth 200 MHz	
	Direction Input	Signal Differential LVDS/ECL/PECL (single ended TTL optional) Z_{diff} : 100 Ω Extended Common Mode input range: -4V to +5V Fail Safe input feature		Front Panel Connector Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins
POWER CONSUMPTIONS	0.1 A (max) @ +5V +12V and -12V rails are not used			

Tab. 6.2: A395A Mezzanine specifications table

A395B Mezzanine Board			
I/O SECTION	Nr. of Channels 32	Logic Direct	Bandwidth 250 MHz
	Direction Output	Signal Differential LVDS Requires 100 Ω termination	Front Panel Connector Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins
POWER CONSUMPTIONS	0.1 A (max) @ +5V +12V and -12V rails are not used		

Tab. 6.3: A395B Mezzanine specifications table

A395C Mezzanine Board			
I/O SECTION	Nr. of Channels 32	Logic Direct	Bandwidth 300 MHz
	Direction Output	Signal Differential ECL	Front Panel Connector Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins
POWER CONSUMPTIONS	1.4 A (max) @ +5V +12V and -12V rails are not used		

Tab. 6.4: A395C Mezzanine specifications table

A395D Mezzanine Board			
I/O SECTION	Nr. of Channels 8	Logic Direct	Bandwidth 250 MHz
	Direction I/O selectable	Signal selectable TTL/NIM: TTL IN = Direct TTL OUT = Direct NIM IN = Invert NIM OUT = Direct	Front Panel Connector LEMO 00
	Impedance Selectable 50 Ω /high-Z by on-board jumper		
POWER CONSUMPTIONS	1.1 A (max) @ +5V +12V and -12V rails are not used		

Tab. 6.5: A395D Mezzanine specifications table

A395E Mezzanine Board			
I/O SECTION	Nr. of Channels 8	Logic Analog	Bandwidth n.a.
	Direction Output	Signal 16-bit resolution $\pm 5V$ @10k Ω RL $\pm 4V$ @200 Ω RL	Front Panel Connector LEMO 00
POWER CONSUMPTIONS	0.3 A (max) @ +5V +12V and -12V rails are not used		

Tab. 6.6: A395E Mezzanine specifications table





OPERATING THE V2495 WITH MORE THAN ONE A395C OR A395D MEZZANINE BOARDS REQUIRES USING VME CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING DUE TO INSUFFICIENT VENTILATION MAY DAMAGE THE MODULE.

7 Packaging and Compliancy

The V2495 board is available in 1-unit wide VME 6U x 160mm form factor.

The device is inspected by CAEN before shipment and it is guaranteed to leave the factory free of mechanical or electrical defects.

The content of the delivered package standardly consists of the part list shown in the table below (Tab. 7.1).

	Part	Description	Qt
	V2495 (with or without mezzanine board extension ⁽¹⁾)	Programmable Logic Unit	x1
	USB cable	USB-2.0 cable, type A to mini-USB, L=1mt	x1
	Documentation	UM5175 - V2495 PLU User Manual	-

Tab. 7.1: Delivered kit content

⁽¹⁾ Mezzanine boards are available by ordering option (refer to Tab. 1.2).

CAUTION: to manage the product, consult the operating instructions provided.

When receiving the unit, the user is strictly recommended to:

- Inspect containers for damage during shipment. Report any damage to the freight carrier for possible insurance claims.
- Check that all the components received match those listed on the enclosed packing list as in Tab. 7.1. (CAEN cannot accept responsibility for missing items unless we are notified promptly of any discrepancies.)
- Open shipping containers; be careful not to damage contents.
- Inspect contents and report any damage. The inspection should confirm that there is no exterior damage to the unit such as broken knobs or connectors and that the front panel and display face are not scratched or cracked. Keep all packing material until the inspection has been completed.
- If damage is detected, file a claim with the carrier immediately and notify CAEN service.
- If equipment must be returned for any reason, carefully repack equipment in the original shipping container with original packing materials if possible. Please, contact CAEN service.
- If equipment is to be installed later, place equipment in the original shipping container and store it in a safe place until ready to install.



DO NOT SUBJECT THE ITEM TO UNDUE SHOCK OF VIBRATIONS



DO NOT BUMP, DROP OR SLIDE SHIPPING CONTAINERS



DO NOT LEAVE ITEMS OR SHIPPING CONTAINERS UNSUPERVISED IN AREAS WHERE PERSONNEL UNTRAINED MAY MISHANDLE THE ITEMS



USE ONLY ACCESSORIES WHICH MEET THE MANUFACTURER'S SPECIFICATIONS

8 PID (Product Identifier)

PID is the CAEN product identifier, an incremental number greater than 10000 that is unique for each product. The PID is on a label affixed to the product (Fig. 8.1), it is even stored in an on-board non-volatile memory (Sec. 12.3.9), and readable by CAEN toolbox software (Sec. 11.2.1).

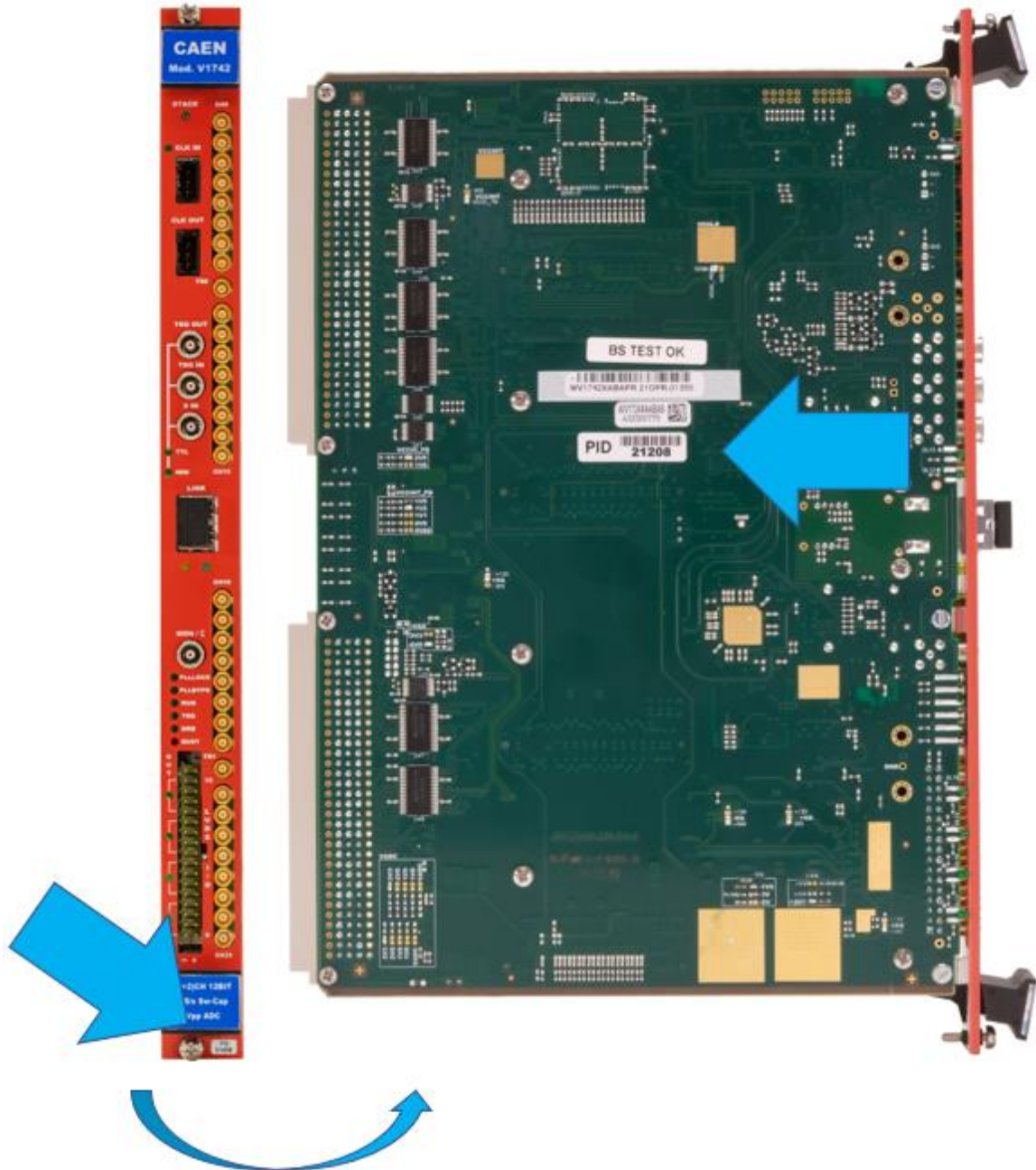


Fig. 8.1: PID location on the device (the number and board model in the pictures are purely indicative)

9 Getting Started with V2495

9.1 Expansion Mezzanines

Four different type of mezzanine boards are available by ordering option to extend the V2495 functions (**Tab. 1.2**).

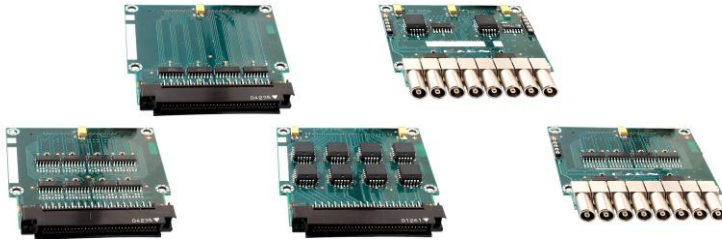


Fig. 9.1: Mezzanine boards for the V2495

9.2 Mezzanine Boards Installation

In order to install an A395x-series mezzanine board on the V2495 motherboard, please use a Phillips screwdriver.

- Remove (unscrew) the metal cover of one of the available mezzanine slots.
- Plug the mezzanine board into the 100-pin expansion connector on the motherboard (see Chap. 5)
- Fix the mezzanine board with the screws

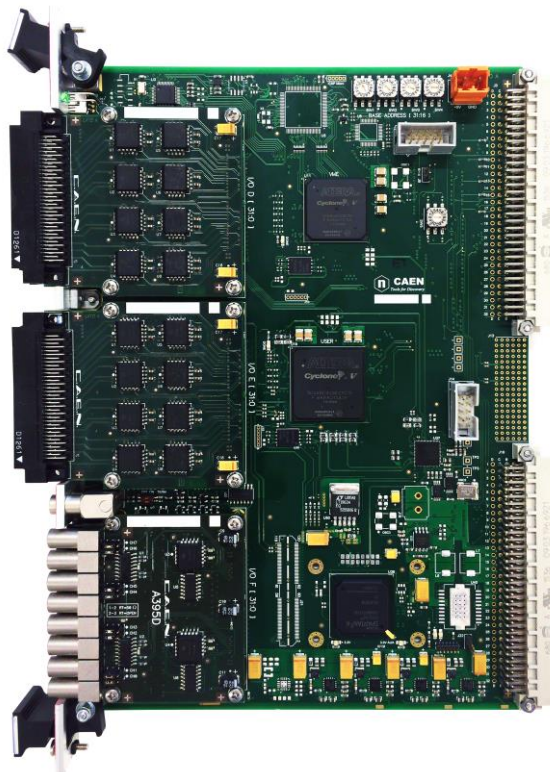


Fig. 9.2: V2495 motherboard hosting the mezzanine boards



OPERATING THE V2495 WITH MORE THAN ONE A395C OR A395D MEZZANINE BOARDS REQUIRES USING VME CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEATING DUE TO INSUFFICIENT VENTILATION MAY DAMAGE THE MODULE.

9.3 Front Panel Connector Cabling

Motherboard I/O sections A, B, C and A395A, A395B and A395C mezzanine boards feature the Robinson Nugent P50E-068-P1-SR1-TG multi-pin connector (see Chap. 4), whose pin layout is shown in Fig. 9.3.

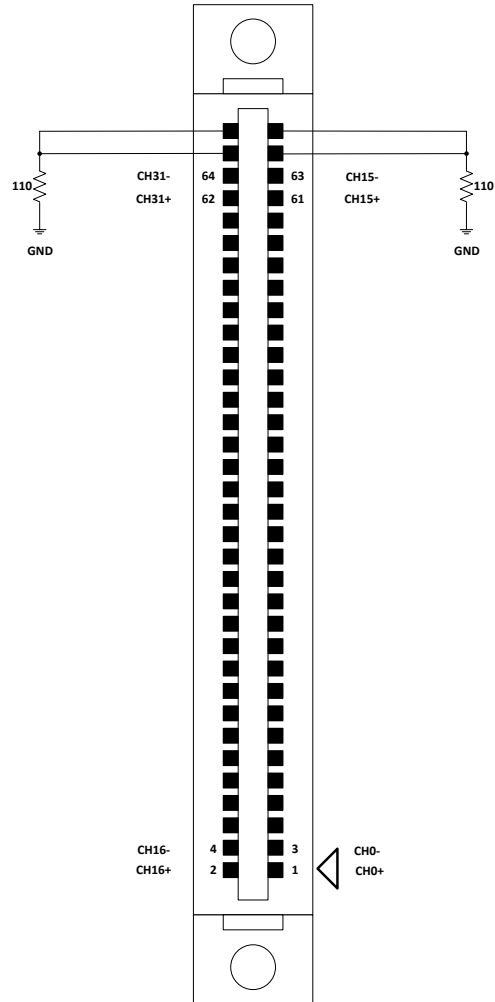


Fig. 9.3: Multi-pin connector pin assignment

The CAEN A967 Cable Adapter (Fig. 9.4) allows to adapt each Robinson Nugent multi-pin connector into two 1" 17+17-pin Header-type male connectors (3M, 4634-7301) with locks through two 25 cm long flat cables. Refer to the cable datasheet [RD3] for specifications and to Tab. 1.2 for the ordering option.



Fig. 9.4: CAEN A967 Cable Adapter

9.4 Setting the VME Base Address

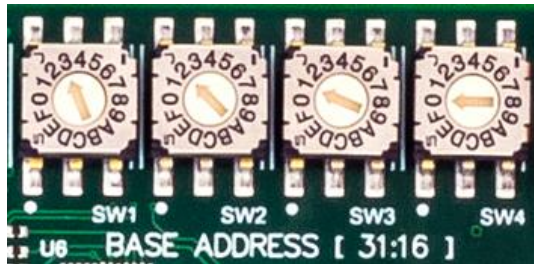


Fig. 9.5: Base Address on-board rotary switches

Four on-board rotary switches (SW1, SW2, SW3 and SW4 in Fig. 9.5), with 16 positions each, set the hexadecimal value of the VME Base Address (VBA) which univocally identifies the board over the VME bus. Such switches are placed on the component side of the motherboard (see Fig. 3.1).

- SW1 sets bits [31:28] of VBA;
- SW2 sets bits [27:24] of VBA;
- SW3 sets bits [23:20] of VBA;
- SW4 sets bits [19:16] of VBA.

9.5 Selecting the User FPGA Firmware

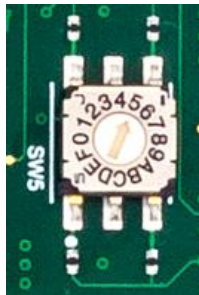


Fig. 9.6: User Firmware rotary switch

The on-board SW5 rotary switch selects which of the six firmware images will be loaded on the UFGPA at power-on. Five demos and one boot and recovery (factory) firmware are preloaded in the flash memory (see Chap. 14 for details).

Default SW5 position map:

Position 0 = Factory User Firmware; this copy is used as recovery boot and is not writable by the user.

Position 1 = Gate Pattern Demo (see Sec. 14.4)

Position 2 = Pattern Recorder Demo (see Sec. 14.5)

Position 3 = DAC (A395E) Demo (see Sec. 14.6)

Position 4 = Gate and Delay Demo (see Sec. 14.7)

Position 5 = available (empty)



Note: All the positions from 6 up to 15 are equivalent to position 0: factory firmware is loaded.

10 Power-on Configuration Sequence

When the board is powered on, the on-board programmable devices are configured with the firmware images stored in their dedicated flash memories. If all programmable devices (MFPGA, UFPGA and GDG) are correctly configured, the CFG LED is lit on. In case an anomaly occurs, the CFG LED status can be:

1) **BLINKING**: the FPGAs are configured, but the Main FPGA remained in Factory mode.

The MFPGA can be configured by two kind of firmware images which are stored on the dedicated flash memory: the Factory firmware and the Application firmware. The Factory firmware is a basic firmware specifically intended for boot and recovery functions. The Application firmware is the standard operating firmware and can be upgraded by the user through the VME or the USB interface.

At power-on, the MFPGA configures itself with the Factory firmware image and subsequently attempts to load the Application firmware. If the application firmware is missing or corrupted, the MFPGA will remain in the factory mode. The Factory firmware guarantees the communication with the board and allows the MFPGA Application firmware upgrade.

2) **OFF**: one or more FPGAs may not have been configured.

In this case, the user can take different actions according to the status of the internal configuration LEDs:

- If the MFPGA Configuration LED is off, an attempt to force the MFPGA in Factory mode can be performed (see next paragraph). If the CFG LED starts blinking, an application firmware upgrade can be attempted.
- If the UFPGA Configuration LED is off when the SW5 selector is set on one of the positions between 1 and 5, the switch should be set to position 0 and the board should be power cycled. Therefore, the UFPGA is configured in Factory mode and the CFG LED will start blinking. It is then possible to attempt a User Application firmware upgrade on the flash memory page which caused the issue.
- If the UFPGA Configuration LED is off and the SW5 selector is set to position 0 or the GDG Configuration LED lights up orange, please contact CAEN for further instructions.

Refer to Chap. 15 for CAEN Support contacts.

10.1.1 Boot Mode Selection

The on-board J9 jumper (see **Fig. 10.1**), when short-circuited, forces the Main FPGA to be reconfigured in Factory mode. This procedure allows to restore the board from anomalous conditions.

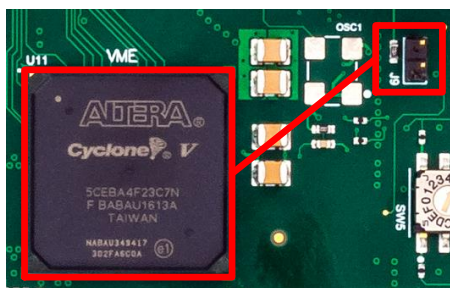


Fig. 10.1: Boot mode jumper for the Main FPGA

J9 -> Open (default): configures the Main FPGA by the Application firmware (if present or valid)

J9 -> Closed: forces the Main FPGA to configure itself with the Factory firmware (Factory mode).



Note: The jumper status is checked only at the board power-up.

11 Driver and Software Installation

11.1 Drivers

To communicate with the board using one of the available communication buses, specific drivers should be installed on your host device.



Note: to ensure the best system performance, it is recommended to have always the latest drivers release installed.

11.1.1 Direct USB Driver

In order to communicate with the V2495 through the front panel USB interface (see Chap. 4), the related driver is available for free download at the V2495 *Downloads* page on CAEN web site (**login required**).

The USB driver is provided for Windows and Linux OS.

➤ WINDOWS OS

A step-by-step driver installation procedure is given next.



Note: The procedure is based on a Windows 10 system. It may be slightly different for another Windows OS.

1. Download and unpack the driver installation package on the host PC.
2. Plug the USB cable on the V2495 and on the PC. Windows should detect the new hardware.
3. Go to the *Device Manager* area. The new hardware is listed in *Other devices* as “V2495” (see Fig. 2.1).

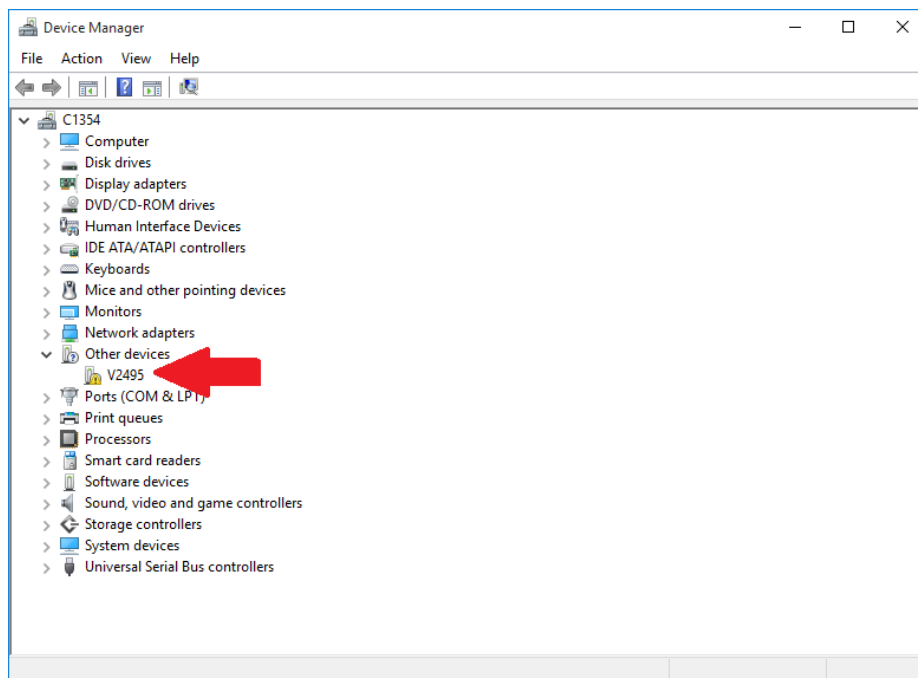


Fig. 11.1: V2495 hardware detection

4. Right click on “V2495” item and select *Update Driver Software* option in the slide menu.

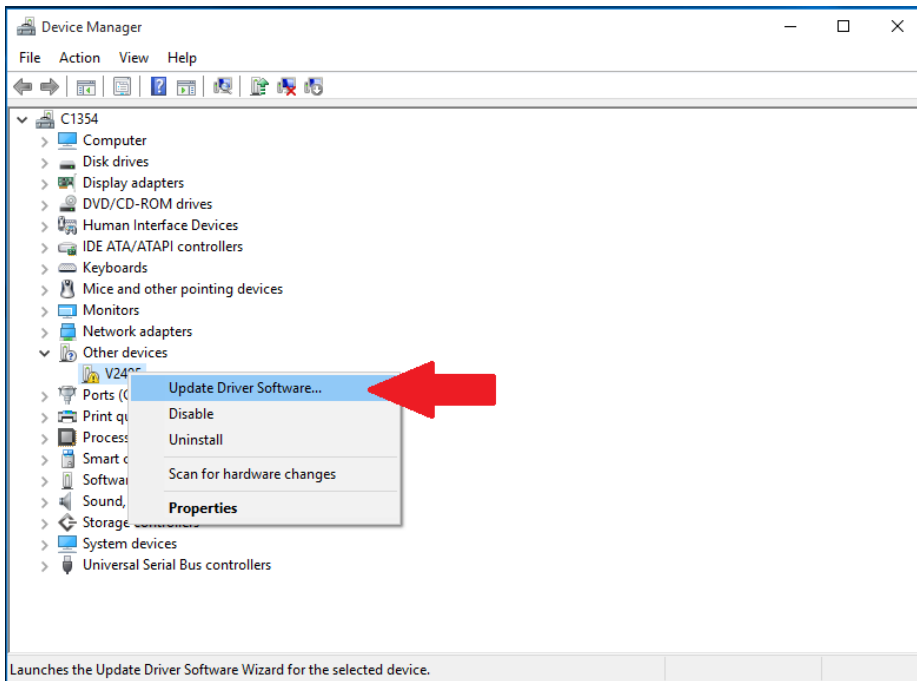


Fig. 11.2: USB driver manual installation: Step1

5. Select *Browse my computer for driver software* as in Fig. 11.3.

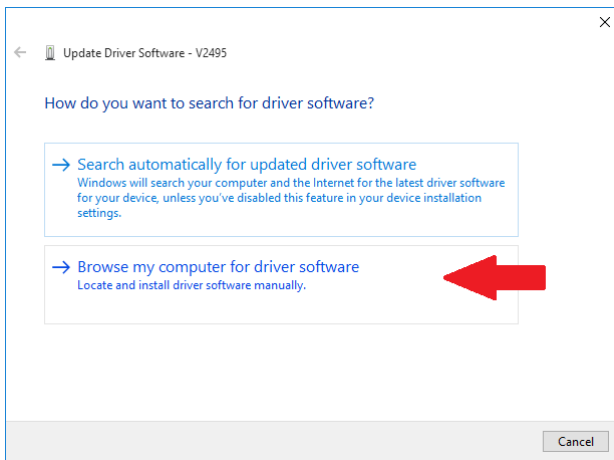


Fig. 11.3: USB driver manual installation: Step2

6. Use the [Browse] button to point to the driver folder in the destination path on the host PC.

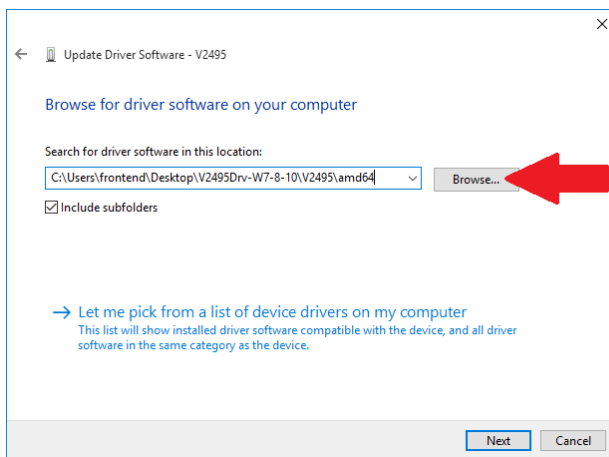


Fig. 11.4: USB driver manual installation: Step3

7. Click the [Close] button at the end of the installation process.

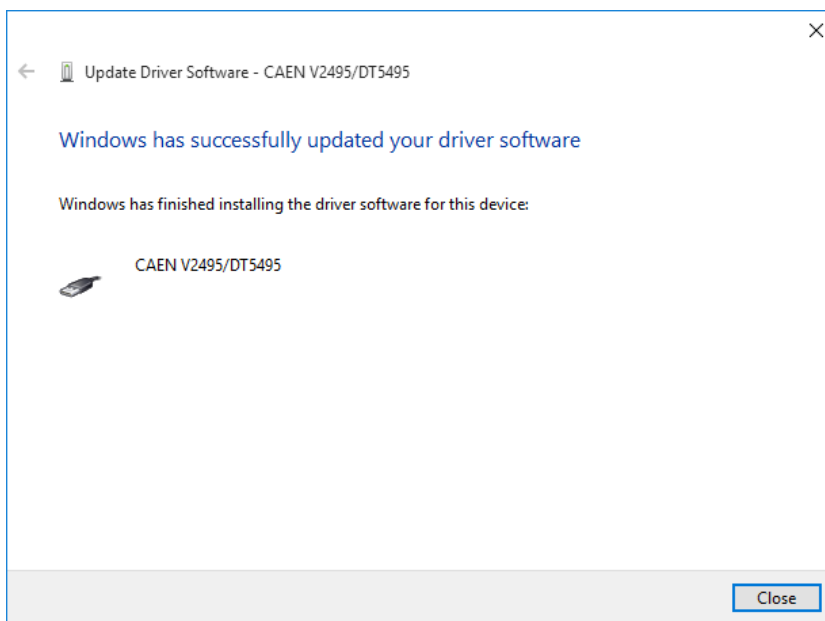


Fig. 11.5: USB driver manual installation: Step4

8. Check that the “CAEN V2495/DT5495” item appears in the *Universal Serial Bus controllers* list.

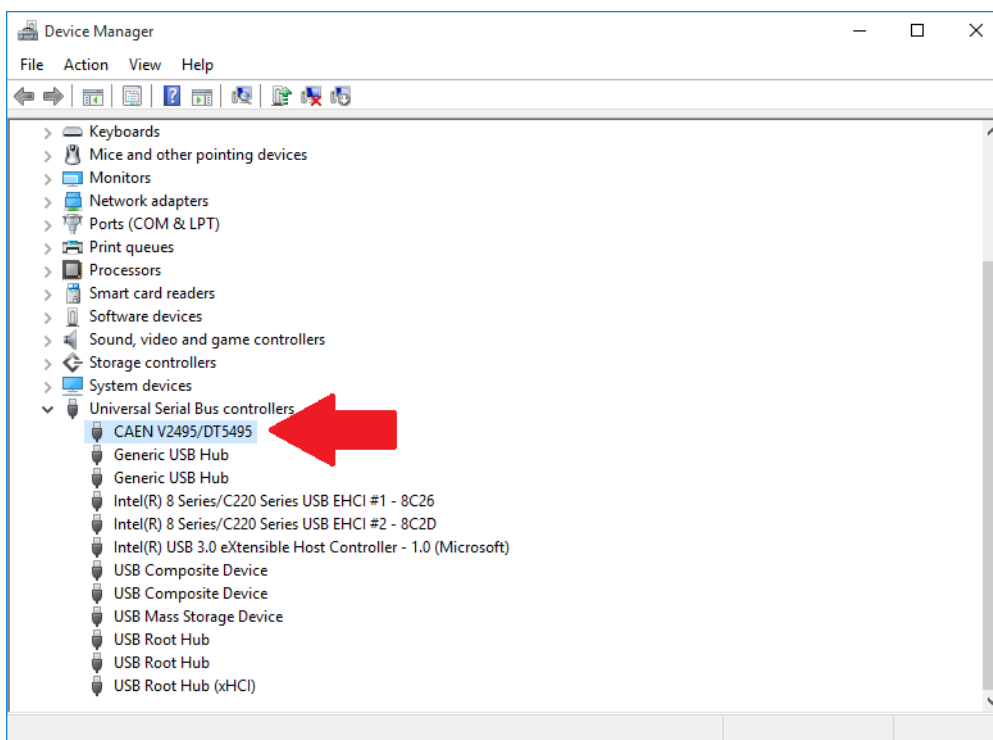


Fig. 11.6: USB driver manual installation: Step5

➤ **Linux OS**

V2495 is fully supported by Linux kernels from version 3.13 on.

11.1.2 VME Access

The V2495 can be accessed via the VME bus. CAEN provides USB-to-VME bridges (mod. V3718 and V4718), CONET-to-VME bridges (mod. V3718, V4718), Ethernet-to-VME bridge (mod. V4718).

➤ **V3718 USB-2.0 Driver**

The required driver is available for free download at the V3718 *Downloads* page on CAEN web site (**login required**) and manually installed. The installation procedure described for the direct USB driver can be taken as reference.

➤ **V4718 USB-3.0 Driver**

The required driver is available for free download at the V4718 *Downloads* page on CAEN web site (**login required**) and manually installed. The installation procedure described for the direct USB driver can be taken as reference.

➤ **CONET Driver**

The V3718 and V4718 optical link requires the installation of CAEN A5818 PCI Express Gen 3 Controller on your PC (alternatively, old A2818 PCI or A3818 PCIe cards). The related drivers should be installed, available for free download from the controller web page in the *Downloads* area (**login required**), and manually installed. Please refer to the controller User Manual for the driver installation instructions.

11.2 Software Tools

11.2.1 CAEN Toolbox

CAEN Toolbox is the comprehensive software suite designed for CAEN Front-End boards.

With V2495, CAEN Toolbox simplifies various tasks into a few easy steps, including:

- Upgrade the MFPGA firmware
- Load the User firmware on the UFPGA
- Verify the Main and User FPGA firmware
- Read the release number of the MFPGA firmware
- Store and get the Product Unlock Code in case of paid firmware
- Get the Board Info file (useful in case of support requests)

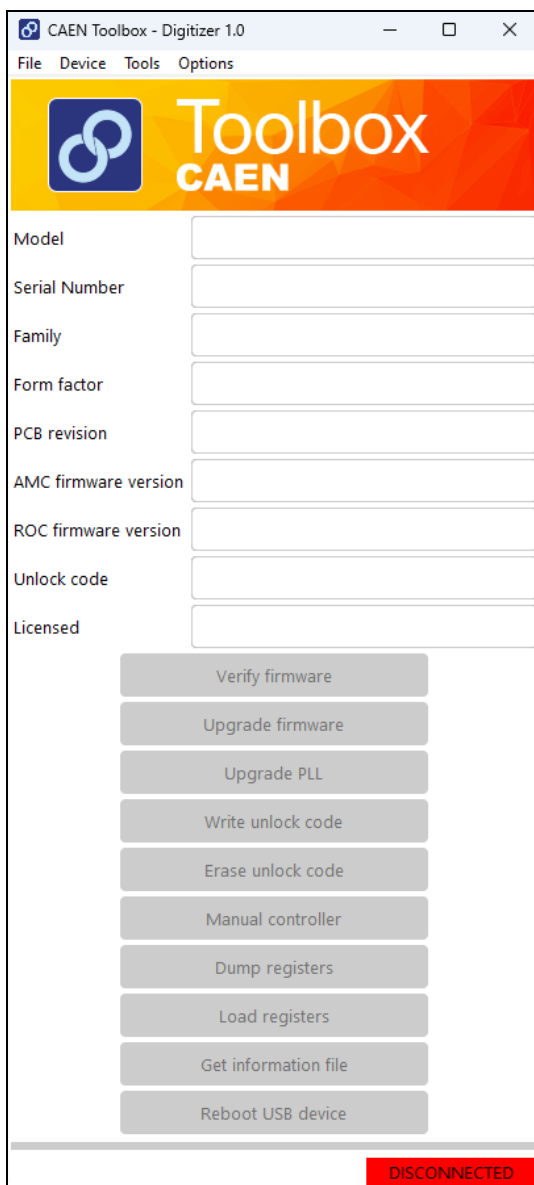


Fig. 11.7: CAEN Toolbox Graphical User Interface

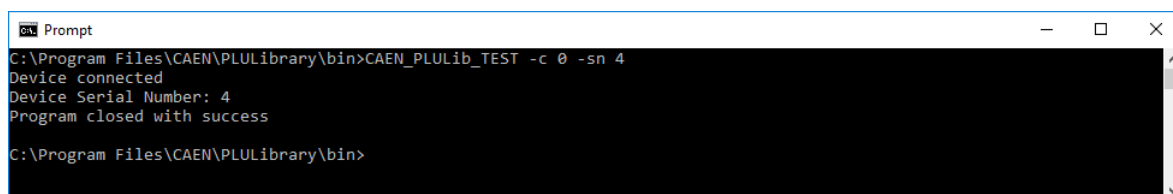
CAEN Toolbox runs on Windows® and Linux® platforms. The software is stand-alone on both the available versions.

Refer to the CAEN Toolbox documentation for installation instructions and a detailed description **[RD1]**.

11.2.2 PLULib Library

CAEN PLULib library is a library of C functions developed to control V2495 and DT5495 programmable logic units through direct USB and Ethernet communication interfaces, but also through the VMEbus connection by using CAEN Bridges.

The library includes a simple demo application, which is not intended for the board readout, but rather to automatically test the library functions. The user can then inspect the code as reference for his customized software development based on the PLU library.



```
CA Prompt
C:\Program Files\CAEN\PLULibrary\bin>CAEN_PLULib_TEST -c 0 -sn 4
Device connected
Device Serial Number: 4
Program closed with success
C:\Program Files\CAEN\PLULibrary\bin>
```

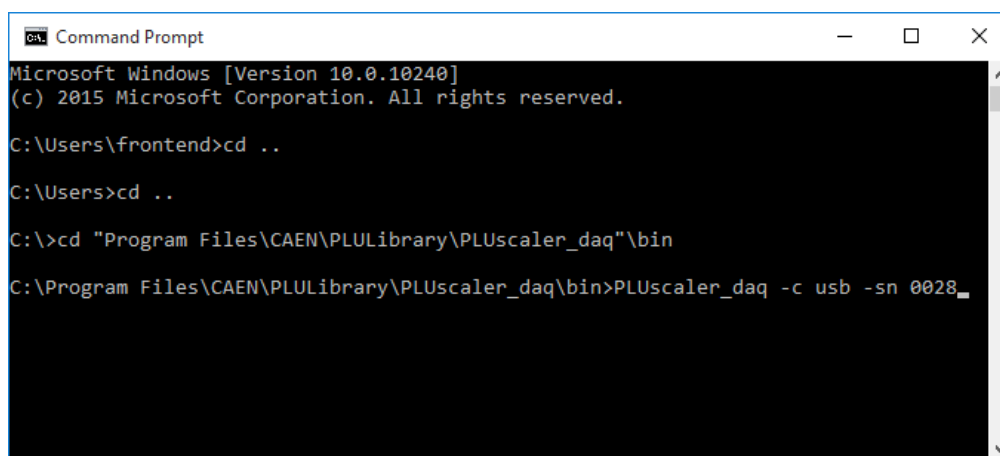
Fig. 11.8: CAEN PLULib Demo application prompt

CAEN PLULib library can operate on Windows® and Linux®, 32 and 64-bit. The documentation [RD4] and installation packages are available for free download at the PLULib *Downloads* page on CAEN web site (**login required**).

11.2.3 PLUscaler_daq

PLUscaler_daq is a CAEN software dedicated to managing data acquisition from DT5495 and V2495 Programmable Logic Unit with the FW2495SC firmware (see Chap. 15). It is a C-based simple application without a graphical user interface which relies on an external configuration text file.

The source code included in the package gives the user a useful starting point to develop customized software applications.



```
CA Command Prompt
Microsoft Windows [Version 10.0.10240]
(c) 2015 Microsoft Corporation. All rights reserved.

C:\Users\frontend>cd ..
C:\Users>cd ..
C:\>cd "Program Files\CAEN\PLULibrary\PLUscaler_daq"\bin
C:\Program Files\CAEN\PLULibrary\PLUscaler_daq\bin>PLUscaler_daq -c usb -sn 0028_
```

Fig. 11.9: PLUscaler_daq prompt

PLUscaler_daq can operate on Windows® and Linux®, 32 and 64-bit, and requires the PLULib library to be installed. The documentation [RD5] and installation packages are available for free download at the FW2495SC *Downloads* page on CAEN web site (**login required**).

12 Communication Interfaces

The V2495 board can be accessed via both VME bus and USB interface. All registers are accessible from both communication interfaces (VME/USB).

12.1 VME Bus

The V2495 boards can be individually addressed on the bus by means of their assigned base address.

The base address is set by means of on-board rotary switches (see Sec. 9.4) for all VME accesses except for geographical addressing.

Registers can all be accessed via VME bus in A24/A32 addressing mode and D32 mode.

VME interface supports interrupt generation requested by the User PFGA: User FPGA can generate an interrupt request by asserting its nINT signal (active low). The interrupt will be generated only if the appropriate registers have been configured (see Tab. 12.2).

USB and VME cycles cannot be performed at the same time. It is up to the user to guarantee that each bus cycle is mutually exclusive.

12.2 USB

USB interface grants access to the same address space and corresponding registers of the VME interface.

Register access over USB must be performed with Base Address equal to 0. The BA parameter in any of the following register tables is assumed to be zero for USB accesses.

12.3 Address Map

The following table illustrates the V2495 address map:

Address	Description
BA + 0x0000-0x0FFF	UFPGA data access
BA + 0x1000-0x7FFF	UFPGA register access
BA + 0x8000-0x80FF	VME Interface Registers
BA + 0x8100-0x81FF	Configuration ROM
BA + 0x8200-0x83FF	Configuration and Status Registers
BA + 0x8400-0x84FF	Reserved
BA + 0x8500-0x86FF	MFPGA flash configuration
BA + 0x8700-0x88FF	UFPGA flash configuration
BA + 0x8900-0x8AFF	GDG flash configuration
BA + 0x8B00-0x8BFF	Reserved
BA + 0x8C00-0x8FFF	Internal scratch RAM
BA + 0x9000-0xFFFF	reserved

Tab. 12.1: V2495 register address map

12.3.1 User FPGA Data Access (0x0000-0x0FFF)

The UFPGA data access space is allocated specifically for the readout of data produced in the UFPGA logic which need to exploit the maximum readout throughput available. This space can be accessed by using the available block transfer mechanism over the VME or USB communication interfaces.

Block data transfer allows to implement a faster readout. Block transfers requests over VME or USB do not trigger any transfer over the internal local bus between the MFPGA and UFPGA: a data prefetch mechanism, implemented in the MFPGA, stores User data into a local data queue (prefetch data queue). Please, refer to the prefetch mechanism description in Sec. 13.4. In consequence, data from the UFPGA data access space are read from the prefetch data queue in the MFPGA.

12.3.2 User FPGA Register Access (0x1000-0x7FFF)

UFPGA register address range is allocated for User register read/write.

A read or write transfer (single cycle) can be triggered on the local bus by performing a corresponding read transfer in the 0x1000-0x7FFF address interval.

The local bus master in the MFPGA acts as a transparent bridge between the communication interface (VME/USB) and the local bus in this interval. A couple of examples are given to illustrate the transparent bridge behaviour.

- VME register access

Assume the board has a base address set to 0x32100000. An access to a user register mapped at offset 0x1000 on the local bus can be triggered by a VME corresponding read or write cycle at address 0x32101000.

- USB register access

Each module can be individually identified over the USB bus by its serial number. An access to a user register mapped at offset 0x1000 on the local bus can be triggered by a USB access cycle at address 0x1000.

12.3.3 VME Interface Registers (0x8000-0x80FF)

Address	Register/Content	Read/Write
BA + 0x8000	VME Control Register	R/W
BA + 0x8004	<i>reserved</i>	
BA + 0x8008	VME Interrupt Level	R/W
BA + 0x800C	VME Interrupt Status ID	R/W
BA + 0x8010	<i>reserved</i>	
BA + 0x8014	<i>reserved</i>	
BA + 0x8018	<i>reserved</i>	
BA + 0x8020	Scratch Register	R/W
BA + 0x8024-0x80F8	<i>reserved</i>	
BA + 0x80FC	VME Base Address	R

Tab. 12.2: VME interface registers

VME interface registers implement VME-related control and status information. They can also be accessed from USB for monitoring or configuration.

12.3.4 VME Control Register

Bit	Description
[31:1]	<i>reserved</i>
[0]	VME Interrupt Mode 0 = Release On Register Access (RORA) Interrupt mode (default) 1 = Release On Acknowledge (ROAK) Interrupt mode

12.3.5 VME Interrupt Level Register

Bit	Description
[31:3]	<i>reserved</i>
[2:0]	VME Interrupt Level: 0 = interrupts are disabled (default) n = interrupts on IRQn line are enabled (n = 1, 2, ..., 7)

12.3.6 VME Interrupt Status ID Register

Bit	Description
[31:0]	This register contains the 32-bit STATUS/ID set by the module on the VME data bus during the Interrupt Acknowledge cycle

12.3.7 Scratch Register

Bit	Description
[31:0]	This register allows to perform 32-bit accesses for test purposes. Default value is 0xAAAAAAAA

12.3.8 VME Base Address Register

Bit	Description
[31:0]	This register allows to read the value of on-board rotary switches (see Fig. 9.5). It is meant to be used from the USB interface for testing purposes

12.3.9 Configuration ROM (0x8100-0x81FF)

The following registers contain module configuration information according to **Tab. 12.3**.

Only the 8 LSBs of each location of the Configuration ROM are significant.

Description	Address	Content
checksum	0x8100	An eight bit 2's complement binary checksum. The sum of the bytes starts from offset 0x8104 for the number of bytes specified in the length field (inclusive)
checksum_length2	0x8104	0x00
checksum_length1	0x8108	0x00
checksum_length0	0x810C	0x20
constant2	0x8110	0x84
constant1	0x8114	0x84
constant0	0x8118	0x01
c_code	0x811C	0x43
r_code	0x8120	0x52
oui2	0x8124	0x00
oui1	0x8128	0x40
oui0	0x812C	0xE6
version	0x8130	0x00
board2	0x8134	0x00
board1	0x8138	0x09
board0	0x813C	0xBF
revis3	0x8140	0x00
revis2	0x8144	0x00
revis1	0x8148	0x00
revis0	0x814C	PCB revision
sernum3	0x8178	PID 32-bit (MSB) / <i>reserved</i>
Sernum2	0x817C	PID 32 bit / <i>reserved</i>
sernum1	0x8180	PID 32 bit / PID 16 bit (MSB) / Serial Number (MSB)
sernum0	0x8184	PID 32 bit (LSB) / PID 16 bit (LSB) /Serial Number (LSB)

Tab. 12.3: ROM Address Map of the V2495



Note: The oui0/1 fields represent CAEN Manufacturer identifier (IEEE OUI), which is equal to 0x40E6.



Note: The version field identifies the module version (0x00 = V2495).

Note: Old boards are identified by the Serial Number. It is a 16-bit value (decimal number between 0 and 9999) readable by accessing at 0x8180 (MSB) and 0x8184 (LSB) addresses: if the serial number on the module front panel is 1245 (hex 0x4DD), for instance, the Serial Number's MSB (0x8180) will be 0x04, while the Serial Number's LSB (0x8184) will be 0xDD.



On new boards, the Serial Number has then been replaced by the PID. It initially was a 16-bit value (decimal number between 10000 and 65535) readable by accessing 0x8180 (MSB) and 0x8184 (LSB) addresses.

On very new boards, the PID was finally extended to 32 bits and readable by accessing 0x8178 (MSB), 0x817C, 0x8180, and 8184 (LSB) addresses

12.3.10 Configuration and Status Registers (0x8200-0x83FF)

Address	Register/Content	Read/Write
Base + 0x8200	MFPGA firmware revision	R
Base + 0x8204 ÷ 0x8214	<i>reserved</i>	
Base + 0x8218	Software reset	W
Base + 0x8220	Scratch register	R/W
Base + 0x8224 ÷ 0x83FC	<i>reserved</i>	-

Tab. 12.4: CSR registers

12.3.11 MFPGA Firmware Revision Register

Bit	Description
[31:16]	reserved
[15:8]	Major revision number
[7:0]	Minor revision number

12.3.12 Software Reset Register

Bit	Description
[31:0]	The value written into this register will determine the kind of software reset: 1 = generate a local bus reset only (nLBRES local bus signal) Others = reserved for future options

12.3.13 Scratch Register

Bit	Description
[31:0]	This register allows to perform 32-bit accesses for test purposes. Default value is 0xAAAAAAAA

12.3.14 Flash Configuration (0x8500-0x8AFF)

This address range is reserved to flash remote programming.



Note: access to the FLASH is through the provided functions of the PLULib library (see Sec. 11.2).

12.3.15 Internal Scratch SRAM(0x8C00-0x8FFF)

This area is available either for test access or for volatile data storage. Any address in this interval is implemented by an internal RAM location.

13 Firmware Development

13.1 Introduction

The goal of this chapter is to let the User familiarize with the information and the tools needed to develop proprietary firmware for the V2495 board.

A thorough description of the main firmware functionalities will be provided; the features of essential components like the local bus interface and the gate and delay generator will also be discussed.

Basically, two ways of making firmware can be used:

- VHDL tools on the market. This method is intended for experts in FPGA programming.
- The SCI-Compiler, Graphical Programming Language for CAEN Open FPGA Boards. This new method is available for all level users, but principally for those who are not familiar with VHDL or other FPGA programming languages.

The first section briefly introduces SCI-Compiler and gives references to find all the needed detailed information.

Following, the document focuses on the VHDL method, describing also four demos provided in the UFPGA flash memory. A step-by-step guide will be given to run the examples. Their goal is to provide an extensive overview of the main functionalities of the V2495 board and of its mezzanine cards. The code of these demos, together with a firmware template, can be downloaded from the CAEN website. When developing custom projects, it is recommended to start with the included template firmware, as it includes the correct FPGA pinning and constraints. A short description of the user top-level I/O signals will also be given.

The V2495 board is an upgraded version of the V1495 board. The two boards have the same I/O connectors and mezzanine card support. On the firmware development side, there are differences, mainly due to the new Gate and Delay Generator and to the newly introduced USB connection. Please refer to Sec. 13.6 for the details to port the V1495 projects on the V2495 board.



Note: Due to the different I/O pin mapping and FPGA devices, the FPGA bit-streams and the projects previously developed for the V1495 board are not compatible with the V2495 board.

13.1.1 Safety Notice

When working with mezzanine boards featuring input channels, particular attention must be paid during the firmware development.

The signals from such channels, after electrical conditioning on the mezzanine, get into the USER FPGA inputs. At power-on, if the firmware loaded on the FPGA drives those inputs without the appropriate precautions, severe conflicts may be generated, and hardware components could be damaged if the current requirements exceed the current limit provided by the motherboard on the 3V3 supply voltage.

CAUTION: Firmware development requires special attention.



WITHOUT PROPER ATTENTION, LOADING ON THE USER FPGA A FIRMWARE DRIVING THE INPUTS OF MEZZANINE BOARDS MAY GENERATE CONFLICTS LEADING TO SEVERE DAMAGE OF HARDWARE COMPONENTS.

Some useful methods for coding the firmware to avoid conflicts are described in Sec. 13.3.1.

13.2 Sci-Compiler

Sci-Compiler represents an innovative approach to simplify firmware development on CAEN Open FPGA boards. This software utilizes a block-diagram-based approach that incorporates a range of high-level functionalities (blocks) to conceal the real firmware coding. As a result, it becomes possible to create and compile custom firmware from a basic block diagram structure.

The power of Sci-Compiler is to make it possible to program a FPGA without strictly requiring knowledge of FPGA programming languages.

Please, find all the information and material about Sci-Compiler, and how to use it with your CAEN Programmable Logic Unit, on the dedicated website:

<https://www.sci-compiler.com/>

13.3 User FPGA I/O Ports

This section illustrates the I/O ports of the UFPGA. Port names are the same of the VHDL entity top-level ports used in the template and demo firmware.

➤ **Clock:** The user FPGA receives the board system clock

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
CLK	1	Input	50 MHz system clock

Tab. 13.1: Clock ports description table

➤ **Mainboard Robinson Nugent connector ports:** the ports A and B are input only. They feature 32 input channels that reach the UFPGA as 32 single-ended LVTTTL lines (3.3 V).

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
A	32	Input	A port values
B	32	Input	B port values
C	32	Output	C port value

Tab. 13.2: Mainboard Robinson-Nugent connector description table

➤ **LEMO ports:** each of the LEMOs on the front panel can be used as input or output. The signals used are the following:

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
GIN	2	Input	Input values for G0, G1
GOUT	2	Output	Output values for G0, G1
SELG		Output	NIM/TTL selector 0 = NIM 1 = TTL
nOEG		Output	Output enable (active low) (0=output, 1=input)

Tab. 13.3: LEMO G ports description table

It should be noted that the ports G0, G1 can be set as inputs in two different ways:

- By setting nOEG=1 and driving the LEMO inputs. In this way both ports will be used as inputs; their status can be read from GIN[0] and GIN[1].
- By setting to 0 both nOEG and the output signal of the input port and enabling the related 50 Ohm termination (see Chap. 5). In this way it is possible to force a logic level without damaging the output and to use one port as an input and the other as an output.

Example: G0 input, G1 output

nOEG=0

GOUT[0]=0

Enable the 50 Ohm G0 termination

In this way, it is possible to provide an input on the G0 channel, while having an output on the G1 port (through the GOUT[1] signal). Note that in this configuration G1 should not be externally forced, as this might damage the input circuit.

The 500hm termination should also be enabled when a NIM input is provided (instead of a TTL). When the NIM logic level is chosen the logic levels are inverted with respect to the TTL case: It is up to the firmware to handle this inversion, for example using the SELG signal to invert the logic level as shown in the following VHDL assignment:

```
GIN_MOD <= GIN[0] when SELG='1' else not GIN[0];
```

➤ **Expansion I/O ports:** for each mezzanine, **Tab. 13.4** shows the supported signals (X = D, E, F).

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
IDx	3	Input	Card ID "000" = A395A "001" = A395B "010" = A395C "011" = A395D "100" = A395E "111" = No mezzanine present
SELx	1	Output	NIM/TTL selector 0 = NIM 1 = TTL
nOEx	1	Output	Output enable (active low) 0 = output 1 = input
X	32	Input/Output	Data bus to/from the mezzanines

Tab. 13.4: Expansion I/O ports description table

Please note that:

- The nOEx signal is meaningful for the A395B, A395C and A395D mezzanines, while SELx is meaningful only for the A395D mezzanine card. If the A395D is not used, the nOEs and SELx signals can be left undriven. When the A395B or A395C are used, the nOEx signal must be set low (nOEx = 0).
- Mezzanines with 32 I/O signals have a one-to-one correspondence between physical signals and I/O pins (i.e. X[i] corresponds to the i-th channel of the mezzanine).

The A395D mezzanine card also allows its 8 channels to be individually used as inputs.

The steps to do are:

- set nOEx to 0 (all channels are outputs);
- terminate to 50 Ohm the channel(s) intended to be used as input.

The second step is possible by moving to 1-2 the relevant jumper on the mezzanine board which relies next to each channel, as in **Fig. 13.1**.

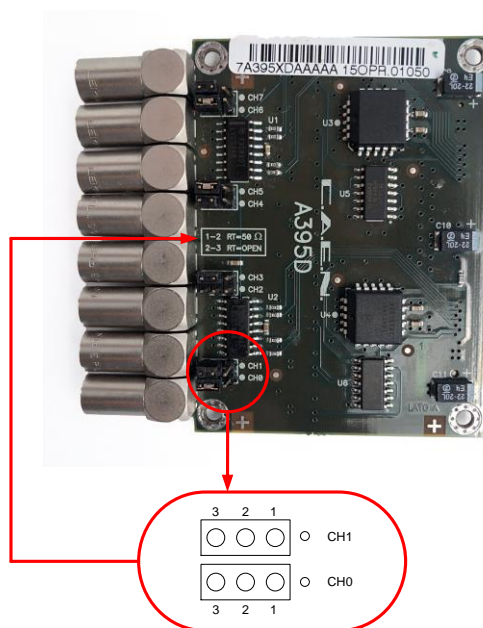


Fig. 13.1: A395 jumpers for the channel impedance selection

In case the A395D mezzanine is used, the mapping between the external channels and the X bus is shown in **Tab. 13.5**. A schematic view of the A395D board is shown in **Fig. 13.2**.

CHANNEL	INPUT SIGNALS	OUTPUT SIGNALS
0	X[2]	X[0]
1	X[18]	X[16]
2	X[3]	X[1]
3	X[19]	X[17]
4	X[14]	X[12]
5	X[30]	X[28]
6	X[15]	X[13]
7	X[31]	X[29]

Tab. 13.5: A395D mapping

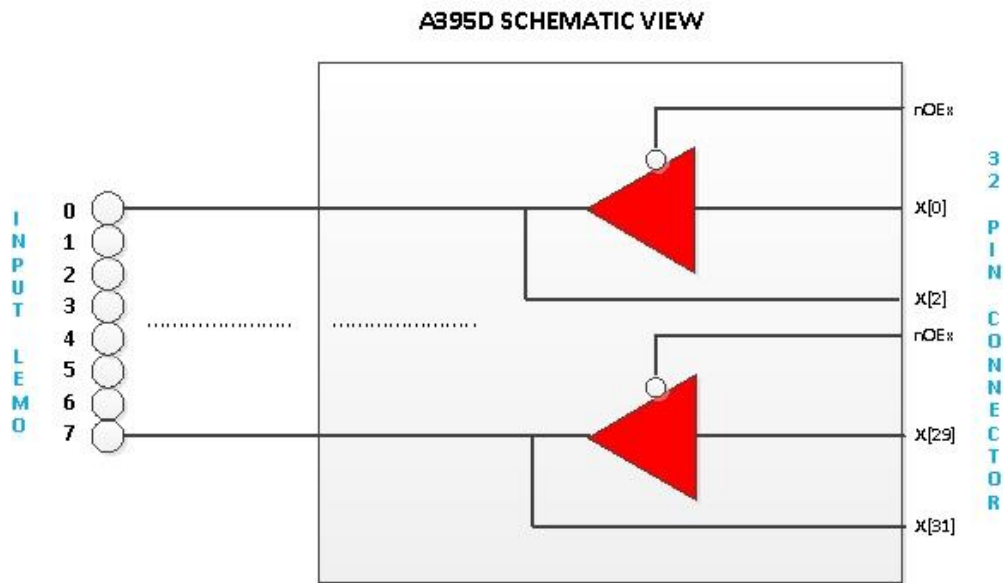


Fig. 13.2: Simplified scheme related to **Tab. 13.5**

For example:

- A395D channel 0 can be driven with signal X[0] and its status can be read from X[2].
- A395D channel 1 can be driven with signal X[16] and its status can be read from X[18].

➤ **User LEDs:** Refer to the eight User LEDs on the front panel (see Chap. 4).

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
LED	8	Output	LED drivers

Tab. 13.6: LED ports description table

In order to switch on one of the eight LEDs on the front panel, the corresponding signal (LED[7:0]) should be set to 1.

➤ **Gate & Delay Generator interface ports:** The GDG is connected to the UFGPA via the following signals:

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
GD_START	32	Output	GDG start signals
GD_DELAYED	32	Input	GDG output signals
SPI_MISO	1	Input	SPI MISO (Master Input Slave Output)
SPI_SCLK	1	Output	Serial clock
SPI_CS	1	Output	SPI Chip Select
SPI_MOSI	1	Output	SPI MOSI (Master Output Slave Input)

Tab. 13.7: Gate and Delay Generator ports description table

➤ **Local Bus ports:** The Local Bus signals are shown in **Tab. 13.8**.

SIGNAL NAME	WIDTH	TYPE	DESCRIPTION
nLBRES	1	Input	Bus reset (active low)
nBLAST	1	Input	Last cycle (active low)
WnR	1	Input	Write/Read cycle 0 = read 1 = write
nADS	1	Input	Address strobe (active low)
nREADY	1	Output	Slave ready/Prefetch request
LAD	16	Input/Output	Data/address bus

Tab. 13.8: Local Bus ports description table

13.3.1 Preventing from User FPGA Input Conflicts

In this section, some technics are described for the firmware development to avoid conflicts when loading custom firmware on the USER FPGA which drives the inputs of an A395x mezzanine (see Sec. 13.1.1).

- Put the following constant declarations in a package or in the architecture declarative region:

```
constant A395A_ID_CODE : std_logic_vector(2 downto 0) := "000" ;
constant A395B_ID_CODE : std_logic_vector(2 downto 0) := "001" ;
constant A395C_ID_CODE : std_logic_vector(2 downto 0) := "010" ;
constant A395D_ID_CODE : std_logic_vector(2 downto 0) := "011" ;
constant A395E_ID_CODE : std_logic_vector(2 downto 0) := "100" ;
```

- Put the code below into your top-level architecture, where nOED, nOEE and nOEF are the top-level ports to control mezzanine I/O direction for port D, E and F respectively; IDD, IDE and IDF are the top-level ports to sense the mezzanine ID code for auto-detection; d_oe_n_reg_i, e_oe_n_reg_i and f_oe_n_reg_i are the user internal signals to drive mezzanine direction.

If the mezzanine being detected on a slot has inputs, this code avoids driving them.

```
nOED <= d_oe_n_reg_i and d_oe_n_auto;
nOEE <= e_oe_n_reg_i and e_oe_n_auto;
nOEF <= f_oe_n_reg_i and f_oe_n_auto;
```

```
d_oe_n_auto <= '0' when ((IDD = A395B_ID_CODE) or (IDD = A395C_ID_CODE) or
(IDD = A395E_ID_CODE)) else
    '1';
```

```
e_oe_n_auto <= '0' when ((IDE = A395B_ID_CODE) or (IDE = A395C_ID_CODE) or
(IDE = A395E_ID_CODE)) else
    '1';
```

```
f_oe_n_auto <= '0' when ((IDF = A395B_ID_CODE) or (IDF = A395C_ID_CODE) or
(IDF = A395E_ID_CODE)) else
    '1';
```

13.4 Local Bus Interface

The Local Bus (LB) is the communication interface between the MFPGA and the UFPGA.

It is made of a Master (LBM), implemented inside the MFPGA, and of a Slave (LBS), implemented inside the UFPGA. The communication protocol between the LBM and the LBS is based on the following signals. In what follows OUT(IN) means that the signal goes from the LBM(LBS) to the LBS(LBM) and AL stands for active-low:

- nADS (OUT, AL): it is set by the LBM when a r/w operation is performed. The LBS samples the register address from LAD when nADS is set.
- WnR (OUT): it notifies the LBS whether the access is in write- (WnR=1) or read- (WnR=0) mode. The value of WnR is relevant only when nADS is set.
- nREADY (IN, AL): It is a dual purpose signal. it is set by the LBS to notify the LBM that the LBS is ready for r/w data transfer. It can also be used for the data prefetch mechanism (see next).
- nBLAST (OUT, AL): it signals the last cycle of a data transfer. It is set when either the LBS is not ready or the LBM cannot accept data (e.g. because the FIFO used for data prefetch is full).
- LAD (IN/OUT): the 16-bit bus used to read/write both address and data.

LBM can generate two kind of transfers over the local bus:

- Single word (32-bit) read/write transfer
- Multi word prefetch transfer

Single word transfers are initiated by the LBM for register access. It is composed by a single clock address phase and two 16-bit data phases. A data phase is completed if the LBS asserts nREADY low. The transfer ends on the second data phase when the LBM asserts the nBLAST signal low.

Examples of the signal logic taken using Altera™ Signal Tap are shown in Fig. 13.3 and Fig. 13.4. For a read and a write access on the LBS.



Fig. 13.3: Local bus signals at a write access (x8BADF00D is written on register x1800)



Fig. 13.4: Local bus signal at a read access (x8BADF00D is read from register x1800)

A data prefetch mechanism, implemented in the MFPGA, stores User data into a MFPGA local data queue (prefetch data queue). The MFPGA prefetch queue data is available for readout over the VME or USB interface (see Sec. 12.3). The prefetch mechanism is illustrated by Fig. 13.5.

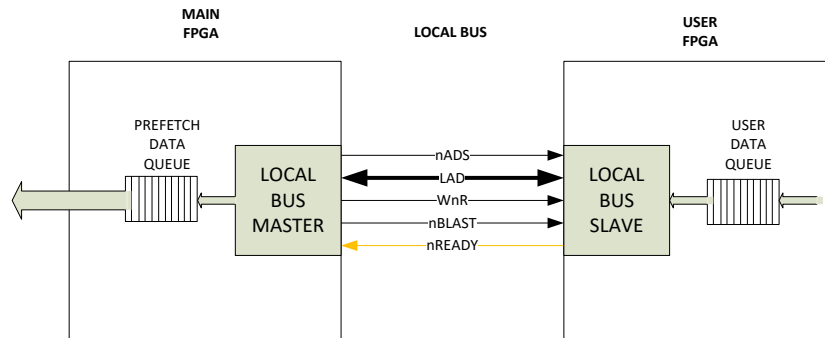


Fig. 13.5: Prefetch mechanism

Prefetch read cycles are initiated by the UFGPA logic: nREADY local bus signal must be used by the User logic to request a new data prefetch cycle by the local bus master (MFPGA): The request is active when the nREADY is low. The local bus master should have an internal prefetch queue (FIFO component). If a user request is pending and the local bus master has available space into the prefetch queue, it will start an internal block transfer from local bus address 0x0000 (fixed). The User logic is required to respond only to address 0x0000: data from its data queue are made available to the V2495 local bus. If a new register access is requested to the local bus master while a prefetch cycle is ongoing, the prefetch cycle will be interrupted by asserting the nBLAST signal and the register access will be served with priority. At the end of a register access, the user logic can keep the nREADY signal active to request a new prefetch cycle to the LBM, which will fetch new data in its queue.

Please refer to the lb_int.vhd source code in the User demo firmware projects.: it is a Local Bus slave implementation provided by CAEN as a reference.

The lb_int.vhd found in the Pattern Recorder demo firmware (see Sec. **Pattern Recorder Demo Description**) is a demonstration of user logic implementation of the data prefetch mechanism.

13.5 Gate and Delay Controller

13.5.1 General Description

The GDG can be used by the user logic to gate and delay up to 32 digital signals. The delay and gate values can be set using a dedicated serial bus (SPI bus). The signals are sent to the GDG, where they are gated and delayed according to the user settings and then returned to the UFPGA. The width of the delayed signal only depends on the gate value set and is not related to the width of the incoming signal.

The gate and delay values are 16-bit wide and **their sum cannot exceed 65535 (0xFFFF)**. They are both generated by using an internal clock, which computes the number of clock cycles between the incoming signal and the leading and trailing edge of the gate signal. Referring to **Fig. 13.6**, the times of occurrence of the leading (T_{lead}) and trailing (T_{trail}) can be obtained using the following formulas, where $N_g(N_d)$ is the gate(delay) value set by register and T_0, T_1 are the time values reported in **Tab. 13.9**:

$$T_{lead} = \begin{cases} 0 & \text{if } N_d=0 \\ T_0+T_1(N_d-1) & \text{if } N_d>0 \end{cases}$$

$$T_{trail} = \begin{cases} 0 & \text{if } N_d=N_g=0 \\ T_0+T_1(N_d+N_g-1) & \text{if } (N_d+N_g)\geq 1 \end{cases}$$

The relationship between T_{lead}, T_{trail} and the delay and gate duration is:

$$T_{delay}=T_{lead}$$

$$T_{gate}=T_{trail}-T_{lead}$$

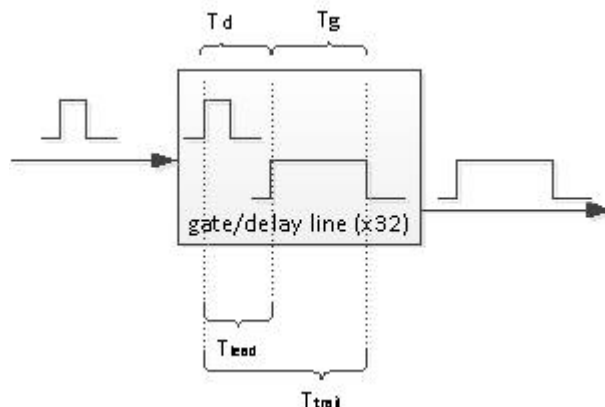


Fig. 13.6: Gate and Delay parameters representation

T_1 represents the minimum increment of either the gate or the delay value. The presence of T_0 is due to a slightly longer duration of the minimum delay time increment (or gate increment, if the $N_g=0$) with respect to the standard T_1 increment. It should be noted that both T_1 and T_0 can vary from channel to channel, with an expected variation interval of $\pm 10\%$ for both. Please also consider that, when setting $N_d=0$, the observed delay of the outgoing signal with respect to the incoming one is due to the paths on the PCB and inside the FPGAs, which are delay channel-dependent.

Example 1: If the delay value is set to 0x0 and the gate value is set to 0x5, the gate will last $12.2+10.7*4=55$ ns.

Example 2: If the delay value is set to 0x8 (typ. $12+7*10.7=86.9$ ns), the maximum possible gate value is 0xFFFF (typ. $65527*10.7 \approx 701$ μ s).

Example 3: If the delay value is set to 0xFFFF (≈ 701 μ s), the maximum possible gate value is 0x8 (typ. 86.9 ns).

PARAMETER	VALUE
T_0	12 ns (typ.) $\pm 10\%$
T_1	10.7 ns (typ.) $\pm 10\%$
T_{max}	$T_0 + T_1 (2^{16}-1)$

Tab. 13.9: Main parameters of the Gate and Delay Generator

The UFPGA can set the relevant configuration registers and read data from the generator through the SPI protocol. CAEN does not provide a detailed description of the communication protocol over the SPI bus for GDG configuration. A VHDL component is provided in the `gd_control.vhd` source code (GD_CONTROL), included in all the user demo firmware.

GD_CONTROL implements the following registers that can be accessed from the local bus. The LB_INT component reserves addresses starting from 0x7F00 to GD_CONTROL access. LB_INT and GD_CONTROL are connected by a dedicated interface for register write and read.

A set of LB registers are used to configure the GDG, as described in **Tab. 13.10**:

ADDRESS	REGISTER/CONTENT	ACCESS MODE		Read/Write
Base + 0x7F00	Data Write	A24/A32	D16/D32	R/W
Base + 0x7F04	Command register	A24/A32	D16/D32	R/W
Base + 0x7F08	Control register	A24/A32	D16/D32	R/W
Base + 0x7F0C	Data read	A24/A32	D16/D32	R
Base + 0x7F10	Status register	A24/A32	D16/D32	R

Tab. 13.10: Local Bus registers description for the Gate and Delay Generator configuration

13.5.2 Register Description

- **DATA WRITE:** the datum (gate or delay) must be written here before it is transmitted through SPI to the GDG.

Address: 0x7F00.

Mode: Read and Write.

Bit	Description
[31:0]	Gate or delay datum to transmit to the GDG

- **COMMAND register:** it is where the action to be performed is set. The action depends on the value of the 2 LSBs of the Control register (read or write mode): one of these bits should be asserted to execute the related action. The channel interested by the action is set through the 6 LSBs of the register (relevant when [15:0] = 0x100 in write mode and [15:0] = 0x2000, 0x3000 in read mode).

Address: 0x7F04

Mode: Read and Write

Write Mode

Bit	Description
[31:16]	<i>reserved</i>
[15:0]	0x2000 = the internal gate value is modified with the content of the data write register (but not sent to the DFPGA) 0x3000 = the internal delay value is modified with the content of the data write register (but not sent to the DFPGA) 0x0100(+channel) = the gate AND delay values of the selected channel are modified with the internal values, sent to the DFPGA by the UFPGA through SPI 0x0300 = the delay of all channels is reset 0x0400 = the delay of all channels is calibrated 0x0500 = the internal gate and delay values are broadcast to all 32 channels

Read Mode

Bit	Description
[31:16]	<i>reserved</i>
[15:0]	0x2000(+channel) = the gate value of the specified channel is read through SPI 0x3000(+channel) = the delay value of the specified channel is read through SPI

➤ **CONTROL register:** bit[0] sets a write or read action.

Address: 0x7F08.

Mode: Read and Write.

Bit	Description
[31:2]	<i>reserved</i>
[1]	1 = a read action is performed
[0]	1 = a write action is performed

➤ **DATA READ:** it is where the datum (gate or delay) can be read after an SPI read access to the GDG has been performed (see the Read Mode of the COMMAND register).

Address: 0x7F0C.

Mode: Read only.

Bit	Description
[31:0]	Gate or delay datum resulting from READ MODE access to GDG

➤ **STATUS register**

Address: 0x7F10.

Mode: Read only.

Bit	Description
[31:1]	<i>reserved</i>
[0]	Gate and delay ready signal (when 0, the Gate and Delay controller is busy. A new command to the Gate and Delay controller should not be issued before this bit sets back to 1)

13.5.3 Example Procedures

- **MODIFY THE GATE OR THE DELAY VALUE OF A CHANNEL**

The gate or the delay of a signal from the UFGPA can be modified by following this procedure (the registers quoted are accessible via VME):

- Set a delay (gate) value in the DATA WRITE register
- Set the COMMAND register to 0x2000 (0x3000) to modify the delay (gate) internal value
- Set the control register to 0x1/0x0
- Set the COMMAND register to 0x100 + CHANNEL (6 bits) to write the gate and delay values on the FPGA through the SPI bus, for the channel specified by the six LSBs. Note that the gate and delay values are written in the same action
- Set the CONTROL register to 0x1/0x0

- **READ THE GATE OR THE DELAY VALUE OF A CHANNEL**

- Set the COMMAND register to 0x2000 (0x3000) + CHANNEL (6 bits) to read the delay (gate) value of a specific channel
- Set the CONTROL register to 0x2/0x0
- Read the required value in the DATA READ register

- **BROADCAST A GATE OR DELAY VALUE OF A CHANNEL**

- Set the desired values of the delay and gate values (see the first example, first two steps)
- Set the COMMAND register to 0x500
- Set the CONTROL register to 0x1/0x0

Note that in the case of a broadcast command the delay and gate values are serialized to the GDG at the same time. The bits related to the channel index (six LSBs of the CONTROL register) are irrelevant in this case.

13.6 Porting V1495 to V2495

Firmware designs targeted to the V1495 User FPGA can be ported to V2495 by keeping in mind the following differences between the two modules:

- The V2495 FPGA device is different (Cyclone V versus Cyclone I) and with larger logic resources. While there will be no resource constraints, the FPGA configuration scheme and output binary files are different for the two boards.
- A design that used on-board delay lines with V1495 must be redesigned to take into account the new features and characteristics of the V2495 GDG.
- The address map of the V1495 VME FPGA and V2495 MAIN FPGA have some differences to take into account:
 - Registers in V1495 are mapped at 16-bit aligned addresses, while V2495 features a 32-bit aligned address map. Access in VME D16 mode is still possible with V2495, but discouraged. Register access should always be in D32 mode.
 - Common registers with different address:
 - VME Interrupt level register:
 - 0x8004 in V1495
 - 0x8008 in V2495
 - VME Interrupt Status/ID register:
 - 0x8006 in V1495
 - 0x800C in V2495
 - GEO address register:
 - 0x8008 in V1495
 - 0x8010 in V2495
 - Firmware revision:
 - 0x800C in V1495
 - 0x8200 in V2495
- The local bus map is the same for V1495 and V2495. Block transfers are allowed only in the 0x0000-0x0FFF address interval. The same user data prefetch mechanism is implemented. Local bus register accesses are mapped to the same 0x1000-0x7FFF address interval.



Note: The V2495 no longer requires the 0x100C local bus address to be reserved for user firmware revision register with special constraints due to the firmware licensing mechanism. In V2495 all user register can be implemented in the allowed address range without any constraints of functionality or content

- The flash access register map and protocol is different between the two boards: the specific setting and tools must be used for each module.

14 Demo Firmware

14.1 Introduction

This chapter describes a set of UFPGA demos that CAEN provides as demonstration of the V2495 functionalities and as a guide for developing customized user application firmware.

The demos can be loaded on the UFPGA from a 6-page FLASH memory through the SW5 rotary switch (see Sec. 9.5). The switch position 0 loads the Factory firmware, while positions 1 to 5 load different demo firmware described in the following paragraphs. Positions higher than 5 load the Factory firmware (i.e. they are functionally equivalent to position 0).

To run a firmware “as it is”, it is required to use the functions of the CAEN PLULib library to access the proper (refer to Sec. 11.2). To modify the demos and upload the new firmware on the FPGA, basic knowledge of VHDL language and Altera Quartus II software are required.

In what follows, the features of the four demos loaded in the UFPGA’s flash memory will be described.

By default, each demo lights front panel user LED with the following configurations:

Demo	Description
Demo1	LED 0 ON; others OFF
Demo2	LED 1 ON; others OFF
Demo3	LED 1 and LED 0 ON; others OFF
Demo4	LED 2 ON; others OFF

14.2 Demo Structure

All demo projects feature a common file structure:

- A configuration file (**v2495_package.vhd**), allowing to set the number of CONFIG and MONITOR registers, their respective base address, the demo ID and the firmware revision. The CONFIG registers are mapped between 0x1000 and 0x17FC, while the MONITOR registers are mapped between 0x1800 and 0x1FFC.
- A gate and delay block (**gd_control.vhd**), acting as a controller for the GDG (the example in Sec. 14.7 specifically focuses on the configuration of GDG delays);
- The local bus slave (**lb_int.vhd**), allowing to read/write the registers needed in the demo operations;
- The SPI master (**spi_master.vhd**) and interface (**spi_interface.vhd**), allowing the communication to/from the GDG to be serialized;
- A demo-specific part, containing core demonstration logic.

14.3 Demo Setup

In order to run one of the demo firmware, the following instructions should be followed:

- Select the desired position of the rotary switch and then restart the crate
- Connect to the V2495 board to read/write registers
- Set the required configuration through the control register(s).

14.4 Gate Pattern Demo Description

14.4.1 Introduction

In this example, a logic combination of the input port signals A and B is sent to the C connector (32 lines). The user can choose the output among 10 available options by setting the 4 LSBs of the control register (see the register list). Apart from the value of A, B, A AND B and A OR B, the aforementioned signals in “capture” mode (a bit is set whenever a signal shows up) can be selected.

14.4.2 Register Map

In this example, 9 registers are used, 5 of which (MONITOR registers) can only be read and 4 (CONTROL registers) can be both read and written. All registers are 32 bit wide and can be accessed in single access mode.

ADDRESS	REGISTER/CONTENT	ACCESS MODE		Read/Write
Base + 0x1000	Firmware version	A24/A32	D16/D32	R
Base + 0x1004	Value of port A (input)	A24/A32	D16/D32	R
Base + 0x1008	Value of port B (input)	A24/A32	D16/D32	R
Base + 0x100C	Value of port C (output)	A24/A32	D16/D32	R
Base + 0x1010	Status register	A24/A32	D16/D32	R
Base + 0x1800	Mask of input port A	A24/A32	D16/D32	R/W
Base + 0x1804	Mask of input port B	A24/A32	D16/D32	R/W
Base + 0x1808	Control register	A24/A32	D16/D32	R/W
Base + 0x180C	User Value of port C	A24/A32	D16/D32	R/W

14.4.3 Register Description

- **FIRMWARE REVISION register:** Contains the firmware revision number.

Address: 0x1000.

Mode: Read only.

Bit	Description
[31:0]	Firmware revision progressive number

- **A-PORT VALUE register:** Contains the 32 input bits of port A.

Address: 0x1004.

Mode: Read only.

Bit	Description
[31:0]	Input value of Port A

- **B-PORT VALUE register:** Contains the 32 input bits of port B.

Address: 0x1008.

Mode: Read only.

Bit	Description
[31:0]	Input value of Port B

- **C-PORT VALUE register:** Contains the 32 output bits of port C (selectable by the user in this demo).

Address: 0x100C.

Mode: Read only.

Bit	Description
[31:0]	Output value of port C

➤ **STATUS register:** Contains status information.

Address: 0x1010.

Mode: Read only.

Bit	Description
[31:5]	reserved
[4]	Register clear signal
[3]	Register gate signal
[2]	External clear signal
[1]	External gate signal
[0]	Data ready

➤ **A-PORT MASK register:** Masks the channels of port A.

Address: 0x1800.

Mode: Read and Write.

Bit	Description
[31:0]	The n-th bit set to 1 means that the corresponding channel of port A is masked

➤ **B-PORT MASK register:** Masks the channels of port B.

Address: 0x1804.

Mode: Read and Write.

Bit	Description
[31:0]	The n-th bit set to 1 means that the corresponding channel of port B is masked

➤ **CONTROL register:** Allows to set the demo configuration.

Address: 0x1808.

Mode: Read and Write.

Bit	Description
[31:9]	reserved
[8]	Allows to select the signal type on ports G0, G1: 0 = NIM level, 1 = TTL level
[7:6]	Reserved
[5]	The gate of input port C ends when this bit is set
[4]	The gate of input port C starts when this bit is set
[3:0]	<p>0x0 = the port A (possibly masked) is sent to C when a gate signal is active. 0x1 = the port B (possibly masked) is sent to C when a gate signal is active. 0x2 = the AND of A and B (possibly masked) is sent to C when a gate signal is active. 0x3 = the OR of A and B (possibly masked) is sent to C when a gate signal is active. 0x4 = the port A (possibly masked) is captured and sent to C when a gate signal is active 0x5 = the port B (possibly masked) is captured and sent to C when a gate signal is active 0x6 = the AND of ports A and B (possibly masked) is captured and sent to C when a gate signal is active 0x7 = the OR of ports A and B (possibly masked) is captured and sent to C when a gate signal is active 0x8 = a clock counter (@ 50 MHz) is sent to C 0x9/0xF = the value of a register is sent to C</p>

➤ **C-PORT USER VALUE register:** Allows to set the C port value when Control register bits[3:0] are set to 0x9/0xF.

Address: 0x180C.

Mode: Read and Write.

Bit	Description
[31:0]	User value of Port C

14.5 Pattern Recorder Demo Description

14.5.1 Introduction

In this demo, a digital pattern recorder is implemented. When a start signal is received, the digital input specified through the control register is sampled at a user-configurable sampling rate, and a user-configurable number of samples are collected in a FIFO. Once all samples have been stored, they can be readout through VME read accesses.

14.5.2 Register Map

In this example, 9 registers are used, 5 of which (MONITOR registers) can be only read and 4 (CONTROL registers) can be both read and written.

The sampling clock can be either internal (100 MHz, generated from the 50 MHz input clock through a PLL) or external, through the G0 connector: in this case a signal compatible with one of the supported levels (NIM or TTL) should be provided.

All registers are 32 bit wide and can be accessed in single access mode.

ADDRESS	REGISTER/CONTENT	ACCESS MODE		Read/Write
Base + 0x0000	FIFO content readout	A24/A32	D16/D32	R
Base + 0x1000	Firmware version	A24/A32	D16/D32	R
Base + 0x1004	Value of port A (input)	A24/A32	D16/D32	R
Base + 0x1008	Value of port B (input)	A24/A32	D16/D32	R
Base + 0x100C	Value of port C (output)	A24/A32	D16/D32	R
Base + 0x1800	Mask of input port A	A24/A32	D16/D32	R/W
Base + 0x1804	Mask of input port B	A24/A32	D16/D32	R/W
Base + 0x1808	Control register	A24/A32	D16/D32	R/W
Base + 0x180C	User Value of port C	A24/A32	D16/D32	R/W

14.5.3 Register Description

- **FIRMWARE REVISION register:** Contains the firmware revision number

Address: 0x1000.

Mode: Read only.

Bit	Description
[31:0]	Firmware revision progressive number

- **A PORT VALUE:** the 32 input bits of port A

Address: 0x1004.

Mode: Read only.

Bit	Description
[31:0]	Input on port A

- **B PORT VALUE:** the 32 input bits of port B

Address: 0x1008.

Mode: Read only.

Bit	Description
[31:0]	Input on port B

- **C PORT VALUE:** the 32 output bits of port C (selectable by the user in this demo)

Address: 0x100C.

Mode: Read only.

Bit	Description
[31:0]	Output to port C

- **A-PORT MASK register:** Masks the channels of port A.

Address: 0x1800.

Mode: Read and Write.

Bit	Description
[31:0]	The n-th bit set to 1 means that the corresponding channel of port A is masked

- **B-PORT MASK register:** Masks the channels of port B.

Address: 0x1804.

Mode: Read and Write.

Bit	Description
[31:0]	The n-th bit set to 1 means that the corresponding channel of port B is masked

- **CONTROL register:** allows to set the demo configuration.

Address: 0x1808.

Mode: Read and Write.

Bit	Description
[31:20]	Number of stored samples in the FIFO
[19:16]	Downsampling factor (frequency divider)
[15:10]	<i>reserved</i>
[9]	Software acquisition start
[8]	Software acquisition stop
[7:6]	<i>reserved</i>
[5:4]	Output selection (port C) 00 = Port A 01 = Port B 10 = clock counter 11 = user output (register 0x180C)
[3:2]	<i>reserved</i>
[1]	The selected clock source 0 = internal clock source 1 = external clock source (G0 port)
[0]	I/O port level 0 = NIM level 1 = TTL level

- **C PORT VALUE register:** allows to set an arbitrary value to port C.

Address: 0x180C.

Mode: Read and Write.

Bit	Description
[31:0]	User output value for port C

14.6 DAC Demo Description

14.6.1 Introduction

In this demo, the use of a A395E mezzanine card to configure a DCC output value on its 8 output channels will be explained. The DAC registers are 16 bits wide, and the dynamic range of the output voltage is +/- 5 V (refer to **Tab. 6.6** for detailed specifications).

14.6.2 Register Map

In this example, 4 registers are used, 2 of which (MONITOR registers) can only be read and 2 (CONTROL registers) can be both read and written. All registers are 32 bit wide and can be accessed in single access mode.

ADDRESS	REGISTER/CONTENT	ACCESS MODE		Read/Write
Base + 0x1000	Firmware Version	A24/A32	D16/D32	R
Base + 0x1004	Mezzanine ID number	A24/A32	D16/D32	R
Base + 0x1800	Control register	A24/A32	D16/D32	R/W
Base + 0x1804	DAC register	A24/A32	D16/D32	R/W

14.6.3 Register Description

- **FIRMWARE VERSION register:** Stores the revision number of the firmware.

Address: 0x1000.

Mode: Read only.

Bit	Description
[31:0]	Revision Number

- **MEZZANINE ID NUMBER register:** Contains the Mezzanine ID values (see **Tab. 13.4**).

Address: 0x1004.

Mode: Read only.

Bit	Description
[31:12]	<i>reserved</i>
[11:8]	Mezzanine ID, port F
[7:4]	Mezzanine ID, port E
[3:0]	Mezzanine ID, port D

- **CONTROL register**

Address: 0x1800.

Mode: Read and Write.

Bit	Description
[31:29]	<i>reserved</i>
[28]	Activation of test mode (sawtooth signal on all channels)
[27:25]	Reserved
[24]	1 = the DAC value is written for the specified mezzanine and channel 0 = the DAC value is read for the specified mezzanine and channel (the result is put in 0x1804)
[23:22]	<i>reserved</i>
[21:20]	Selects the mezzanine for either a write or read access "00" = F "01" = E "10" = D
[19:16]	The 3 LSBs [18:16] select the channel for either a write or read access. If a write access is performed and [19] = 1 all channels are selected for writing; if a read access is performed [19] is ignored
[15:0]	DAC value

➤ **DAC register:** Contains the DAC value of the channel specified by bits[21:16] of the register 0x1800.

Address: 0x1804.

Mode: Read and Write.

Bit	Description
[31:0]	DAC value

Please, note that the DAC value obtained from register 0x1804 is not read from the chip, but it is the last set value for that specific channel.

14.7 Gate and Delay Demo Description

14.7.1 Introduction

In this demo the functionalities and use of the Gate and Delay Generator will be shown. The signal to be delayed can be selected between an internally-generated clock of configurable frequency (submultiples of 50 MHz) and the input from the G0 connector (please refer to Sec. 3.5 for the G0 and G1 port configuration required in this case). An output signal of configurable width and delay with respect to the input signal's leading edge will be available on G1.

14.7.2 Register Map

In this example, 3 registers are used, 1 of which (MONITOR register) can be only read and 2 (CONTROL registers) can be both read and written. All registers are 32-bit wide and can be accessed in single access mode.

ADDRESS	REGISTER/CONTENT	ACCESS MODE		Read/Write
Base + 0x1000	Firmware Version	A24/A32	D16/D32	R
Base + 0x1800	Control register	A24/A32	D16/D32	R/W
Base + 0x1804	Clock frequency register	A24/A32	D16/D32	R/W

The registers of the Gate and Delay controller are used to configure the GDG parameters.

ADDRESS	REGISTER/CONTENT	ACCESS MODE		Read/Write
Base + 0x7F00	Data write register	A24/A32	D16/D32	R/W
Base + 0x7F04	Command register	A24/A32	D16/D32	R/W
Base + 0x7F08	Control register	A24/A32	D16/D32	R/W
Base + 0x7F0C	Data read register	A24/A32	D16/D32	R
Base + 0x7F10	Status register	A24/A32	D16/D32	R

14.7.3 Register Description

- **FIRMWARE VERSION register:** Stores the revision number of the firmware.

Address: 0x1000.

Mode: Read only.


Bit	Description
[31:0]	Revision Number

- **CONTROL register:**

Address: 0x1800.

Mode: Read and Write.

Bit	Description
[8:4]	The DFPGA channel used to delay the input signal
[1]	Input signal selection: 0 = clock signal (frequency set by bits [8:4]) 1 = G0 input
[0]	I/O port level selection: 0 = NIM level 1 = TTL level

 **WARNING:** When the G0 connector is used as an input, the user should follow the procedure described in Sec. 13.2.

- **CLOCK FREQUENCY register:** Sets the value of the frequency divider factor of the clock selectable as input (0x0 = 50 MHz, 0x1= 25 MHz,).

Address: 0x1804.

Mode: Read and Write.

Bit	Description
[31:0]	Frequency divider factor 0x0 = Clock frequency is 50 MHz 0x1 = Clock frequency is 25 MHz ...

- **DATA WRITE register:** The information written in this register is sent to the GDG.

Address: 0x7F00.

Mode: Read and Write.

Bit	Description
[31:0]	Data

- **COMMAND register**

Address: 0x7F04.

Mode: Read and Write.

Bit	Description
[31:16]	reserved
[15:12]	Control register[0]=1: 0x2 = The content of the Data write register is written in the gate internal buffer 0x3 = The content of the Data write register is written in the delay internal buffer Control register[1]=1: 0x2 = The gate value of the channel specified by [7:0] is read 0x3 = The delay value of the channel specified by [7:0] is read
[11:8]	0x1 = The values of gate and delay previously buffered using [15:12] are sent to the DFPGA for the channel specified by [7:0] 0x3 = The delays are reset 0x4 = The delays are calibrated 0x5 = The values of gate and delay previously buffered using [15:12] are broadcast to all channels
[7:0]	Delay channel selection (the 3 MSBs should be set to 0)

- **CONTROL register**

Address: 0x7F08.

Mode: Read and Write.

Bit	Description
[30:2]	reserved
[1]	1 = Start of read operation
[0]	1 = Start of write operation

- **DATA READ register:** The information from the DFPGA can be read in this register.

Address: 0x7F0C.

Mode: Read only.

Bit	Description
[31:0]	Data

➤ **STATUS register**

Address: 0x7F10.

Mode: Read only.

Bit	Description
[31:1]	<i>reserved</i>
[0]	Gate and delay ready signal (when 0, the Gate and Delay controller is busy. A new command to the Gate and Delay controller should not be issued before this bit sets back to 1)

15 FW2495SC Pay Firmware

CAEN provides the FW2495SC pay firmware for the DT5495 and V2495 boards. By loading this firmware on the USER FPGA of the board, it can be used as a Multievent latching scaler housing up to 160 independent counting channels (reachable thanks to the channel extension given by the x395 mezzanines).

The firmware is downloadable as free trial from CAEN website at the FW2495SC page and will work fully functional for 30 minutes; rebooting the board gives another 30-minute session. The user must then purchase a license to unlock the firmware and use it without time limitation.

In order to demonstrate the FW2495SC firmware, the PLUscaler_daq is web available, including the source code as a base for the user development of customized applications (see Sec. **11.2**).

For a detailed description of the firmware and related software, please refer to the FW2495SC User Manual **[RD5]**.

16 Software Development

Software applications can be developed for the V2495 by using the functions and features provided by the CAEN PLULib library **[RD4]**.

CAEN PLULib library requires the Main FPGA Application Firmware revision 1.4 or higher!

1 Technical Support

To contact CAEN specialists for requests on the software, hardware, and board return and repair, it is necessary a MyCAEN+ account on www.caen.it:

<https://www.caen.it/support-services/getting-started-with-mycaen-portal/>

All the instructions for use the Support platform are in the document:



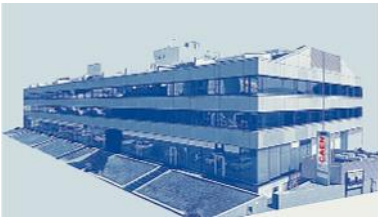
A paper copy of the document is delivered with CAEN boards.

The document is downloadable for free in PDF digital format at:

<https://www.caen.it/safety-information-product-support>



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