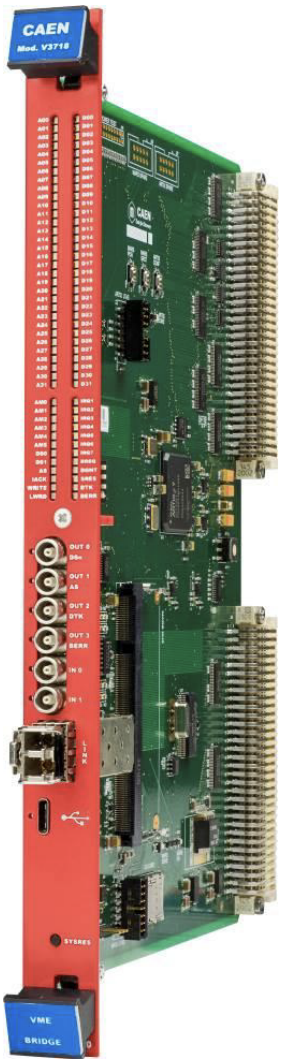
Rev.4 - August 30th 2022

PRELIMINARY

V3718 / VX3718

VME to USB 2.0 / Optical Link Bridge



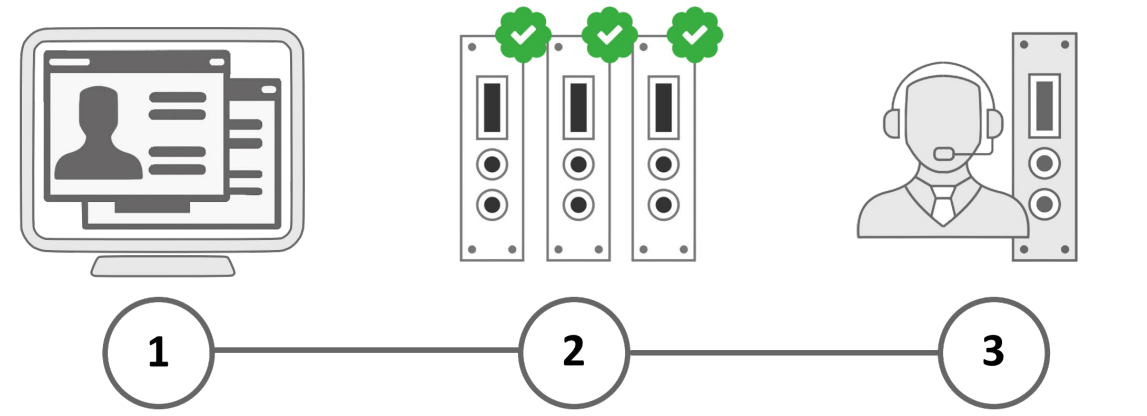
CAEN
Tools for Discovery

User Manual
UM7685

Register your device

Register your device to your **MyCAEN+** account and get access to our customer services, such as notification for new firmware or software upgrade, tracking service procedures or open a ticket for assistance. **MyCAEN+** accounts have a dedicated support service for their registered products. A set of basic information can be shared with the operator, speeding up the troubleshooting process and improving the efficiency of the support interactions.

MyCAEN+ dashboard is designed to offer you a direct access to all our after sales services. Registration is totally free, to create an account go to https://www.caen.it/become-mycaenplus-user and fill the registration form with your data.



https://www.caen.it/become-mycaenplus-user/

Purpose of this Manual

This document contains the full hardware description of the V3718/VX3718 VME-to-USB-2.0/Optical Link Bridge.

Change Document Record

Date	Revision	Changes
July 29th, 2020	00	Initial release.
June 17th, 2021	01	Added banner on the Software Support of the I/O programming. Removed chapter on Power Requirements. Updated and renamed Chap. **4** , updated Sec. **Internal Registers** and Sec. **Timer & Pulse Generator**. Added Sec. **Scaler**, Sec. **Coincidence**, Sec. **Input/output Register** and Sec. **A4818 Driver**.
July 7th, 2021	02	Removed "PRELIMINARY" following the product validation.
September 3rd, 2021	03	Updated Sec. **Firmware File**
August 30th, 2022	04	Corrected some bits in the register description

Symbols, Abbreviated Terms and Notation

n.a.

Reference Documents

[RD1] GD2512 – CAENUpgrader QuickStart Guide

[RD2] UM1934 - CAENComm User & Reference Manual

[RD3] UM1935 - CAENDigitizer User & Reference Manual

[RD4] UM7715 – CAENVMELib User & Reference Manual

[RD5] UM4413 - A2818 Technical Information Manual

[RD6] UM3121 - A3818 Technical Information Manual

[RD7] AN2472 - CONET1 to CONET2 migration

[RD8] DS7799 – A4818 Adapter Data Sheet

https://www.caen.it/support-services/documentation-area/

CAEN S.p.A.
Via Vetraia, 11 55049 Viareggio (LU) - ITALY
Tel. +39.0584.388.398 Fax +39.0584.388.959
info@caen.it
www.caen.it

Disclaimer

MADE IN ITALY: We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

Index

List of Figures

List of Tables

Safety Notices

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIRFLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: This product needs proper handling.

THIS BRIDGE DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)!
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

CAEN provides the specific document "Precautions for Handling, Storage and Installation" available in the documentation tab of the product web page that the user is mandatory to read before operating with CAEN equipment.

1 Introduction

The V3718 is CAEN VME-to-USB2.0/Optical Link Bridge implementing a VME master controlled by a PC via USB 2.0 and CONET Link (CAEN proprietary optical link protocol), including all the functions in a 1-unit wide VME 6U form factor.

The Bridge is also available in the VX3718 version with VME64X mechanics (VME64X cycles not implemented). In the present document, the "V3718" term will be used to generally refer to both versions, unless otherwise specified.

The optical link connection between the V3718 and the host PC requires a CAEN optical controller (A3818 PCI Express or the A2818 PCI card) or the A4818 CONET-to-USB3 compact adapter, and an optical fiber cable (see **Tab. 1.1**). Multi-crate sessions can be easily performed thanks to the CONET Daisy chain capability: up to eight V3718 units can be controlled by a single link of an A2818/A3818/A4818 building a CONET Optical Network.

The V3718 can perform all the cycles foreseen by the VME64 standard except those intended for 3U boards. The Bridge can operate as VME System Controller (normally when plugged in slot 1) acting as a Bus Arbiter in Multi-Master systems. The activity on the VME bus can be monitored in detail both locally (through an 88-LED DataWay Display) and remotely.

The front panel of the V3718 hosts six TTL/NIM programmable I/Os on LEMO connectors: four outputs (default assignment: DSn, AS, DTK, BERR) and two inputs. The I/Os can be programmed via USB and Optical Link to implement functions like Timer, Counter, Pulse generator, I/O register, and others (see Chap. **8**).

The supported data transfer rate is up to 30 MB/s by USB 2.0 and up to 80 MB/s by CONET2. Thanks to the 128KB memory buffer, the activity on the VME bus is not slowed down by the transfer rate on the USB port, or on the CONET one, especially when several V3718 units share the same network.

The V3718 can be integrated into the most common Windows® and Linux® computers by CAEN dedicated drivers. Middleware libraries and useful example demos are also provided. Firmware can be upgraded via USB/Optical link.

THE SOFTWARE SUPPORT OF THE FRONT PANEL I/O PROGRAMMING IS FROM THE CAENVMELib LIBRARY REV.3.3 ON

Board Models	Description
V3718	V3718 – VME to USB2/CONET Bridge
VX3718	VX3718 – VME to USB2/CONET Bridge
Related Products	**Description**
A2818	A2818 – PCI Optical Link Controller
A3818A	A3818A – PCIe 1 Optical Link Controller
A3818B	A3818B – PCIe 2 Optical Link Controller
A3818C	A3818C – PCIe 4 Optical Link Controller
A4818	A4818 - CONET to USB3 Adapter
Accessories	**Description**
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of models and related items

2 Block Diagram

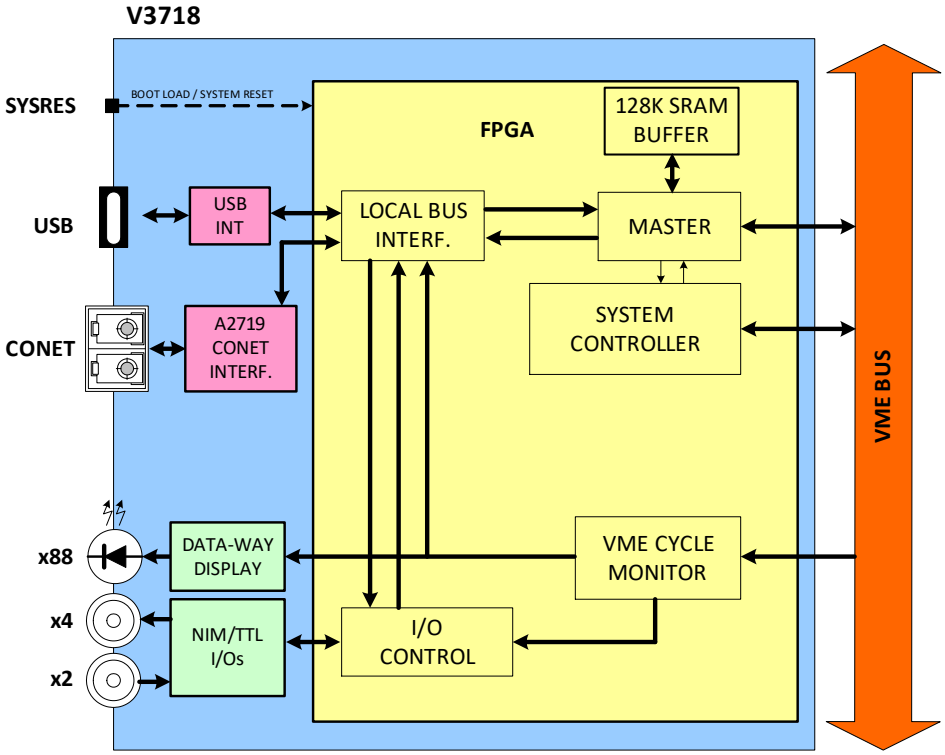


Fig. 2.1: Simplified block diagram

The FPGA represents the core of the module, implementing the USB and CONET communication protocols, handling the LED display and I/O connectors on the front side, and the VME Master on the backside.

Inside the FPGA, a 128KB buffer permits temporary data storage during VME cycles: the VME data rate is therefore decoupled from the USB and optical link rate and may take place at full speed.

3 Technical Specifications

PHYSICAL	**Form Factor** 1-unit wide VME 6U	**Weight** 315 g	
PC INTERFACE	**USB** USB-2.0 Type-C socket	**Optical Link** CONET (CAEN protocol) FSP+ connector	
TRANSFER RATE	• up to 80 MB/s with CONET2 • up to 30 MB/s with USB-2.0		
ADDRESSING	A16, A24, A32, CR/CSR, LCK; ADO, ADOH cycles		
DATA CYCLES	D08, D16, D32 for R/W and RMW; D16, D32 for BLT, D64 for MBLT		
INTERRUPT CYCLES	D08, D16, D32, IACK		
INTERRUPTS TRANSFER AND MONITOR	**Optical Link** VME interrupts IRQ[7:1] passed directly from VME to the PCIe bus via the optical link; the host system is notified asynchronously (polling not required)	**USB** VME interrupts are not directly passed to the PC; the host system has to poll IRQ[7:1] via USB	
LED DISPLAY	Data bus, address bus, address modifier, interrupt request, control signals		
PANEL I/Os	**OUT[3:0]** 4 signal outputs SW programmable functions Single-ended NIM/TTL (R_t = 50 Ω) LEMO 00 female socket	**IN[1:0]** 2 signal inputs SW programmable functions Single-ended NIM/TTL (HW programmable) Z_{in} = 50 Ω or 1 kΩ hardware selectable LEMO 00 female socket	
SOFTWARE	• Windows® and Linux® support • Drivers for the communication links (USB-2.0, CONET) • Middleware libraries C/C++ • Example demos and firmware upgrade tool		
POWER REQUIREMENTS	0.6 A @ +5V	0.050 A @ +12V	0.050 A @ -12V

Tab. 3.1: Specifications table

4 Mechanics

V3718/VX3718 are 1-unit wide 6U VME64/VME64X boards.

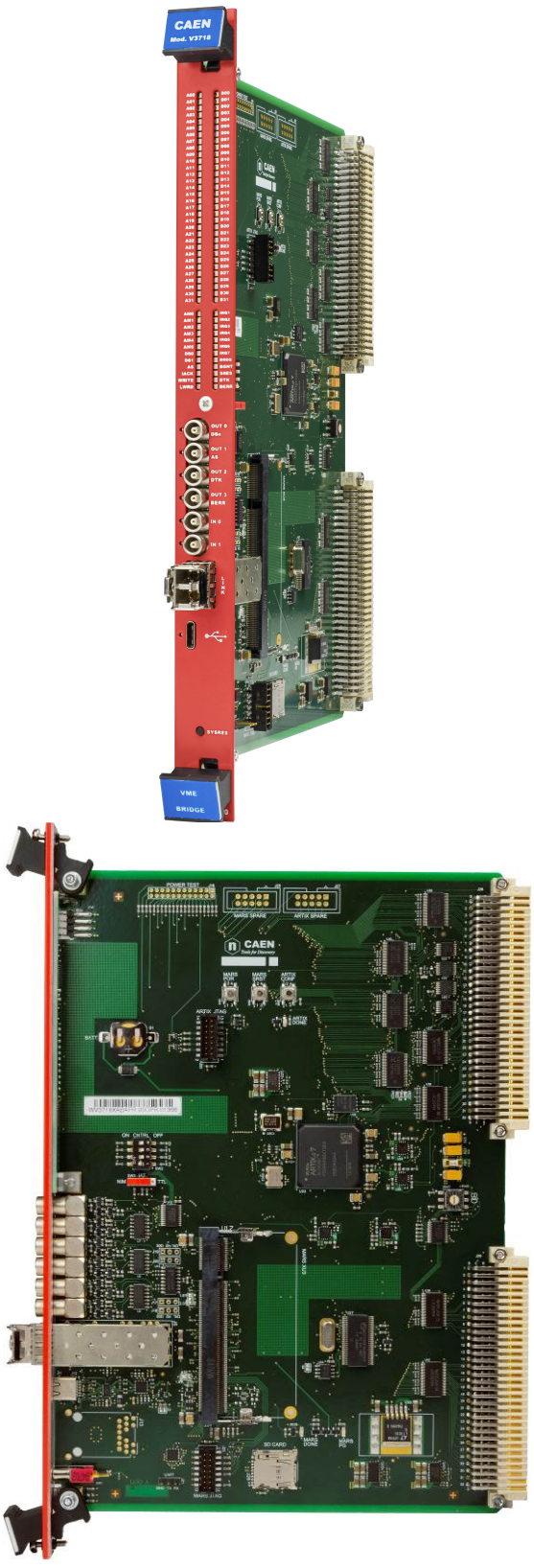


Fig. 4.1: Module view

5 Panel Description

V3718 and VX3718 share the same panel arrangement.

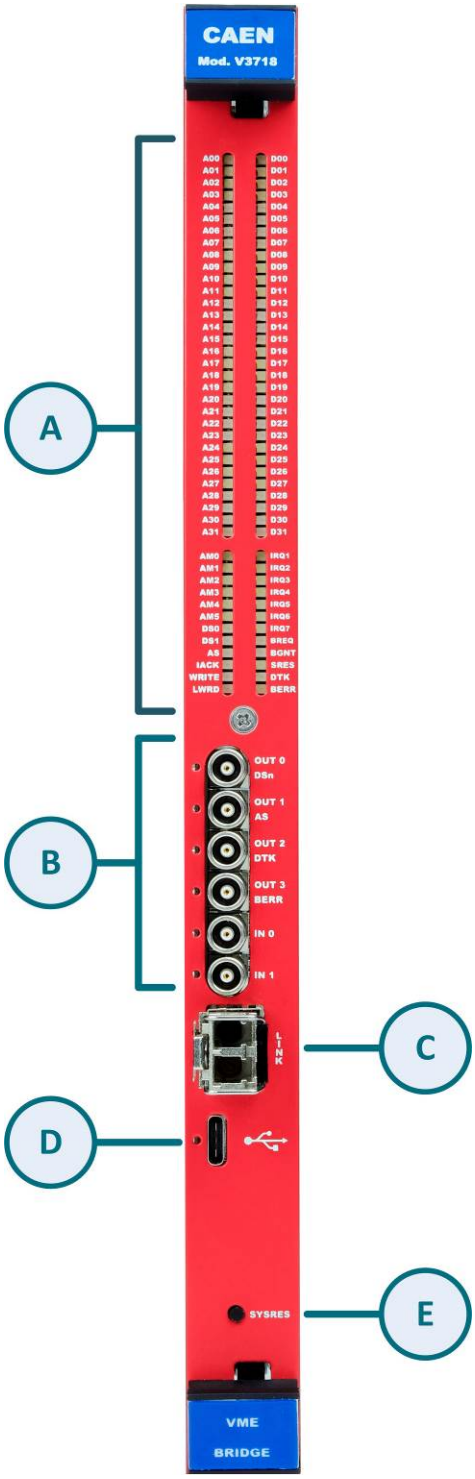


Fig. 5.1: Front panel

Front Panel

A

DATAWAY DISPLAY

FUNCTION

88-LED visual monitor of the activity on the VME bus (data bus, address bus, address modifier, interrupt request, control signals). See **Chap. 7**.

B

DIGITAL INPUTS/OUTPUTS

FUNCTION

Four outputs and two inputs, software programmable, hardware selectable NIM/TTL (see Chap. **8**). Inputs are internally terminated at 50 Ω or 1 kΩ by an on-board jumper (see Chap. **6**); outputs require 50 Ω termination.

Default signals (see also Sec. **Internal Registers**):

- OUT 0 = DSn
- OUT 1 = ASn
- OUT 2 = DTACKn
- OUT 3 = BERRn
- IN 0 = Scaler gate
- IN 1 = Scaler input

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

INDICATORS

LEDs (GREEN): when on, indicate activity on the relevant I/O channel.

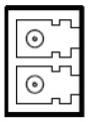
C

OPTICAL LINK PORT

FUNCTION

Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125µm cable featuring LC connectors on both sides. Can support a maximum data rate of 80 MB/s.

PINOUT



TX (red wrap)

RX (black wrap)

MECHANICAL SPECS

Series: SFF Transceivers.

Type: FTLF8519F-2KNL (LC connectors).

Manufacturer: FINISAR.

INDICATORS

LEDs (GREEN/ORANGE)**:** GREEN LED indicates the network presence, while ORANGE LED signals the data transfer activity.

D

USB PORT

FUNCTION

USB connector for data readout and flow control. Compliant to USB-1.1 and USB-2.0. Can support a maximum data rate of 30 MB/s.

MECHANICAL SPECS

Series: USB connectors.

Type: TYPE-C RECEPTACLE (632723300011).

Manufacturer: Wurth.

INDICATORS

LED (GREEN): indicates the USB communication is active.

E

SYSTEM RESET BUTTON

FUNCTION

1) System Reset: hold the SYSRES button down until the SRES LED flashes on the dataway display to perform a system reset (see Chap. **7**).
2) Boot load control: the button allows to alternatively enter the Backup mode or the Safe Mode to possibly recover from a partial or global FLASH issue (See Sec. **Troubleshooting)**

- *No action*: power on the Bridge without any action on the SYSRES button. The Bridge will boot in Standard mode and the firmware copy stored in the Standard page of the FLASH is loaded on the FPGA (standard operating).
- *Short pressure*: power on the crate holding the SYSRES button down and release the button as soon as the front panel I/O LEDs light on. The Bridge will boot in Backup mode and the firmware copy stored in the Backup page of the FLASH is loaded on the FPGA.
- *Long pressure*: like the short-pressure case but release the SYSRES button after the front panel I/O LEDs light off. The Bridge will boot in Safe Mode and the firmware copy stored in the Factory page of the FLASH is loaded on the FPGA.

6 Internal Components

Switches

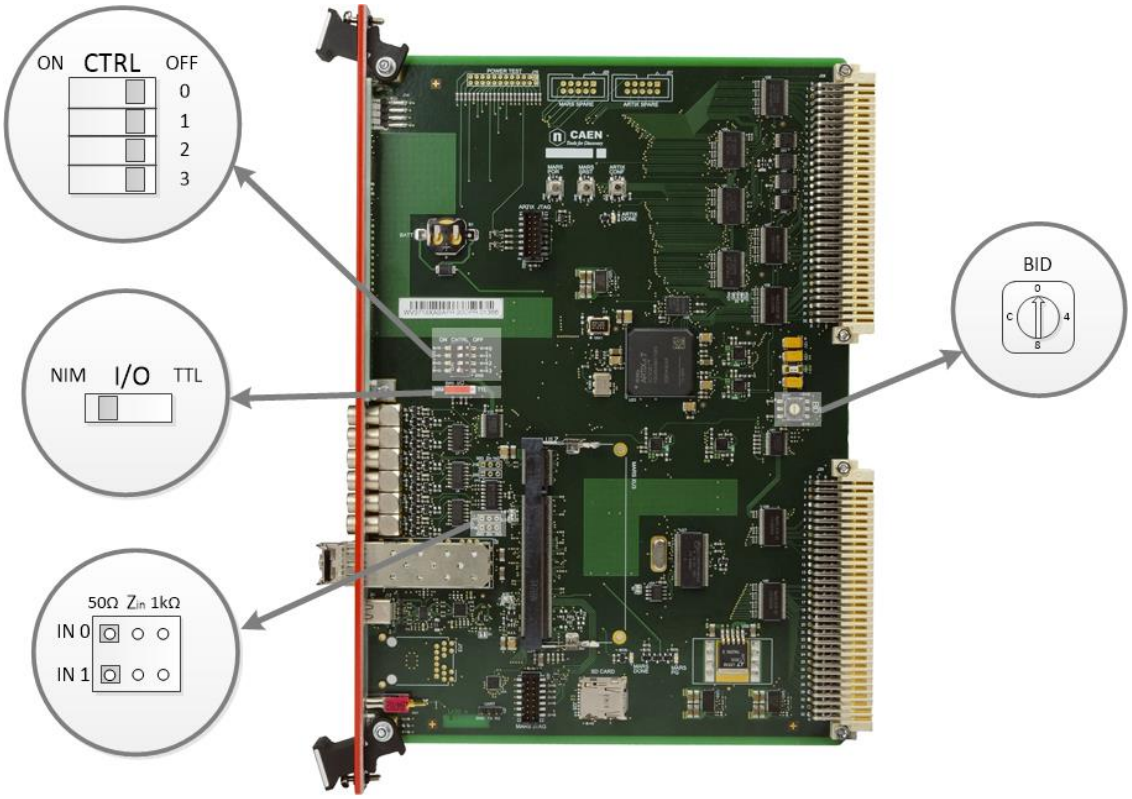


Fig. 6.1: Internal components

CTRL Dip Switches

Four selectors of VME functions; the status of each switch can be read also in the STATUS Register (see Sec. **Internal Registers**).

- **PROG[0]**: forces the System Controller to be enabled, regardless of the 1st Slot detection (ON: SYSTEM CONTROLLER enabled; OFF: don't care).
- **PROG[1]**: forces the System Controller to be disabled, regardless of the 1st Slot detection (ON: SYSTEM CONTROLLER disabled; OFF: don't care).
- **PROG[2]**: when this switch is ON, the master initiates the VME cycles without waiting for the Bus Grant from the arbiter; this setting must be used only for test purposes, since conflicts may occur when more VME masters are present (ON: requester bypassed; OFF: don't care).
- **PROG[3]**: *not used*.

NOTE: if PROG[0] is set to ON, then PROG[1] must be set to OFF and vice versa.

I/O Dip Switch

Common selector between NIM and TTL signals for the front panel I/Os (LEMO). The status of this switch can be read also in the STATUS Register (see Sec. **Internal Registers**).

INPUT Z_{in} Jumper

Selector of the input impedance for IN 0 and IN 1 front panel inputs: 50Ω default.

BID Rotary Switch

Board identifier (Board ID).

Product Identification Number (PID)

The PID is the unique CAEN product identification number composed of a prefix followed by an incremental number greater than 10000 (**Fig. 6.2**).

Fig. 6.2: PID label

The PID label is placed on the B-side of the V3718 board (**Fig. 6.3**).

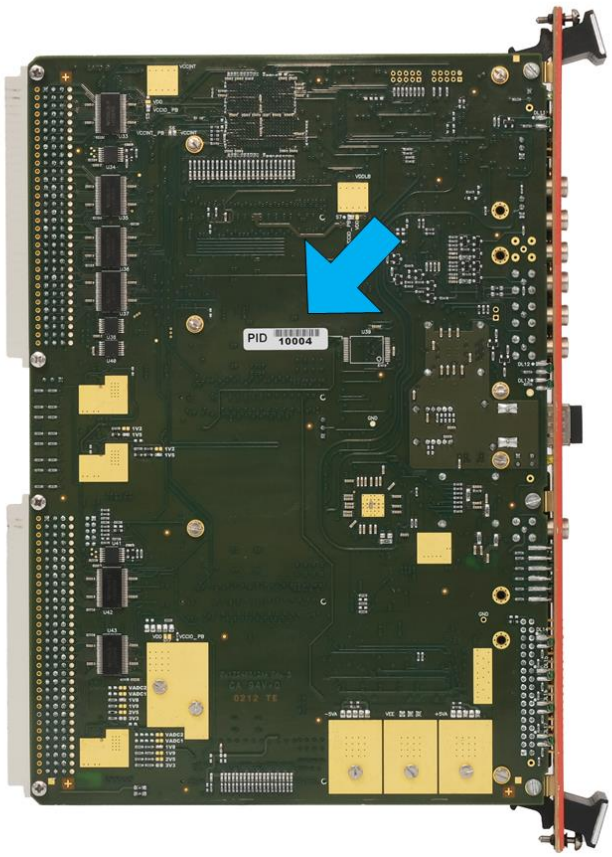


Fig. 6.3: PID location

7 VME Dataway Display

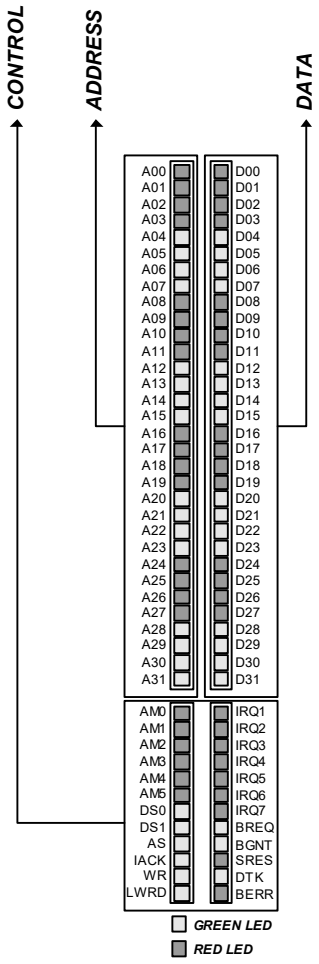


Fig. 7.1: Dataway display layout

The V3718 is provided with an 88-LED Dataway Display. The LEDs report the VME Bus status (address, data, and control lines) related to the latest cycle.

NAME	FUNCTION
A[31:0] AM[5:0] IACK WRITE LWORD	These LEDs are frozen on the AS leading edge and remain stable until the next cycle
D[31:0]	These LEDs are frozen either on the DS leading edge during the write cycles or on the DTACK (or BERR) leading edge during the read cycles; the datum remains stable until the next cycle; in case of BLT cycles, the last read datum remains visible
DS0 DS1	These LEDs turn on as the signal is active during the cycle just executed; they remain stable until the next cycle
AS	This LED flashes on the AS leading edge; it is used for signaling a cycle execution
BGR	This LED flashes as any Bus Grant line (BG[3:0]) is active
BRQ	This LED flashes as any Bus Request line (BR[3:0]) is active
SRES	This LED flashes as the SYSRES is active (see Sec. **Front Panel**)
DTK	This LED turns on if the cycle just executed was terminated with a DTACK asserted by a slave; it remains on until the next cycle
BERR	This LED turns on if the cycle just executed was terminated with a BERR; it remains on until the next cycle

Tab. 7.1: Dataway display table

8 Programmable Inputs/Outputs

As described in Chap. **5**, the V3718 houses six software programmable GPIOs on the front panel: four outputs and two inputs. The signals can be either NIM or TTL, selectable by onboard dip switch (see Chap. **6**). Six green LEDs (one per connector) light up as the relevant signal is active.

The allowed programmable functions are the topic of this chapter, while the available registers are described in Sec. **Internal Registers**.

Timer & Pulse Generator

There are two modules implemented (Pulser A and Pulser B), which work independently. Each module produces a burst of N pulses (N can be infinite, then the pulses are continuously generated) upon a start signal which can be HW from a GPIO or SW from a register. The delay from the start signal, the pulser period T, and the pulse width W are programmable. The Pulser output can be directed to a GPIO. The stop, which can be HW from a GPIO or SW from a register, will interrupt the sequence and set to zero the outputs.

A schematic view of the main parameters is shown in **Fig. 8.1**.

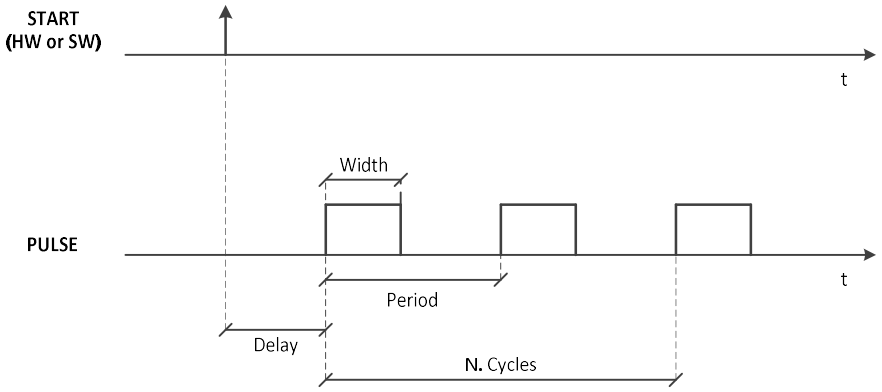


Fig. 8.1: Timer & Pulser Generator main parameters

By these modules, for example, it is possible to implement functions as:

- Clock Generator
- Burst Generator
- Monostable
- Gate and Delay Generator
- Set-Reset Flip-Flop

Scaler

There is a single scaler module implemented that can work in different modes. It allows counting a given signal in a previously set acquisition window that can be either a gate signal (Gate mode), or a preset time (D-Well Time mode), or a maximum number of hits (MaxHits mode). Whichever the mode, an analog signal can be generated on an output GPIO as soon as the end of the acquisition window is reached.

In Gate mode, the signal to count can be either an input GPIO (IN0, IN1), or a combination of the two input GPIO (coincidence signal: IN0 AND IN1; OR signal: IN0 OR IN1), or a VME signal (i.e. Data Strobe, Address Strobe, Data Acknowledge, Bus Error). The scaler counts each transition of the given signal. The gate signal can be given by an input GPIO (IN0, IN1) or a software register. At the end of the gate, the number of counts is written in a register and an internal memory.

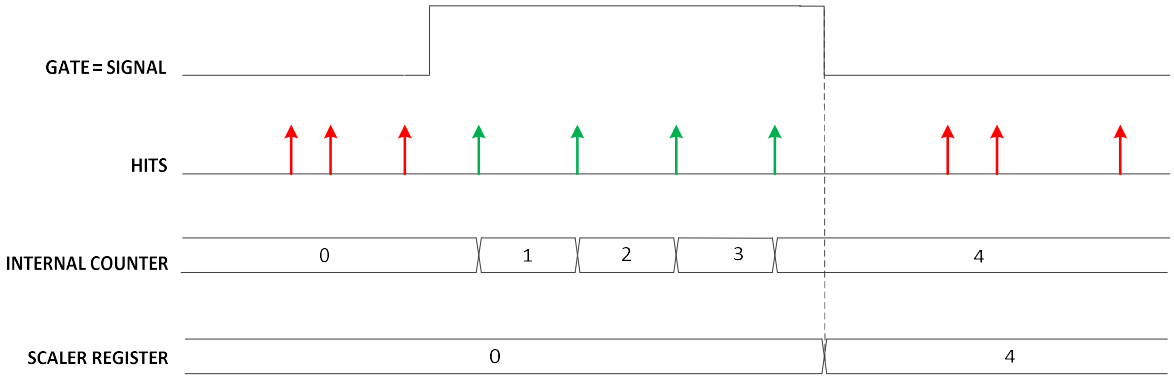


Fig. 8.2: Gate mode example. The gate is a given signal and only the hits within the gate (in green) are counted

In D-Well Time mode, an internal time gate (called D-Well Time), with a resolution of 1 ms, is applied to the scaler. At the end of the D-Well Time, the number of counts is written in a register and an internal memory.

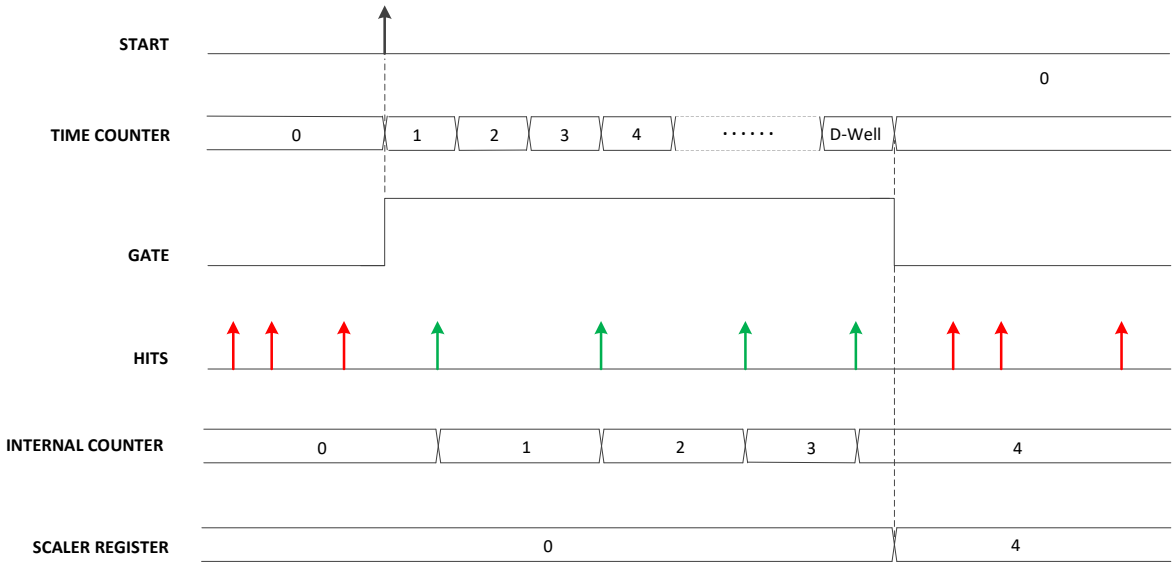


Fig. 8.3: D-Well mode example. Upon the start signal, the time counter starts counting the hits until the preset D-Well time is reached. Not counted hits are marked in red

In MaxHits mode, hits are counted until a hit number is reached.

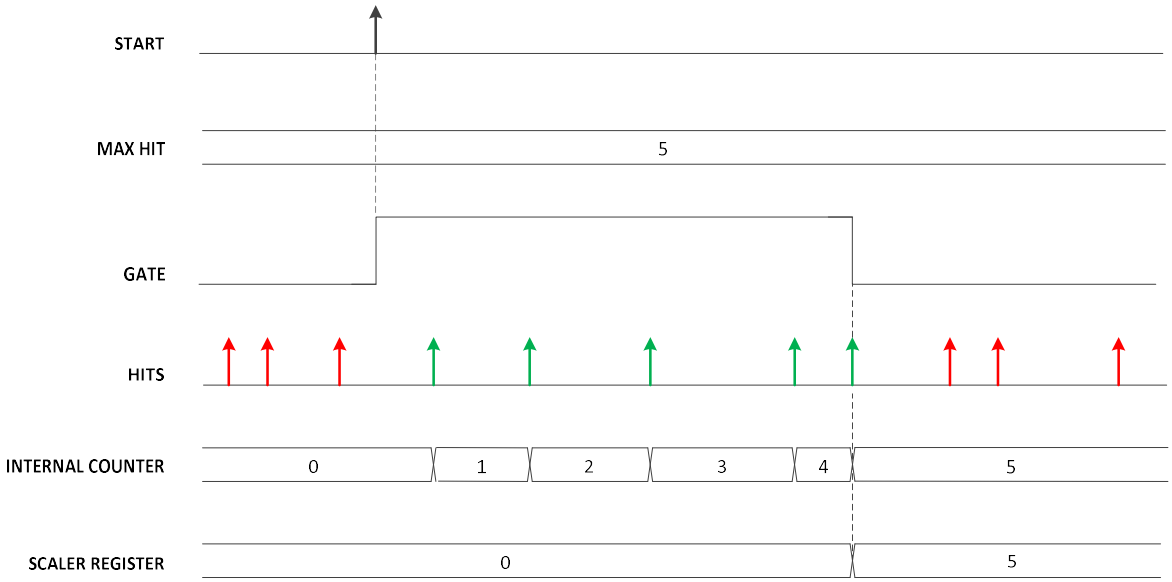


Fig. 8.4: MaxHit mode example. Upon the start signal, only a programmable maximum number of hits are counted

The Start Acquisition can be set either by an external signal (on level), or register, or front panel SYSRES button.

During the acquisition, the counter can be reset either by an external signal, or register, or front panel SYSRES button.

The run mode can be “Single Run” or “Continuous Run”. In the former case, as soon as the end of the first gate (in Gate mode), or the Dwell Time (in D-Well Time mode), or the number of hits (in MaxHits mode) is reached, the acquisition is stopped. In the latter case, the acquisition continues until the start signal is active.

Coincidence

This module makes the coincidence between two inputs. The coincidence signal is provided on the output when both the inputs are set to “1”. The output can be connected either to the input of other units or to an output GPIO.

Input/output Register

The output signals can be programmed via an Output Register, while the input signals can be monitored via an Input Register.

9 Optical Link and USB Layout

The V3718 houses a USB-2.0 compliant port with a maximum transfer rate of 30 MB/s and a Daisy chainable Optical Link (communication path which uses optical fibre cables as a physical transmission line and CONET2 serial protocol) with a maximum transfer rate of 80 MB/s.

USB

A Point-to-point direct connection between the host PC and the V3718 Bridge is supported on any USB-2.0 compatible port.

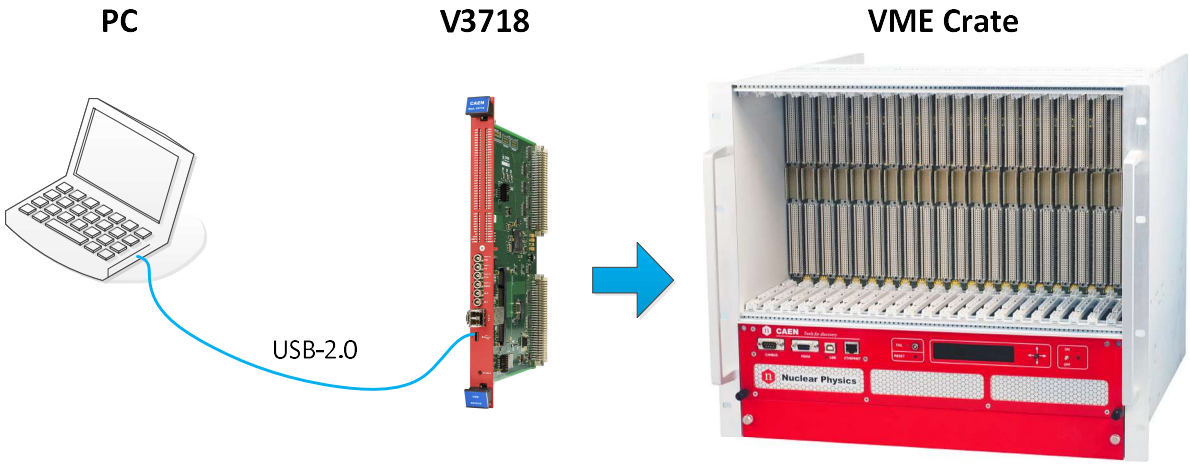


Fig. 9.1: Example of USB layout

Optical Link

The optical link connection between the V3718 Bridge and the host PC is based on CONET2 protocol and requires A2818 or A3818 CAEN Controller with a CONET2 firmware, or the A4818 Adapter board (see **Tab. 1.1**). Detailed information and documentation can be found on the CAEN website in the relevant product web page **[RD4][RD6]**.

The parameters for read/write accesses via Optical Link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc.); wrong parameter settings cause Bus Error.

Note: CONET2 is CAEN proprietary serial protocol developed to allow the optical link communication between the host PC, equipped with an A2818 or an A3818 Controller, and a CAEN CONET slave. CONET2 is 50% more efficient in the data rate transfer than the previous CONET1 version. The two protocol versions are not compliant with each other and before migrating from CONET1 to CONET2 it is recommended to read the instructions provided by CAEN in the dedicated Application Note **[RD7]**.

CONET1 IS SUPPORTED ONLY BY THE A2818 PCI CONTROLLER!

IT IS SO STRICTLY REQUIRED TU UPGRADE THE A2818 WITH A CONET2 FIRMWARE BEFORE COMMUNICATE TO THE V3718!

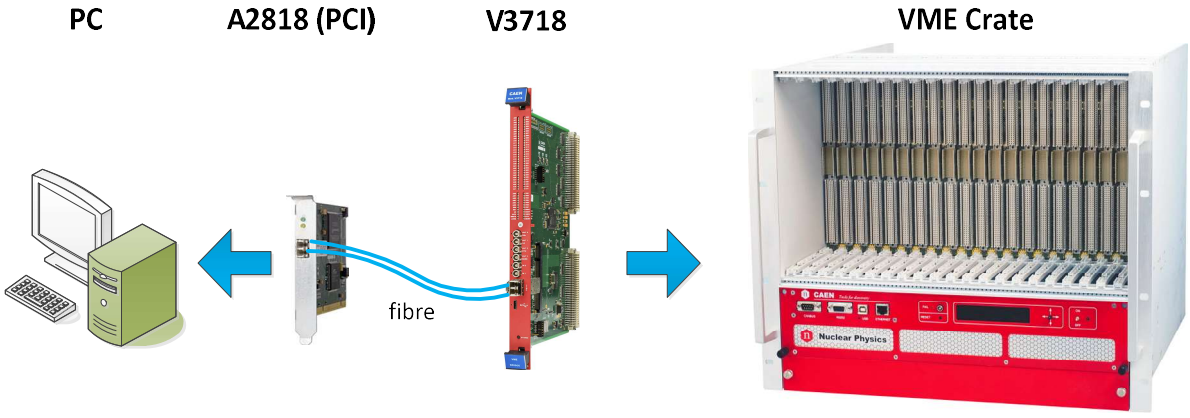


Fig. 9.2: Example of Optical Link setup through A2818 or A3818

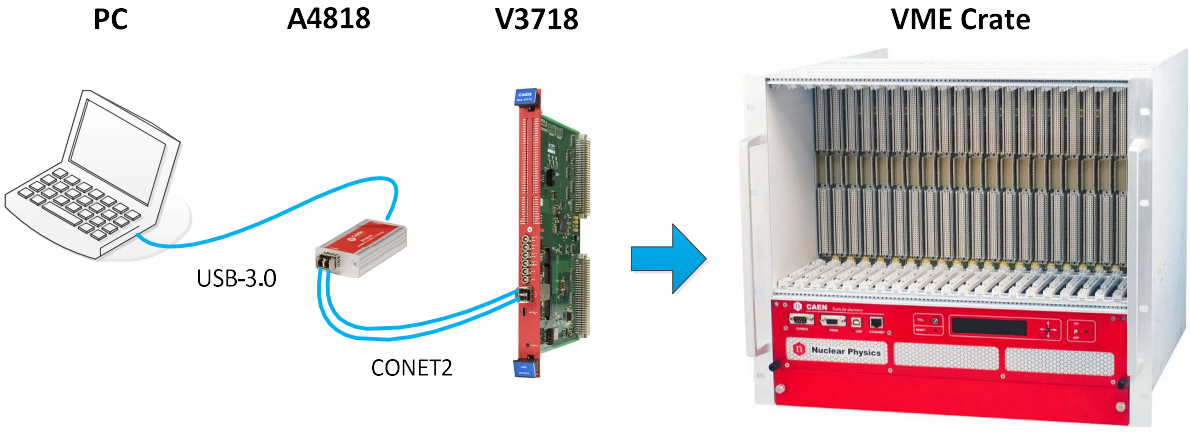


Fig. 9.3: Example of Optical Link setup through A4818

The CAEN Optical Link features Daisy chain capabilities: up to eight CONET slave nodes can be connected in Daisy chain to the link of the A2818 or A4818, and each link of a multi-link A3818 version. The A3818C (4-link) can so support up to 32 CONET slave nodes in the Daisy chain. For this purpose, various types of cables are available (**Tab. 9.1**).

Cable	Length	Connector
X-30	30 m	1 LC Duplex + 2 LC Simplex
X-20	20 m	1 LC Duplex + 2 LC Simplex
X-5	5 m	1 LC Duplex + 2 LC Simplex
I-40	40 m	2 LC Simplex
I-30	30 m	2 LC Simplex
I-20	20 m	2 LC Simplex
I-5	5 m	2 LC Simplex
I-3	30 cm	2 LC Simplex

Tab. 9.1: CONET cables specifications

If the network is composed of one A2818, A3818, or A4818, and only one V3718, then it is suggested to use X-type cables: such cables have a duplex connector on the A2818/A3818/A4818 side and two simplex connectors on the crate side; the simplex connector with the black wrap is for the RX line and the one with the red wrap is for the TX. If more than one V3718 is present, the best solution is to use the X-type cable for connecting the A2818/A3818/A4818 with the first and the last module, and the I-type for connecting intermediate modules. An example is given in **Fig. 9.4**.

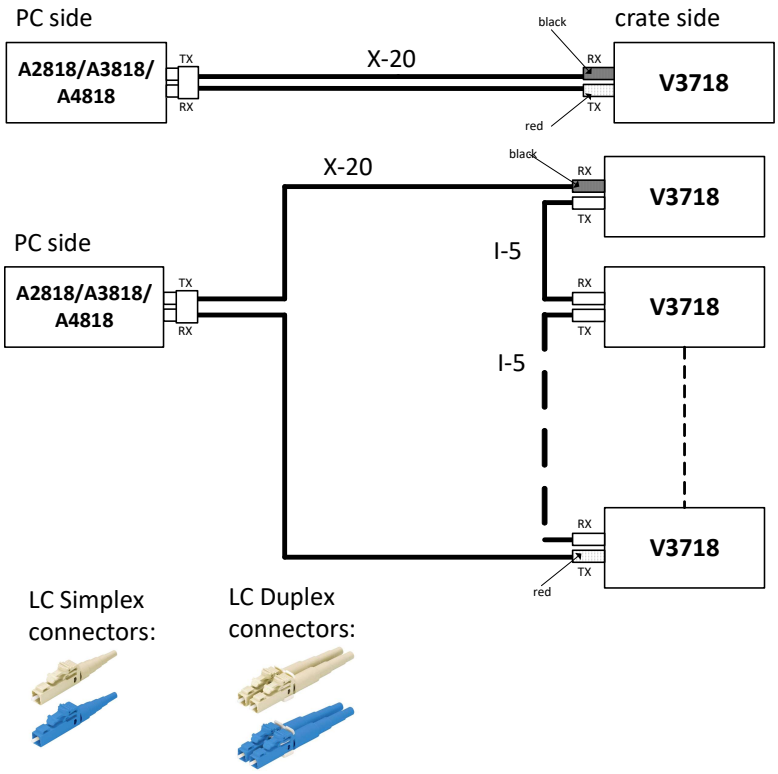


Fig. 9.4: Example of optical network

10 VME Interface

The V3718 provides all the addressing and data transfer modes documented in the VME64 specification (except A64 and those intended to improve 3U applications, like A40 and MD32). The V3718 is also compatible with all VME bus modules compliant to pre-VME64 specifications. As VME bus master, the V3718 supports Read-Modify-Write (RMW), and Address-Only-with-Handshake (ADOH) but does not accept RETRY* as termination from the VME bus slave. The ADOH cycle is used to implement the VME bus Lock command allowing the PC Host to lock VME bus resources.

VME Bus Requester

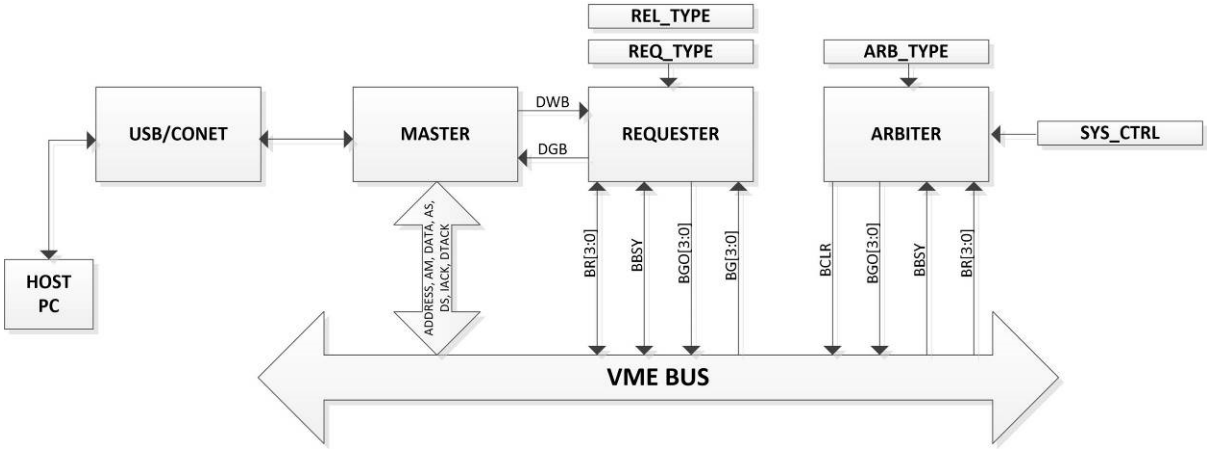


Fig. 10.1: Internal arbitration for VME bus request

When the V3718 operates as VME bus Requester, the functional sequence is following described:

- The USB/CONET sends a VME bus access request.
- The Master asserts DWB (Device Want Bus) and waits for DGB (Device Grant Bus).
- The Requester requests the bus to the Arbiter, via VME (whether the Arbiter is the V3718 itself or not); when the Arbiter has granted the bus, the Requester asserts DGB and BBSY (on the bus).
- The Master performs the VME cycle, then releases DWB.
- If REL_TYPE is RWD (Release When Done), then the Requester releases BBSY.

Fair and Demand Request Modes

The V3718 produces requests on all VME bus request levels: BR3*, BR2*, BR1*, and BR0*. The default setting is for level 3 VME bus requests. The request level is a global programming option set through the Bus Request field in the Control register (see Sec. **Internal Registers**).

The programmed request level is used by the VME bus Master Interface regardless of the channel currently accessing the VME bus Master Interface.

The Requester may be programmed for either Fair or Demand mode. The request mode is a global programming option set through the Requester Type bit in the Control register.

In Fair mode, the V3718 does not request the VME bus until no other VME bus requests are pending at its programmed level. This mode ensures that every requester on an equal level has access to the bus.

In Demand mode, the requester asserts its bus request regardless of the state of the BRn* line. By requesting the bus frequently, requesters far down the daisy chain may be prevented from ever obtaining bus ownership. This is referred to as “starving” those requesters. Note that, to achieve fairness, all bus requesters in a VME bus system must be set to Fair mode.

VME Bus Release

The Requester can be configured as either RWD (release when done) or ROR (release on request) using the Release Type bit in the Control register (see Sec. **Internal Registers**). The default setting is for RWD: the bus is released as soon as the VME access is terminated; in the case of BLT/MBLT cycles, the access is terminated either when the N required bytes are transferred (although the cycle is divided into several blocks according to the VME boundaries) or when BERR* is asserted. ROR means the master releases BBSY* only if a bus request is pending from another VME bus master and once the channel that is the current owner of the VME bus Master Interface is done. Ownership of the bus may be assumed by another channel without re-arbitration on the bus if there are no pending requests on any level on the VME bus.

Addressing Capabilities

The V3718 generates A16, A24, A32, CR/CSR, and LCK address phases on the VME bus. Address Modifiers of any kind (supervisor/non-privileged and program/data) are also programmed through USB or CONET: the V3718 does not handle the AM; the HOST PC passes them via USB as VME cycle parameters. The AM broadcasting depends on the PC drivers.

The master generates ADdress-Only-with-Handshake (ADOH) cycles in support of lock commands for A16, A24, and A32 spaces.

Supported addressing:

A16, A24, A32, CR/CSR	for R/W, RMW, ADO and ADOH
A16, A24, A32	for BLT
A16, A24, A32	for MBLT
ADO	Address Only
ADOH	Address Only with Handshake

Data Transfer Capabilities

The V3718 supports the following cycles:

Cycle Type

R/W	Single Read/Write
RMW	Read Modify Write
BLT	Block Transfer
MBLT	Multiplexed Block Transfer

Data sizing

D08(EO), D16, D32	for R/W, RMW, BLT
D64	for MBLT

- BLT/MBLT cycles may be performed with either address increment or with fixed address (FIFO mode)
- BLT/MBLT cycles are split at hardware level when the boundary (BLT = Nx256 bytes; MBLT = Nx2 Kbytes) is met: AS is released and then re-asserted, the VME bus is not re-arbitered. The boundaries are neglected in FIFO operating mode.
- Non-aligned accesses are not supported

It is then possible to perform data cycles (single and BLT) with hardware byte swapping. The “Swapped” cycles are called: D16_swapped, D32_swapped, and D64_swapped. Such cycles will return “swapped” data, in the following way:

D16_swapped: Byte0 ↔ Byte1, Byte1 ↔ Byte0

D32_swapped: Byte0 ↔ Byte3, Byte1 ↔ Byte2, Byte2 ↔ Byte1, Byte3 ↔ Byte0

D32_swapped: Byte0 ↔ Byte7, Byte1 ↔ Byte6, Byte2 ↔ Byte5, Byte3 ↔ Byte4, Byte4 ↔ Byte3, Byte5 ↔ Byte2, Byte6 ↔ Byte1, Byte7 ↔ Byte0

Interrupt Capabilities

USB Link

The USB does not allow transferring an interrupt to the PC, so the communication between the PC and the V3718 is always started by the PC. The VME interrupts are activated by reading the IRQ lines status from the PC and, if one line is active, then an IACK cycle can be executed.

The V3718 supports the following IACK cycles:

IACK: D08, D16, D32

OPTICAL Link

The VME Bus interrupts are transferred to the PCI/PCIe BUS through the CONET. The interrupt latency (i.e. the interval between the interrupt appearance on the VME bus and the time the interrupt is activated on the PCI bus) is always shorter than 5 µs.

The V3718 supports the following IACK cycles:

IACK: D08, D16, D32

The VME Bus Interrupts can be individually masked for each V3718 in the chain.

The CAENVMLib library (see **Chap.12**) makes available specific functions like the first-to-be-used *IRQEnable()* which enables the generation of PCI bus interrupts following VME bus interrupts, and the *IRQWait()* that must be then called to wait for the interrupt. When the *IRQWait()* returns, the VME bus interrupts are disabled, so an IACK can be performed to obtain the vector and, for RORA interrupts, the access to the interrupter must be performed to stop the interrupt generation. If it is necessary to receive other VME bus interrupts, the IRQEnable must be called again. Find detailed descriptions in the library documentation**[RD4]**.

Cycle Terminations

The V3718 accepts BERR* or DTACK* as cycle terminations. BERR* is handled as cycle termination whether it is produced by the V3718 itself or by another board. The Status word broadcasted as the cycle is acknowledged, informs the HOST PC about the cycle termination type (BERR* or DTACK*).

VME Bus First Slot Detector

The First Slot Detector module samples BG3IN* immediately after reset to determine whether the V3718 resides in slot 1. The VME bus specification requires the BG[3:0]* lines to be driven high during reset. This means that, if a board is preceded by another board in the VME bus system, it will always sample BG3IN* high after reset. BG3IN* can only be sampled low after reset by the first board in the crate (there is no preceding board to drive BG3IN* high). If BG3IN* is sampled at logic low immediately after reset (due to the master internal pull-down), then the V3718 is in slot 1 and becomes SYSTEM CONTROLLER; otherwise, the SYSTEM CONTROLLER module is disabled. This mechanism may be overridden via dip switch setting: the SYSTEM CONTROLLER bit is “forced” to one by setting to ON PROG_0, and is “forced” to zero by setting to ON PROG_1; note that such switches must always be in “opposite” positions (see Chap. **6**).

System Controller Functions

When located in Slot 1 of the VME crate, the V3718 assumes the role of SYSTEM CONTROLLER and sets the SYSTEM CONTROLLER status bit in the STATUS register (see Sec. **Internal Registers**). Following the VME64 specification, as SYSTEM CONTROLLER the V3718 provides:

- a system clock driver
- an arbitration module
- an IACK Daisy Chain Driver (DCD)
- a bus timer

System Clock Driver

The V3718 provides a 16MHz SYSCLK signal when configured as a SYSTEM CONTROLLER.

Arbitration Module

When the V3718 is SYSTEM CONTROLLER, the Arbitration Module is enabled. The Arbitration Module supports the following arbitration modes:

- Fixed Priority Arbitration Mode (PRI),
- Round Robin Arbitration Mode (RRS) (default setting).

These modes can be set in the CONTROL register (see Sec. **Internal Registers**).

In the Fixed Priority Arbitration Mode (PRI), the order of priority is BR[3], BR[2], BR[1], and BR[0] as defined by the VME64 specification. The Arbitration Module issues a Bus Grant (BGO[3:0]) to the highest requesting level. If a Bus Request of higher priority than the current bus owner becomes asserted, the Arbitration Module asserts BCLR until the owner releases the bus (BBSY is negated).

Round Robin Arbitration Mode (RRS) arbitrates all levels in a round-robin mode, repeatedly scanning from levels 3 to 0. Only one grant is issued per level and one owner is never forced from the bus in favour of another requester (BCLR is never asserted). Since only one grant is issued per level on each round-robin cycle, several scans will be required to service a queue of requests at one level.

Bus Timer

A programmable bus timer allows users to select a VME bus time-out period. The time-out period is configurable as 50 µs or 400 µs through the Bus Timeout bit in the Control register (see Sec. **Internal Registers**). The VME bus Timer module asserts BERR if a VME bus transaction times out (indicated by one of the VME bus data strobes remaining asserted beyond the time-out period).

IACK Daisy Chain Driver

The V3718 can operate as IACK Daisy Chain Driver: it drives low the IACKOUT line of the first slot, thus starting the chain propagation, as soon as it detects an Interrupt Acknowledge cycle by an Interrupt Handler (that could be the V3718 itself).

VME64X Cycles

The VME64X cycles are not implemented in this board.

Internal Registers

NAME	ADDRESS	TYPE	Nbit	FUNCTION
STATUS	0x00	read	16	Status register
CONTROL	0x01	read/write	16	VME control register
FIRMWARE_REVISION	0x02	read	16	FW revision register
IRQ_STATUS	0x05	read	16	IRQ status register
IRQ_MASK	0x06	read/write	16	IRQ mask register
IO_LEVEL	0x07	Read/write	16	I/O level set register
IO_POLARITY	0x08	read/write	16	I/O polarity register
OUT_2_0_MUX_SET	0x09	read/write	16	OUT[2:0] Multiplexer set register
OUT3_MUX_SET	0x0A	read/write	16	OUT[3], IN[1:0] Multiplexer set register
IO_STATUS_READ	0x0B	read/write	16	I/O status read register
IO_STATUS_SET	0x0C	read/write	16	I/O status set register
IO_COINC	0x0D	read/write	16	I/O coincidence mask register
PULSE_A_SETUP	0x10	read/write	16	Pulser A source register
PULSE_A_START	0x11	read/write	16	Pulser A start register
PULSE_A_CLEAR_(STOP)	0x12	read/write	16	Pulser A clear (stop) register
PULSE_A_NCYCLE	0x13	read/write	16	Pulser A n cycles register
PULSE_A_WIDTH	0x14	read/write	16	Pulser A width register
PULSE_A_DELAY	0x15	read/write	16	Pulser A dealy register
PULSE_A_PERIOD	0x16	read/write	16	Pulser A period register
PULSE_B_SETUP	0x17	read/write	16	Pulser B source register
PULSE_B_START	0x18	read/write	16	Pulser B start register
PULSE_B_CLEAR_(STOP)	0x19	read/write	16	Pulser B clear (stop) register
PULSE_B_NCYCLE	0x1A	read/write	16	Pulser B n cycles register
PULSE_B_WIDTH	0x1B	read/write	16	Pulser B width register
PULSE_B_DELAY	0x1C	read/write	16	Pulser B dealy register
PULSE_B_PERIOD	0x1D	read/write	16	Pulser B period register
DISPLAY_ADDRESS_LOW	0x20	read	16	Display AD[15:0] register
DISPLAY_ADDRESS_HIGH	0x21	read	16	Display AD[31:16] register
DISPLAY_DATA_LOW	0x22	read	16	Display DT[15:0] register
DISPLAY_DATA_HIGH	0x23	read	16	Display DT[31:16] register
SCALER_SETUP	0x2D	read/write	16	Scaler source register
SCALER_MAXHITS	0x2E	read/write	16	Scaler end counter register
SCALER_DWELL_TIME	0x2F	read/write	16	Scaler dwell time register
SCALER_SW_SETTING	0x30	read/write	16	Scaler gate and reset signal register
SCALER_INST_OUT	0x31	read/write	16	Scaler instantaneous out register
SCALER_FIFO_OUT	0x32	read/write	16	*To be implemented*

Fig. 10.2: Register map

THE SOFTWARE SUPPORT OF THE FRONT PANEL I/O PROGRAMMING IS FROM THE CAENVMELib LIBRARY REV.3.3 ON

STATUS Register

This register contains information on the status of the module.

Bit	Description
[0]	SYSTEM RESET: 0 = Inactive 1 = Active
[1]	SYSTEM CONTROL: 0 = Disabled 1 = Enable
[3:2]	*reserved*
[4]	DTACK: 1 = Last cycle terminated with DTACK 0 = Any other case
[5]	BERR: 1 = Last cycle terminated with BERR 0 = Any other case
[7:6]	*reserved*
[8]	Status of Dip Switch 0: 0 = Switch set to OFF 1 = Switch set to ON
[9]	Status of Dip Switch 1: 0 = Switch set to OFF 1 = Switch set to ON
[10]	Status of Dip Switch 2: 0 = Switch set to OFF 1 = Switch set to ON
[11]	Status of Dip Switch 3: 0 = Switch set to OFF 1 = Switch set to ON
[12]	*reserved*
[13]	NIM/TTL STATUS: 0 =NIM 1 = TTL
[15:14]	*reserved*

CONTROL Register

This register allows performing some general settings of the module.

Bit	Description
[0]	*reserved*
[1]	ARBITER TYPE: 0 = Fixed Priority 1= Round Robin
[2]	REQUESTER TYPE: 0 = Fair 1 = Demand
[3]	RELEASE TYPE: 0 = Release When Done (RWD) 1 = Release On Request (ROR)
[5:4]	BUS REQUEST LEVEL
[6]	INTERRUPT REQUEST
[7]	SYSTEM RESET (SysRes)
[8]	BUS TIMEOUT: 0 = 50 µs 1 = 400 µs
[9]	ADDRESS INCREMENT DURING BLT: 0 = enabled 1 = disabled (FIFO mode)
[10]	SINGLE CYCLE SEQUENCE
[15:11]	*reserved*

FIRMWARE REVISION Register

This register contains the firmware revision number coded over 16 bits as X.Y.

Bit	Description
[7:0]	MINOR REVISION NUMBER (Y)
[15:8]	MAJOR REVISION NUMBER (X)

IRQ STATUS Register

This register monitors the status of the IRQ lines.

Bit	Description
[0]	IRQ LINE 1: 0 = inactive 1 = active
[1]	IRQ LINE 2: 0 = inactive 1 = active
[2]	IRQ LINE 3: 0 = inactive 1 = active
[3]	IRQ LINE 4: 0 = inactive 1 = active
[4]	IRQ LINE 5: 0 = inactive 1 = active
[5]	IRQ LINE 6: 0 = inactive 1 = active
[6]	IRQ LINE 7: 0 = inactive 1 = active
[15:7]	*reserved*

IRQ MASK Register

This register sets the IRQ mask.

Bit	Description
[6:0]	IRQ LINE [6:0]
[15:7]	*reserved*

I/O LEVEL SET Register

This register allows setting the TTL/NIM level for the I/O front panel signals.

Bit	Description
[1:0]	*reserved*
[2]	*reserved* (must be 1)
[3]	*reserved* (must be 1)
[4]	*reserved* (must be 0)
[5]	*reserved* (must be 0)
[6]	HW/SW Level selection: 0 = selection is HW (see Chap. **6**) 1 = selection is SW (*default*)
[7]	Level selection: 0 = NIM (*default*) 1 = TTL
[15:8]	*reserved*

I/O POLARITY Register

This register allows inverting the polarity of the front panel I/O signals. Direct means the original polarity, which could be active low or active high. Inverting an active-low I/O then means to set it active high, and vice versa.

Bit	Description
[0]	OUT0 polarity: 0 = direct (*default*) 1 = inverted
[1]	OUT1 polarity: 0 = direct (*default*) 1 = inverted
[2]	OUT2 polarity: 0 = direct (*default*) 1 = inverted
[3]	OUT3 polarity: 0 = direct (*default*) 1 = inverted
[4]	IN0 polarity: 0 = direct (*default*) 1 = inverted
[5]	IN1 polarity: 0 = direct (*default*) 1 = inverted
[15:6]	*reserved*

OUT [2:0] MULTIPLEXER SET Register

This register allows to set the function for OUT0, OUT1, and OUT2 front panel I/Os.

Bit	Description
[3:0]	OUT0 function: 0000 = Data Strobe signal (*default*) 0001 = Address Strobe signal 0010 = Data Acknowledge signal 0011 = Bus Error signal 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved* (OUT0 is set at 0)
[7:4]	OUT1 function: 0000 = Data Strobe signal 0001 = Address Strobe signal (*default*) 0010 = Data Acknowledge signal 0011 = Bus Error signal 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved* (OUT1 is set at 0)
[11:8]	OUT2 function: 0000 = Data Strobe signal 0001 = Address Strobe signal 0010 = Data Acknowledge signal (*default*) 0011 = Bus Error signal 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved* (OUT2 is set at 0)
[15:12]	*reserved*

OUT [3] MULTIPLEXER Register

This register allows to set the function for OUT2, OUT3, IN0 and IN1 front panel I/Os.

Bit	Description
[3:0]	OUT3 function: 0000 = Data Strobe signal 0001 = Address Strobe signal 0010 = Data Acknowledge signal 0011 = Bus Error signal (*default*) 0100 = Coincidence signal 0101 = Pulser A Output 0110 = Pulser B Output 0111 = Counter End Gate signal 1000 = Location Monitor signal 1001 = Register Set Status value 1010 = Device Grant VME bus signal Others = *reserved*
[15:4]	*reserved*

I/O STATUS READ Register

This register allows to read the instantaneous status of the front panel I/Os.

Bit	Description
[0]	OUT0 Status
[1]	OUT1 Status
[2]	OUT2 Status
[3]	OUT3 Status
[4]	IN0 Status
[5]	IN1 Status
[15:6]	*reserved*

I/O STATUS SET Register

This register allows setting the value of the front panel I/Os. To be effective, the I/O function must be set correctly first (see Sec. **OUT [2:0] MULTIPLEXER SET Register** and Sec. **OUT [3] MULTIPLEXER Register**).

Bit	Description
[0]	OUT0 Set
[1]	OUT1 Set
[2]	OUT2 Set
[3]	OUT3 Set
[15:4]	*reserved*

I/O COINCIDENCE Register

This register allows setting the mask for the coincidence mode.

Bit	Description
[1:0]	*reserved*
[2]	IN0: 0 = not in coincidence 1 = participates in coincidence
[3]	IN1 0 = not in coincidence 1 = participates in coincidence
[15:4]	*reserved*

PULSE A SETUP Register

This register allows setting the Pulser A sources for the start signal and the clear signal. The clear signal allows restarting the pulse train from the beginning.

Bit	Description
[0]	Start signal source: 0 = SW (*default*) 1 = HW
[1]	Clear signal source: 0 = SW (*default*) 1 = HW
[15:2]	*reserved*

PULSE A START Register

This register allows to physically start Pulser A.

Bit	Description
[0]	SW start signal: 0 = not issued (*default*) 1 = issued
[3:1]	HW start signal: 010 = IN 0 011 = IN 1 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE A CLEAR Register

This register allows to physically clear Pulser A. This means resetting the counter and waiting for a 0 to 1 transition of the start command. In the case of start source by SW, it must be set at 0 and then to 1 again.

Bit	Description
[0]	SW clear signal 0 = not issued (*default*) 1 = issued
[3:1]	HW clear sources: 010 = IN 0 (set as input) 011 = IN 1 (set as input) 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE A N CYCLE Register

This register allows to set the number of pulses and the resolution for Pulser A. Default register value is 0x0000.

Bit	Description
[14:0]	Number of pulses
[15]	Clock resolution: 0 = 25 ns 1 = 25 µs

PULSE A WIDTH Register

This register allows setting the width of the pulse for Pulser A with the clock resolution set by bit[15] of **PULSE A N CYCLE Register**.

Bit	Description
[15:0]	Pulse width

PULSE A DELAY Register

This register allows setting the delay of the pulse for Pulser A with the clock resolution set by bit[15] of **PULSE A N CYCLE Register**.

Bit	Description
[15:0]	Pulse delay

PULSE A PERIOD Register

This register allows setting the period of the pulse with the clock resolution set by bit[15] of **PULSE A N CYCLE Register**.

Bit	Description
[15:0]	Pulse period

PULSE B SETUP Register

This register allows setting the Pulser B sources for the start signal and the clear signal. The clear signal allows restarting the pulse train from the beginning.

Bit	Description
[0]	Start signal source: 0 = SW (*default*) 1 = HW
[1]	Clear signal source: 0 = SW (*default*) 1 = HW
[15:2]	*reserved*

PULSE B START Register

This register allows to physically start Pulser B.

Bit	Description
[0]	SW start signal: 0 = not issued 1 = issued (*default*)
[3:1]	HW start signal: 010 = IN 0 011 = IN 1 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE B CLEAR Register

This register allows to physically clear Pulser B. This means resetting the counter and waiting for a 0 to 1 transition of the start command. In the case of start source by SW, it must be set at 0 and then to 1 again.

Bit	Description
[0]	SW clear signal is issued
[3:1]	HW clear sources: 010 = IN 0 (set as input) 011 = IN 1 (set as input) 100 = coincidence Others = *reserved*
[15:4]	*reserved*

PULSE B N CYCLE Register

This register allows setting the number of pulses and the resolution for Pulser B.

Bit	Description
[14:0]	Number of pulses
[15]	Clock resolution: 0 = 25 ns 1 = 25 µs

PULSE B WIDTH Register

This register allows setting the width of the pulse for Pulser B with the clock resolution set by bit[15] of the **PULSE B N CYCLE Register**.

Bit	Description
[15:0]	Pulse width value

PULSE B DELAY Register

This register allows setting the delay of the pulse for Pulser B with the clock resolution set by bit[15] of the **PULSE B N CYCLE Register**.

Bit	Description
[15:0]	Pulse delay value

PULSE B PERIOD Register

This register allows setting the period of the pulse with the clock resolution set by bit[15] of the **PULSE B N CYCLE Register**.

Bit	Description
[15:0]	Pulse period value

SCALER SETUP Register

This register allows to set the source of the Scaler input, gate and reset.

Bit	Description
[3:0]	Scaler Input-Source setting: 0000 = *reserved* (do not use) 0001 = *reserved* (do not use) 0010 = IN 0 signal 0011 = IN 1 signal (*default*) 0100 = VME Data Strobe signal 0101 = VME Address Strobe 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1010 = Coincidence signal of IN0/IN1 1011 = N0 OR IN1 signal Others = *reserved*
[7:4]	Scaler Gate-Source Setting: 0000 = *reserved* (do not use) 0001 = *reserved* (do not use) 0010 = IN 0 signal (*default*) 0011 = IN 1 signal 0100 = VME Data Strobe signal 0101 = VME Address Strobe signal 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1000 = **SCALER SW SETTINGS Register** 1001 = Front panel SYSRES button (short pressure < 1.5s) 1010 = Coincidence signal of IN0/IN1 1011 = IN0 OR IN1 signal Others = *reserved*
[11:8]	Scaler Counter Reset: 0000 = *reserved* (do not use) 0001 = *reserved* (do not use) 0010 = IN 0 signal 0011 = IN 1 signal 0100 = VME Data Strobe signal 0101 = VME Address Strobe signal 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1000 = **SCALER SW SETTINGS Register** (*default*) 1001 = Front panel SYSRES button (short pressure < 1.5s) 1010 = Coincidence signal of IN0/IN1 1011 = IN0 OR IN1 signal Others = *reserved*

[15:12]	Scaler Start Source: 0000 = reserved (do not use) 0001 = reserved (do not use) 0010 = IN 0 signal 0011 = IN 1 signal 0100 = VME Data Strobe signal 0101 = VME Address Strobe signal 0110 = VME Data Acknowledge signal 0111 = VME Bus Error signal 1000 = **SCALER SW SETTINGS Register** (*default*) 1001 = Front panel SYSRES button (short pressure < 1.5s) 1010 = Coincidence signal of IN0/IN1 1011 = IN0 OR IN1 signal Others = *reserved*

SCALER MAXHITS Register

This register allows setting the number of events to stop the counter. As soon as the number of hits reaches the register value, the Scaler is stopped.

Bit	Description
[15:0]	Max hits value

SCALER DWELL TIME Register

This register allows setting the time interval (in ms) to store hits. As soon as the time interval is reached, the counter is sent out to the Instantaneous out and the FIFO out, and a new counter is set to store new data.

Bit	Description
[15:0]	D-Well time value

SCALER SW SETTINGS Register

This register manages to set the gate, reset Scaler signals, and start the acquisition.

Bit	Description
[0]	Scaler SW gate (gate is opened by software)
[1]	Scaler SW reset (counters are reset by software)
[2]	Scaler SW Start (the start count is given by software)
[3]	Run mode: 0 = Continuous run (*default*) 1 = Single run

SCALER INSTANTANEOUS OUT Register

This register allows reading only the last output data of the Scaler (if not read, values are lost).

Bit	Description
[15:0]	Scaler data

SCALER FIFO OUT Register

This register allows reading the output data of the Scaler stored in a time interval (if not read, values are lost).

Bit	Description
[15:0]	Scaler data

DISPLAY ADDRESS LOW Register

This register monitors the Address bit[15:0] section of the front panel LED Display.

Bit	Description
[15:0]	DISP_AD[15:0]

DISPLAY ADDRESS HIGH Register

This register monitors the Address bit[31:16] section of the front panel LED Display.

Bit	Description
[15:0]	DISP_AD[31:16]

DISPLAY DATA LOW Register

This register monitors the Data bit[15:0] section of the front panel LED Display.

Bit	Description
[15:0]	DISP_DATA[15:0]

DISPLAY DATA HIGH Register

This register monitors the Data bit[31:16] section of the front panel LED Display.

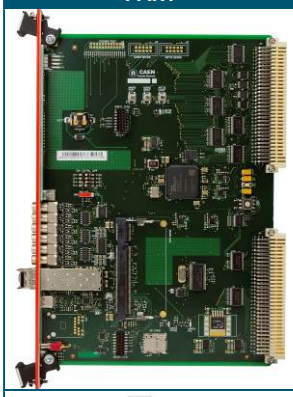
Bit	Description
[15:0]	DISP_DATA[31:16]

11 Hardware Installation

Delivered Kit

The V3718 is inspected by CAEN before the shipment, and it is guaranteed to leave the factory free of mechanical or electrical defects. When receiving the unit, the user is strictly recommended to inspect for any damage which may have occurred during transportation. Particularly, inspect for exterior damages like broken knobs or connectors and check that the panels are not scratched or cracked. All packing material should be held on until the inspection has been completed. If damage is detected, the user must file a claim with the carrier immediately and notify CAEN.

Before installing the unit, make sure to read thoroughly the safety rules and installation requirements (see Sec. **Safety Notices**), then place the package content onto your bench. The content should consist of the parts listed below.

PART	DESCRIPTION
	V3718 module
	Hi-Speed Type A-to-Type C USB-2.0 Cable assembly – 1.8m
	User Manual

Safety Notices

- The V3718 fits into a 6U VME crate
- The VX3718 fits into 6U VME64X compliant crates.
- Use only crates with forced cooling airflow.
- Turn off the crate before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION: This product needs proper cooling.

USE ONLY CRATES WITH FORCED COOLING AIRFLOW SINCE OVERHEATING MAY DEGRADE THE MODULE PERFORMANCES!

CAUTION: This product needs proper handling.

THIS BRIDGE DOES NOT SUPPORT LIVE INSERTION (HOT-SWAP)!
REMOVE OR INSERT THE BOARD WHEN THE CRATE IS POWERED OFF!

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

CAEN provides the specific document "Precautions for Handling, Storage and Installation" available in the documentation tab of the product web page that the user is mandatory to read before operating with CAEN equipment.

Power-on

To power on the board, perform the following steps:

1. Insert the V3718 into the crate
2. Power up the crate

Driver Installation

Once the Bridge is connected to the host PC by the USB cable or Optical Link fibre and both are powered on, the User needs to install the required drivers for the communication link and Operating System.

Direct Optical Link Drivers

The optical link CONET protocol is managed by the A2818 (PCI), A3818 (PCIe) controllers. The driver installation packages are downloadable for free on the CAEN website on the controller page (**login required**).

For the installation of the driver, refer to the documentation **[RD4][RD6]**.

Direct USB Drivers

The driver for the USB-2.0 link of the V3718 is downloadable for free on the CAEN website on the V3718 page (**login required**).

WINDOWS USERS

The procedure is based on a Windows 10 64-bit system; it may be slightly different for another Windows OS.

1. Go to the Device Manager area: find the new hardware listed under Other devices (**Fig. 11.1**).
2. Right-click on the "CAEN V3718" item and select the *Update Driver* option in the slide menu (**Fig. 11.2**).
3. Click on *Browse my computer for driver software* option (**Fig. 11.3**).
4. Press the [*Browse*] button and point to the destination path on the host PC where you unpacked the downloaded driver (**Fig. 11.4**).
5. Press the [*Close*] button at the end of the installation process (**Fig. 11.5**).
6. Check for the new hardware in the Universal Serial Bus controllers list of the Device Manager (**Fig. 11.6**).

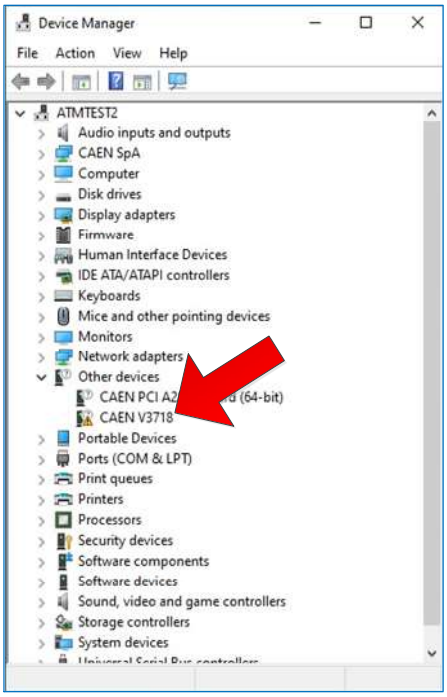


Fig. 11.1: USB Driver Installation: step 1

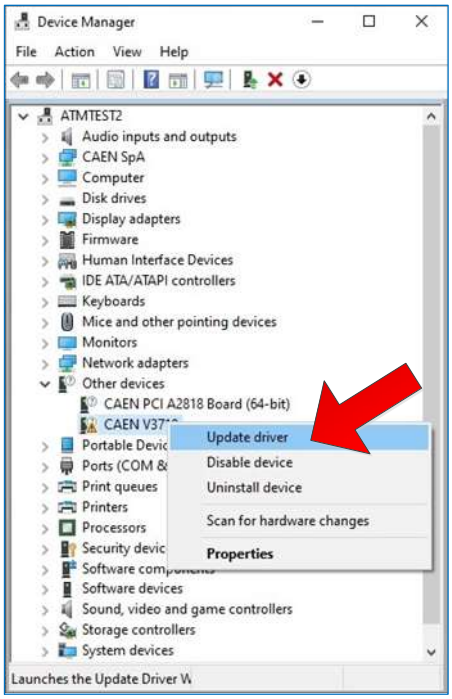


Fig. 11.2: USB Driver Installation: step 2

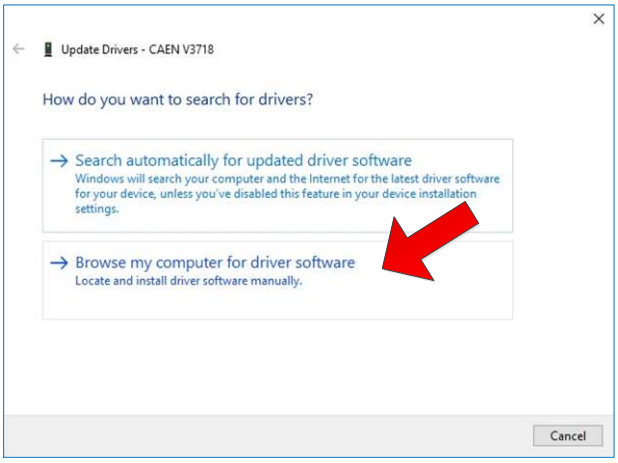


Fig. 11.3: USB Driver Installation: step 3

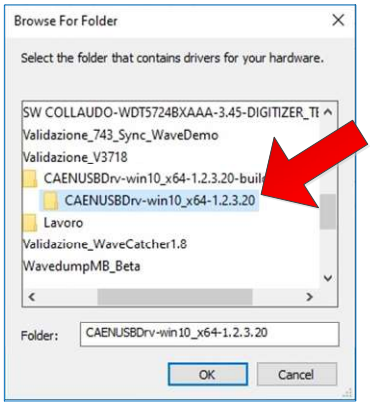


Fig. 11.4: USB Driver Installation: step 4

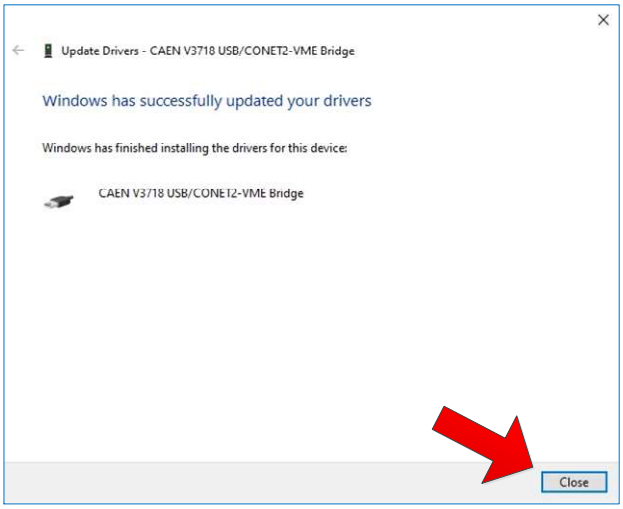


Fig. 11.5: USB Driver Installation: step 5

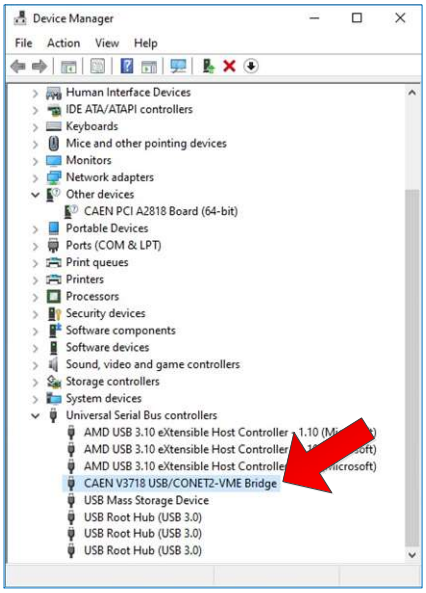


Fig. 11.6: USB Driver Installation: step

A4818 Driver

The V3718 can be controlled by a PC also through the A4818 USB 3.0-to-CONET adapter. The A4818 USB driver package (required only by Windows OS) is downloadable for free on the CAEN website on the adapter page (**login required**).

For the installation of the driver, refer to the documentation **[RD8]**.

12 Software

VMELib Library

CAENVMELib is a set of ANSI C functions helpful for a user software development to configure and control CAEN Bridges (old V/VX1718, V/VX2718, the new V/VX3718) **[RD4]** and the new A4818 adapter.

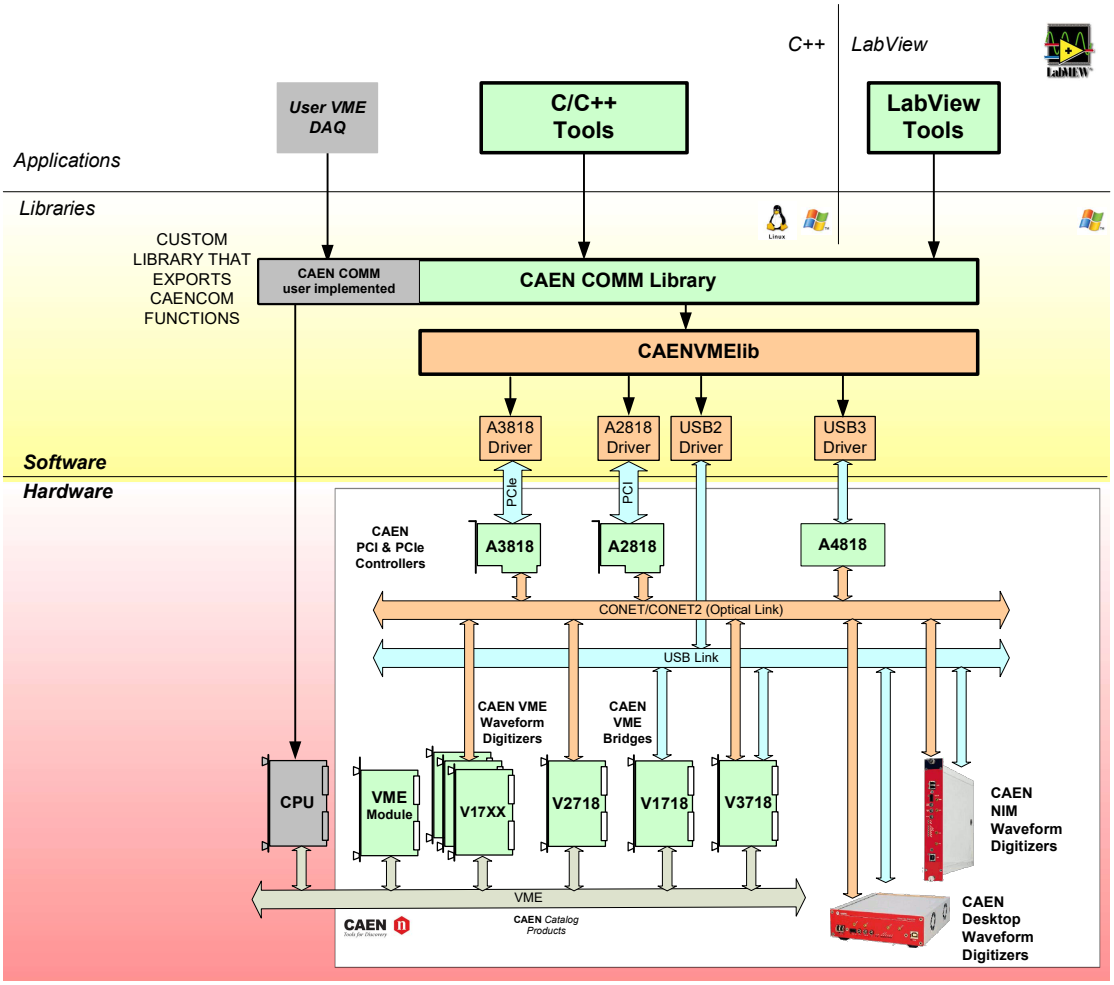


Fig. 12.1: Scheme of CAEN hardware and software layers.

CAENVMELib is logically located between a software application (e.g. sample codes provided by CAEN or user developments) and the lower layer software libraries.

CAENVME Demos

CAEN provides simple demos based on the functions of the CAENVMELib to demonstrate how to control CAEN Bridges and giving to Users a starting point for the development of their applications. Demo versions are available in C/C++ source code (for Windows and Linux OS), labVIEW™ and .NET with friendly graphical interfaces (Windows OS only).

Users find the CAENVME demo console version included in the Linux package of the CAENVMELib library, while Windows Users find all the available versions (console, LabVIEW, and .NET graphic) in a unique package free downloadable at the “CAEN VME Demos” page once they login to CAEN web site (www.caen.it).

CAENUpgrader

CAENUpgrader software is composed of command-line tools together with a Java Graphical User Interface.

On the V3718, CAENUpgrader allows in few easy steps to:

- Upgrade the firmware of the FPGA
- Read out the current firmware revision number

See Sec. **Firmware Upgrade** for instructions.

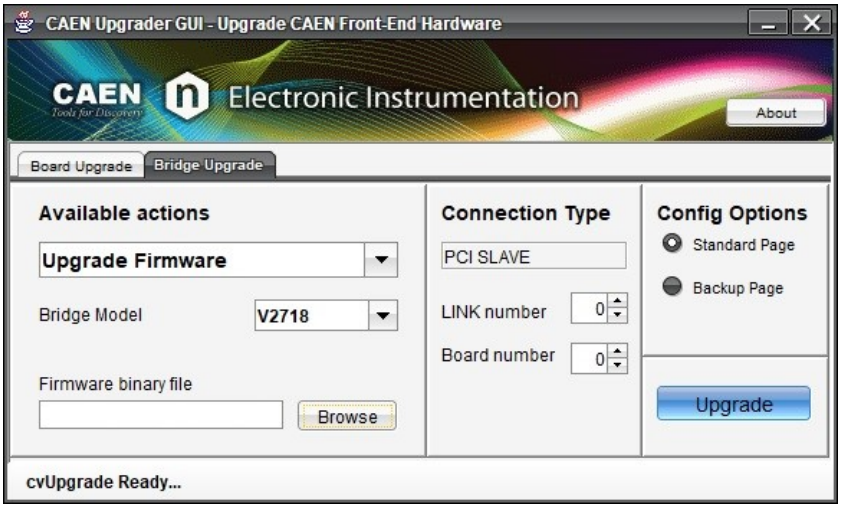


Fig. 12.2: CAENUpgrader Graphical User Interface

CAENUpgrader runs on Windows® and Linux® platforms, 32 and 64-bit operating systems. Users must also install the required third-party Oracle Java RE 8 u40 or higher.

CAENUpgrader for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVME and CAENCOMM libraries to be installed apart by the user.

Refer to the CAENUpgrader documentation for installation instructions and a detailed description **[RD1]**.

13 Firmware and Upgrades

The V3718 firmware is stored onto the on-board FLASH memory. This memory is divided into three main pages called Standard, Backup, and Factory. Each page stores a copy of the firmware that could not necessarily be the same revision number. In normal conditions, at power-on, a microcontroller reads the FLASH memory and automatically programs the FPGA of the module by loading the firmware copy stored in the Standard page of the FLASH.

The Standard page can be accessed by the User in read and write mode. The Backup page can also be accessed by the user in read and write mode, but it is suggested to use this page only in case of failure of the Standard. The Factory page is accessible in read-only mode as it contains a copy of the firmware delivered with the module and intended exclusively for recovery usage if both the Standard and the Backup pages are in a fail status (see Sec. **Troubleshooting**).

IT IS STRONGLY SUGGESTED TO OPERATE THE BRIDGE UPON THE STANDARD COPY OF THE FIRMWARE!

THE USER IS RECOMMENDED TO MAKE UPGRADES ONLY ON THE STANDARD PAGE OF THE FLASH!

Firmware File

Firmware updates are available for download at the V3718 page after logging in to the CAEN website (www.caen.it). The programming file is a binary BIN file, common to V3718 and V4718 Bridges, following described:

V3718-V4718_revX.Y.BIN

where X.Y is the “major.minor” revision number.

Note that the Factory firmware revision is always “128.Y”.

Firmware Upgrade

The user can upgrade the firmware of the V3718 through the CAENUpgrader software (see **Chap. 12**).

1. Launch CAENUpgrader and open the *Bridge Upgrade* tab.
2. Select “Upgrade Firmware” in the *Available actions* slide menu.
3. Set V1718 option as “Bridge Model” if you are going to use the USB link, while V2718 option in case of Optical link.
4. Press the Browse button and point to the firmware programming file on your PC.
5. Set the connection parameters according to your communication link and hardware setup [RD1].
6. Select Standard Page in the “Config Options”.
7. Press the Upgrade button.
8. Wait until the writing process is completed and the software returns a reboot message.
9. Power cycle the board to make the new firmware be loaded on the FPGA.

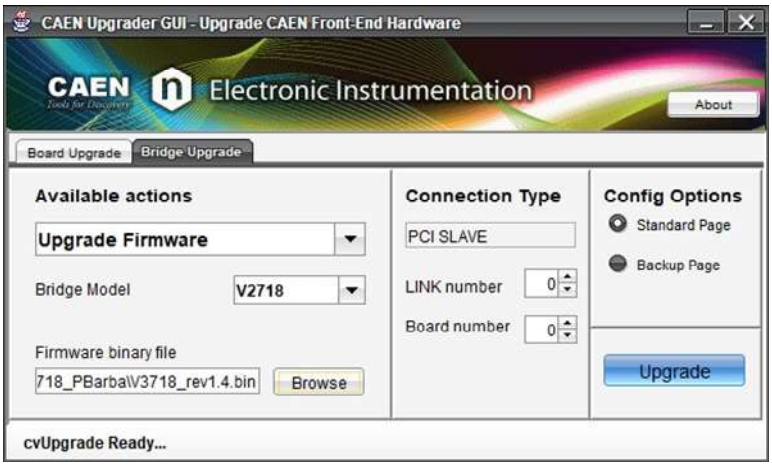


Fig. 13.1: Firmware upgrade settings

WRITING THE FIRMWARE ON THE FLASH NORMALLY TAKES FEW MINUTES. A VOLUNTARY INTERRUPTION OF THE PROCESS WHILE IT IS UNDER WAY MAY CAUSE FLASH DAMAGES!

For verification, the user can read out the current firmware revision number.

1. Select “Get Firmware Release” in the *Available actions* slide menu.
2. Set *V1718* option as “Bridge Model” if you are going to use the USB link, while *V2718* option in case of Optical link.
3. Set the connection parameters according to your communication link and hardware setup **[RD1]**.
4. Press the *Get FW revision* button.

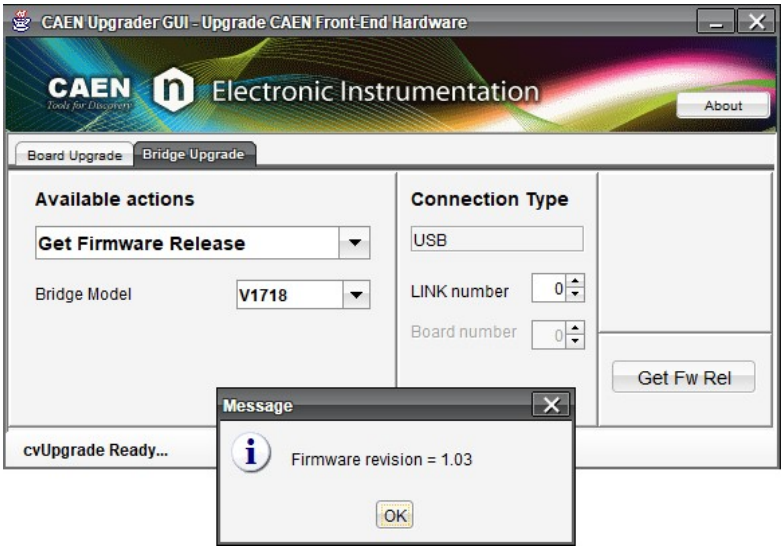


Fig. 13.2: Get Firmware Release settings

Troubleshooting

Usually because of an upgrade failure, the Standard or/and the Backup pages of the FLASH may be corrupted. In case the communication with the V3718 has been compromised, the user can try to recover through the front panel SYSRES button (see Sec. **Front Panel**). If the following attempts fail, please contact CAEN Support (Chap. **14**).

Recover from Standard Page Corruption

In this case, it is possible to reboot the Bridge from the Backup page of the FLASH:

- Hold down the SYSRES button and release it as soon the front panel I/O LEDs light on.
- Use CAENUpgrader to load the firmware on the Standard page of the FLASH.
- Reboot the board in Standard mode (no action on SYSRES) and try to read out the firmware revision number for verification.

Recover from Standard and Backup Pages Corruption

When it is not possible to communicate with the bridge neither in Standard nor in Backup mode, it is necessary to enter the Factory mode:

- Hold down the SYSRES button and release it after the front panel I/O LEDs flash off.
- Use CAENUpgrader to load the firmware on the Backup page of the FLASH.
- Reboot the board in Backup mode and read out the firmware revision number for verification.
- Load the firmware on the Standard page of the FLASH.
- Reboot the board in Standard mode and read out the firmware revision number for verification.

14 Technical Support

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

CAEN GmbH
Brunnenweg 9
64331 Weiterstadt
Germany
Tel. +49 (0)212 254 4077
Mobile +49 (0)151 16 548 484
info@caen-de.com
www.caen-de.com

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305
USA
Phone: +1 (718) 981-0401
Fax: +1 (718) 556-9185
info@caentechnologies.com
www.caentechnologies.com

CAEN S.p.A.
Via Vetraia 11
55049 - Viareggio
Italy
Phone +39 0584 388 398
Fax +39 0584 388 959
info@caen.it
www.caen.it

CAENspa INDIA Private Limited
B205, BLDG42, B Wing,
Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri (W)
Mumbai, Mumbai City,
Maharashtra, India, 400053
info@caen-india.in
www.caen-india.in