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1. DESCRIPTION

1.1.FUNCTIONAL DESCRIPTION

The **Model V 556** is a 1-unit wide VME module that houses 8 Peak Sensing Analog to Digital Conversion channels, able to detect and convert the peak value of the analog signals fed to the relevant connectors.

The basic structure of the circuit is a multistretcher configuration. For each channel the relevant stretcher detects the peak value of the input signal during the time interval in which a GATE input signal is TRUE. The channels can accept input pulses with a dynamic range from 0 V to 4.096 V.

The outputs of the eight stretcher sections are multiplexed and subsequently converted by a fast 12 bit ADC module (1 μ sec conversion time). The ADC module adopts a sliding scale technique to improve the differential linearity.

The board houses a 12 bit counter (Event Counter) for the trigger counting; it is increased whenever a pulse is sent to the GATE input.

Via VME it is possible to enable /disable each channel, to set a Low and a High Threshold for the Zero Suppression and to program a delay between the end of the GATE and the Start of the conversion.

Only the enabled channels are converted; if the value lies in between the Low and the High Threshold the result is stored in an Output Buffer that can be read via VME.

The Output Buffer is arranged in a FIFO logic 512 x16 bit.

The module houses a VME RORA INTERRUPTER: via VME it is possible to program the interrupt generation on the Output Buffer HALF FULL or on the Output Buffer NOT EMPTY.

A front panel LED (DTACK) lights up each time the module generates the VME signal DTACK.

An open-collector signal ("BUSY") is available on the front panel. This allows to obtain a wired-OR Global Busy signal. The BUSY is a high impedance output and is provided with two bridged connectors for daisy chaining.

The V556 Model uses the P1 and P2 connectors of VME and the auxiliary connector for the CERN V430 VMEbus crate (Jaux Dataway).

The module works in A24/A32 mode; the recognized Address Modifier codes are:

- AM= %3D standard supervisor data access;
- AM= %39 standard user data access;
- AM= %0D extended supervisor data access;
- AM= %09 extended user data access.

The module's Base Address is fixed by 6 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board. The Base Address can be selected in the range:

%00 0000 <-> %FF FF00 A24 mode;
%0000 0000 <-> %FFFF FF00 A32 mode.

The data transfer occurs in D16 mode.

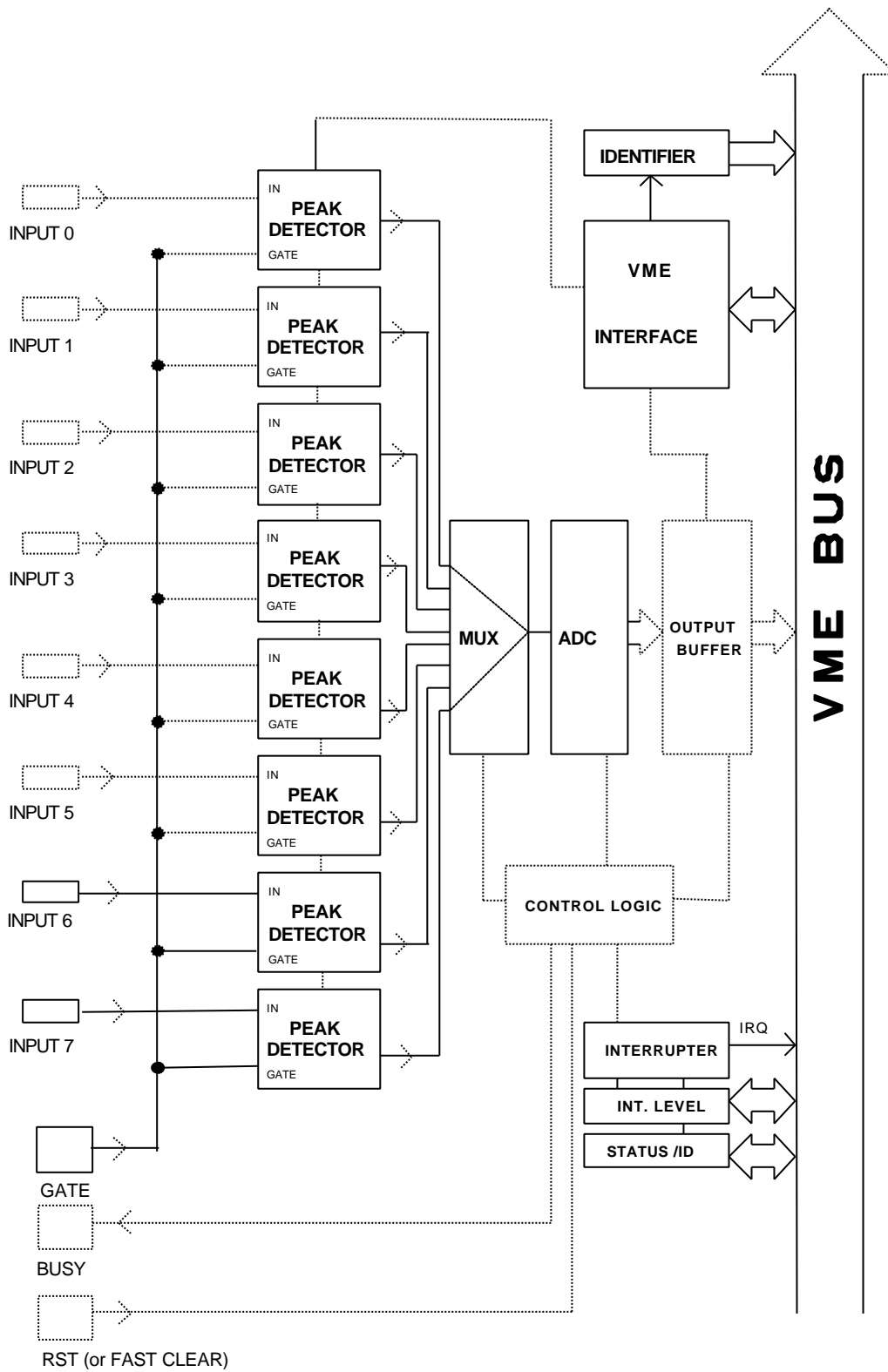


Fig. 1.1: Mod. V556 Block Diagram

2. SPECIFICATIONS

2.1. PACKAGING

1-unit wide VME unit. Height: 6U.

2.2. EXTERNAL COMPONENTS

(Refer to fig. 2.1)

CONNECTORS

- No.8, "IN 0..7", input connectors, LEMO 00 type; for the 8 single channel inputs.
- No.2, "GATE", input connectors, LEMO 00 type; two bridged connectors (for daisy chaining) for the GATE input signals.
- No.2, "RST", input connectors, LEMO 00 type; two bridged connectors (for daisy chaining) for the RST input signals.
- No.2, "BUSY", output connectors, LEMO 00 type; two bridged connectors (for daisy chaining) for the BUSY output signal .

DISPLAYS

- No.1, "DTACK", green LED, VME Selected; it lights up during a VME access.

2.3. INTERNAL COMPONENTS

(Refer to fig. 2.2)

SWITCHES

- No.6, rotary switches for the module VME Base address selection.

2.4. CHARACTERISTICS OF THE SIGNALS

- INPUT CHANNELS: positive polarity, DC coupled, 1 K Ω impedance;
Shape: square wave or semigaussian pulses with risetime > 100 ns;
Input range: 0 to 4096 mV (0.15 to 3.75 V suggested).
- GATE⁽¹⁾: Std. NIM level, high impedance;
min. width 200 ns.
- RST⁽¹⁾: Std. NIM level, high impedance;
min. width 10 ns.
- BUSY: Std. TTL open collector output (active high)

(1) This is a high impedance input and is provided with two bridged connectors for daisy chaining. Note that the high impedance makes this input sensitive to noise, so the chain has to be terminated on 50 Ω on the last module; the same is needed also if one module only is used, whose input has thus to be properly matched.

2.5. PERFORMANCES AND TEST RESULTS

Differential non linearity $\pm 2\%$ (between 10% and 90% of the range)

Integral non linearity $\pm 0.1\%$

Conversion time ⁽²⁾

Minimum	Maximum
3 μ s	13 μ s

(2) This is the time spent in the entire conversion sequence (see § 3.2); the minimum value is obtained when all the 8 values are not in the range selected and hence there is no ADC conversions, Substantially it is the Control Logic scan time. The max. value is obtained when all the 8 values are in the range selected and therefore converted and stored in the output buffer.

2.6. POWER REQUIREMENTS

+ 12 V	500 mA
- 12 V	100 mA
+ 5 V	1.3 A
- 5 V	500 mA

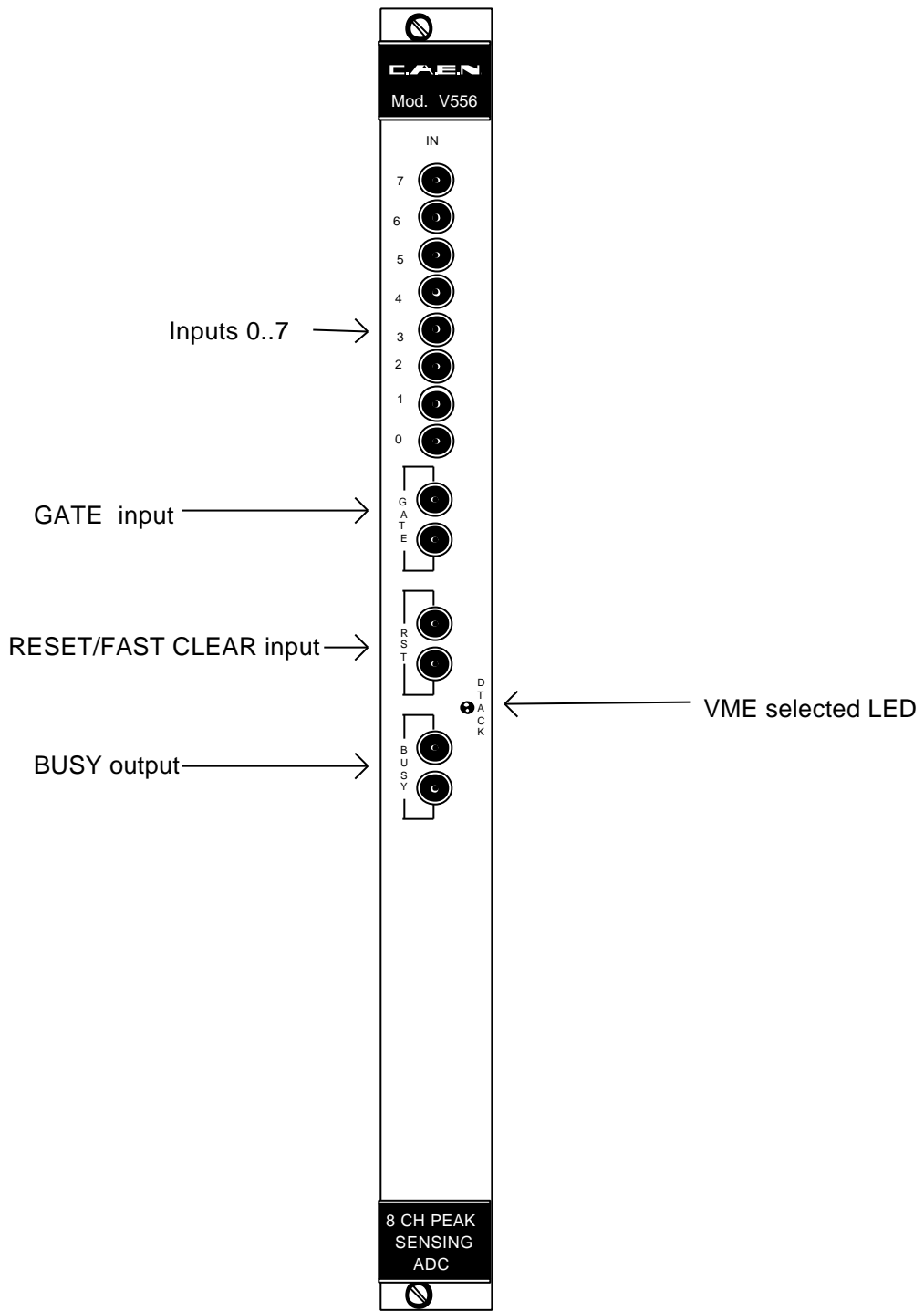


Fig. 2.1: Mod. V556 Front Panel

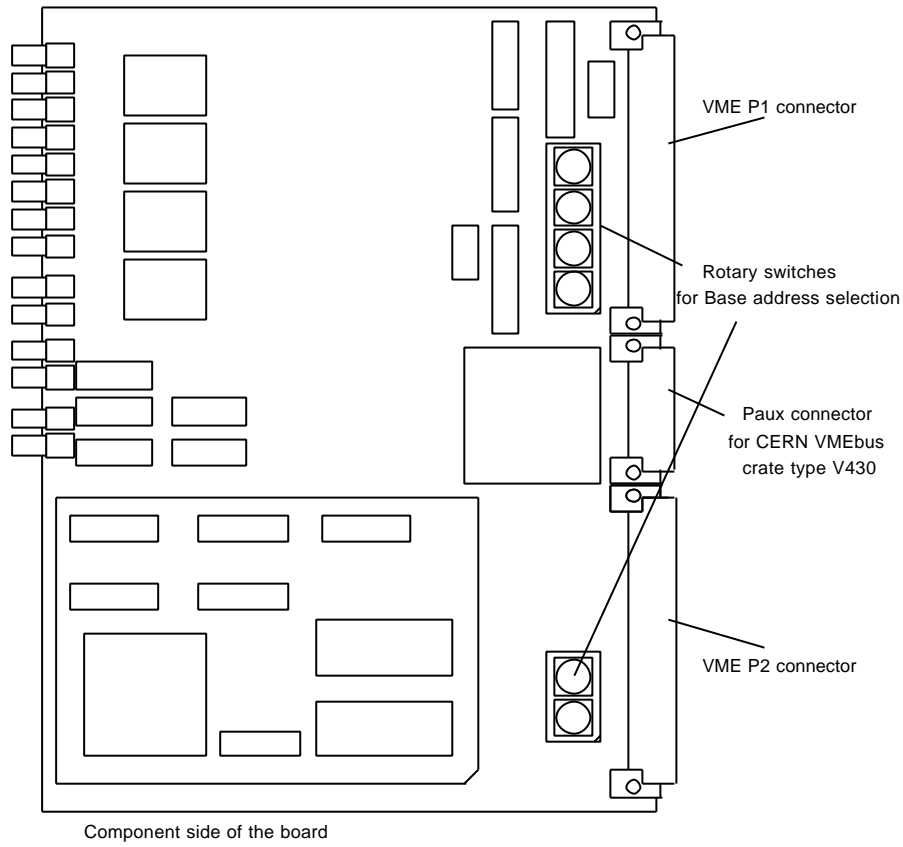


Fig. 2.2: Mod. V556 Components Locations

3. OPERATING MODES

3.1. GENERAL INFORMATION

The module V556 houses 8 Peak Detection channels. The Peak Detection outputs are multiplexed and subsequently converted by a high speed ADC module. A Control Logic controls the conversion sequence; it converts and stores in the Output Buffer only the channels that have values lying in a range between a High and a Low Threshold.

When the module is Busy it sets to TTL logic level "1" the Busy output. Moreover each channel can be individually inhibited via VME.

The module is Busy during the conversion sequence, and when the Output Buffer is not ready to accept data (Buffer full).

3.2. OPERATION SEQUENCE

If the module is not Busy and at least one channel is enabled, the leading edge of a NIM pulse on the GATE input:

- starts the Peak Detection on the enabled channels;

The trailing edge of the GATE signal stops the corresponding Peak Detection section and sets the BUSY output to 1 (Module Busy). It is possible to program a delay up to 8 μ s between the end of the GATE and the Start of conversion via the Delay Register. When the programmed Delay time is over, the Control Logic starts the conversion sequence:

- the output of all the Peak Detection sections are sampled;
- the Control Logic checks if the sampled value are in the selected range;
- If at least one value is lying in the range:
 - a header is stored in the output buffer; it contains the event counter value and the number of the channels in the range;
 - the sampled values in the range are converted and the 12 bit values obtained are stored in the Output Buffer together with the corresponding channel number.
- if no value falls in the range, no channel is converted and no data is written in the Output Buffer.
- increments the Event Counter;
- The Busy is removed and the module is ready for the next acquisition.

Figure 3.1 summarizes the operation sequence here described.

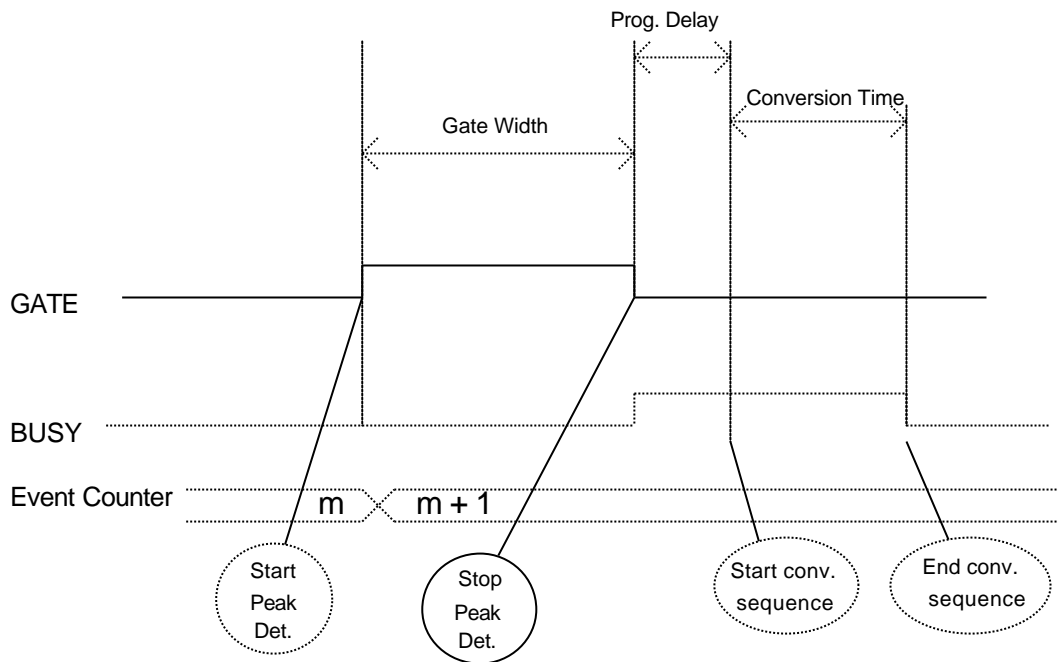


Fig. 3.1: Mod. V556 Acquisition Sequence

3.3. ENABLE/DISABLE CHANNEL OPERATION

Via VME It is possible to enable/disable the Peak Detection section of each channel; The bit <7..0> of the Control Register controls the status of the 8 Peak Detection sections:

- Control Register <n> = 0 → channel n Peak Detection disabled;
- Control Register <n> = 1 → channel n Peak Detection enabled.

The Control Register is available at the VME address Base + %1A.

All the Peak Detection sections are disabled (Control Register <7..0> cleared) in the following cases:

- by accessing via VME the address Base + %1C (Reset Register);
- by generating the VME signal SYSRES;
- at Power-On.

3.4. LOW AND HIGH THRESHOLD SETTING

The Control Logic converts only the channels that have values lying in a range between a High and Low Threshold.

The threshold values are 8 bit wide and are programmable via VME by a write access in two write-only registers:

- Low Threshold Register (THRL reg.) VME address = Base + %10;
- High Threshold Register (THRH reg.) VME address = Base + %12.

3.5.ADC DYNAMIC RANGE

The sliding scale correction reduces slightly the dynamic range of the ADC; the 12 bit digital output is valid from 0 to 3840; values from 3841 to 4095 are not correct.

The usable range of the analog input of the ADC is $\approx 0.15 \text{ V}..3.75 \text{ V}$. The conversion of an analog input that is greater than the upper limit could lead to an unpredictable digital output coding in the range from 0 to 255. The User should use the high threshold to maintain the analog input of the ADC under this upper limit.

The recommended High Threshold values are less than %C7 (hex).

3.6.GATE INPUT

If the module is not BUSY, the leading edge of a NIM pulse on the GATE input (trigger):

- starts the Peak value conversion of the enabled channels;

The trailing edge of a NIM pulse on the GATE input (trigger):

- stops the Peak value conversion of the enabled channels;
- sets the BUSY output to 1 (Module Busy);
- increments the Event Counter.

This is a high impedance input and is provided with two bridged connectors for daisy chaining; this allows to control easily a system of many units.

Note that the high impedance makes this input sensitive to noise, so the chain has to be terminated on 50Ω on the last module; the same is needed also if one module only is used, whose inputs have thus to be properly matched.

3.7.BUSY OUTPUT

An open-collector signal ("BUSY") is available on the front panel. This is a high impedance output and is provided with two bridged connectors for daisy chaining; this allows to obtain a wired-OR Global Busy signal of a system of many units.

Each module sets to 1 its Busy output after the trailing edge of a pulse on the GATE input (Module Busy) and releases it to 0 at the end of the conversion sequence. When the Module is Busy it does not accept another GATE pulse.

If many units are connected in daisy chain mode via the GATE and BUSY signal, after a pulse on the GATE input (trigger) the Global Busy signal is set to 1 and it is released to 0 only when all the V556 modules in the chain have completed the conversion sequence and the entire system is ready to accept another trigger.

This avoids that some modules in the chain accept another trigger while other modules are still Busy. This could cause a lack of coherence in the overall data (the event counter value of different modules could not be coherent).

3.8. RESET/FAST CLEAR INPUT

It is possible to program the the function of this input via the bit<15> of the Control register (FC bit)

- Control register <15> = 0 RESET;
- Control register <15> = 1 FAST CLEAR.

If the RST INPUT works as a RESET (FC bit in in Control Register set to 0), a pulse sets the board in the following state:

1. the event counter is set to 0;
2. the output buffer is reset (FIFO EMPTY);
3. all the channels are disabled (Control Register <7..0> cleared);
4. the delay is set to 0.
5. the Output Buffer is set to the HF mode.
6. the Interrupt start condition is set to 0 (Interrupt on buffer Half Full).
7. the Interrupt level is set to 0.

After a reset the module must be initialized again.

The VME Reset (access to address Base + %1E) and the generation of the VME signal SYSRES perform the same actions; moreover these operations set to 0 the FC bit.

If the RST input works as a FAST CLEAR (FC bit in in Control Register set to 1), a pulse generated after the end of the gate (within the window set with the delay register) aborts the conversion (The event counter is not incremented).

3.9. OUTPUT BUFFER UTILIZATION

The output buffer is arranged in FIFO logic 512 x16 bit .

Two utilization mode are programmable via VME :

HF (Half Full) mode: The Module does not accept any trigger (Module BUSY) when the number of data stored is greater than the half size of the FIFO.

FF (FIFO Full) mode: The Module does not accept any trigger (Module BUSY) when the FIFO is full. In this operating mode it is possible to utilize all the memory location, but it is possible to lose some data (If the FIFO becomes full during a conversion sequence).

3.10. OUTPUT BUFFER STRUCTURE

During the conversion sequence, if at least one Peak Detection output value is lying in the range identified by the High and Low Thresholds, the Control Logic stores in the output buffer the following words:

- a header that contains the event counter value and the number of the channels in the range; this number also indicates the number of subsequent words in the FIFO related to that event.
- the 12 bit converted Peak values together with the corresponding channel number.

If no channel is in the correct range the Output Buffer is not written.

The Output Buffer is available at VME address BASE + % 18.

The bit 15 of the Output Buffer indicates if the word read is a header or a channel data:

- Output Buffer <15> =1 → header
- Output Buffer <15> =0 → channel data

The status of the Output Buffer is available in the Control Register:

- Control Register <12> = 0 → Output Buffer is Half full;
- Control Register <14> = 0 → Output Buffer is Empty.
- Control Register <13> = 0 → Output Buffer is Full.

The following figure shows an example of the Output Buffer structure (see also fig. 4.4, 4.5):

- The first datum written is HEADER 5;
- In the Trigger n. 5 two channels (2 and 5) were in the selected range;
- In the Trigger n. 6 and n. 7 no channel was in the selected range;
- In the Trigger n. 8 three channels (0, 1 and 3) were in the selected range.

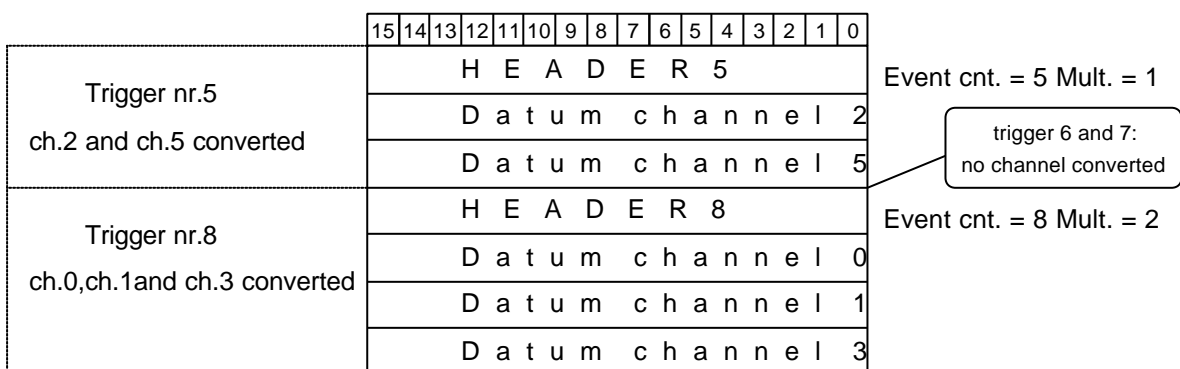


Fig. 3.2: Mod. V556 Output Buffer Data Packet FIFO Structure

3.11. INTERRUPT GENERATION

The operations of the V556 VME INTERRUPTER are fully programmable; via VME it is possible:

- to set the VME interrupt level;
- to program the VME interrupt vector (STATUS/ID);
- to program the interrupt generation on the Output Buffer HALF FULL or on the Output Buffer NOT EMPTY; this is controlled by the bit 2 of the Interrupt Register:
 - Interrupt Register <12> = 0 → Interrupt on Output Buffer HALF FULL;
 - Interrupt Register <12> = 1 → Interrupt on Output Buffer NOT EMPTY.

4. VME INTERFACE

4.1. ADDRESSING CAPABILITY

The module works in A32/A24 mode. This means that the module address must be specified in a field of 32 or 24 bits. The Address Modifiers code recognized by the module are:

AM=%39	standard user data access
AM=%3D	standard supervisor data access
AM=%09	extended user data access
AM=%0D	extended supervisor program access

The module's Base Address is fixed by 6 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board.

The Base Address can be selected in the range:

% 00 0000 <-> % FF FF00 A24 mode;

% 0000 0000 <->% FFFF FF00 A32 mode.

The Base Address reserves in this way a page of 256 bytes for the module. The Address Map of the V556 module is shown in Table 4.1.

4.2. DATA TRANSFER CAPABILITY

The internal registers and the Output Buffer are accessible in D16 mode.

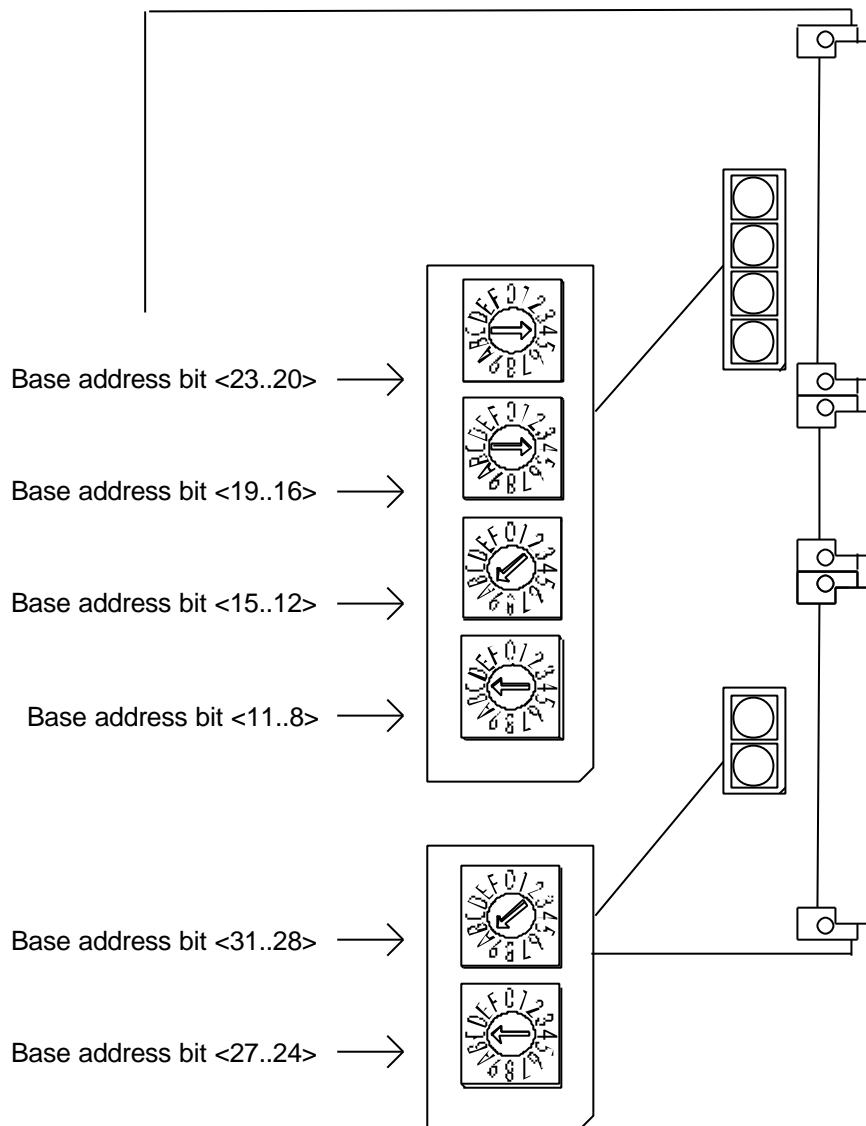


Fig. 4.1: Mod. V556 Base Address Setting

Table 4.1: Address Map for the Mod. V556

ADDRESS	REGISTER/CONTENT	TYPE
Base + %FE Base + %FC Base + %FA	Version & Series Manufacturer & module type Fixed code	read only read only read only
Base + %F8 . . Base + %1E	Not used . . HF Register	 read/write
Base + %1C Base + %1A Base + %18 Base + %16 Base + %14 Base + %12 Base + %10	Reset Register Control Register Output Buffer FF Register Delay Register THRH Register THRL Register	read/write read/write read only read/write read/write write only write only
Base + %0E . . Base + %02	Not used Not used	
Base + %00	Interrupt Register	read/write

4.3. MODULE IDENTIFIER WORDS

(Base address + %FA ,+%FC, +%FE read only)

The Three words located at the highest address on the page are used to identify the module as shown in figure 4.1:

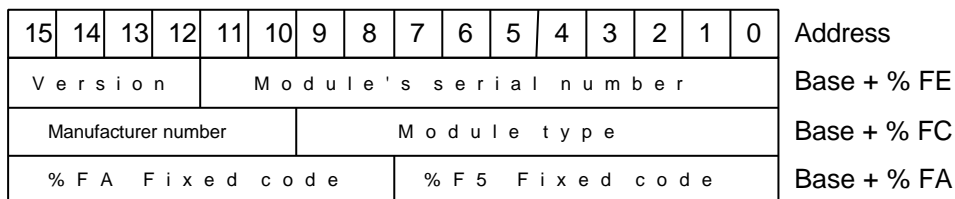


Fig. 4.2: Module Identifier Words

At the address Base + % FA the two particular bytes allow the automatic localization of the module.

For the Mod. V556 the word at address Base + % FC has the following configuration:

Manufacturer N°= 000010 b
 Type of module = 0000110110 b

The word located at the address Base + %FE identifies the single module via the module's serial number and any change in the hardware (for example the use of faster Conversion Logic) will be shown by the Version number.

4.4.HF REGISTER

(Base address + %1E read/write)

A VME access (read or write) to this location set the Output Buffer in the HF mode: the mode is available at the bit 12 of the Delay Register.

- Delay Register <12>=0 HF mode;
- Delay Register <12>=1 FF mode.

4.5.RESET REGISTER

(Base address + %1C read/write)

A VME access (read or write) to this location causes the following:

1. the event counter is set to 0;
2. the output buffer is reset (FIFO EMPTY);
3. all the channels are disabled (Control Register <7..0> cleared);
4. the delay is set to 0;
5. the Output Buffer is set to the HF mode;
6. the Interrupt start condition is set to 0 (Interrupt on buffer Half Full).
7. the Interrupt level is set to 0;
8. the FC bit is set to 0 (the RST input works as RESET).

The same action are performed if the VME signal SYSRES is active.

4.6. CONTROL REGISTER

(Base address + %1A read/write)

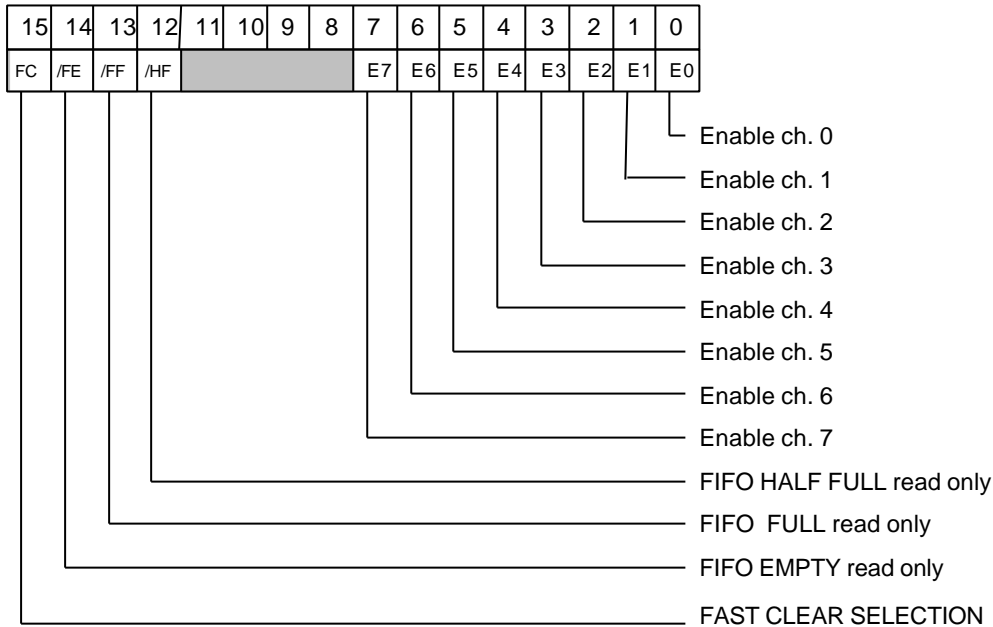


Fig. 4.3: Mod. V556 Control Register

- E<7..0> Enable channel<7..0>:
 = 0 channel n Peak Detection disabled
 = 1 channel n Peak Detection enabled
 These bits are cleared in the following cases:
 by accessing via VME the address Base + %1C (Reset Register);
 by generating the VME signal SYSRES;
 at Power-On.
- /HF Output Buffer half full bit read only.
 = 0 Output Buffer is half full.
- /FE Output Buffer empty bit read only.
 = 0 Output Buffer is empty.
- /FF Output Buffer full bit read only.
 = 0 Output Buffer is full.
- FC Fast Clear selection
 = 0 A pulse in the RST input acts as a RESET of the module.
 = 1 A pulse in the RST input acts as a FAST CLEAR of the module.

(Bits 8 to 11, are unused and are read as "one" on the VME data bus).

4.7.OUTPUT BUFFER

(Base address + %18 read only)

In this Buffer are available the data packets stored during the conversion sequence, if at least one Peak Detection output value is lying in the selected range.

The first word of the packet is a header; it contains the event counter value and the number of the channels in the range; this number also indicates the data packet length.

The other words contain the 12 bit converted Peak values together with the corresponding channel number.

The bit 15 of the word distinguishes between header and channel data:

- Output Buffer <15> =1 → header
- Output Buffer <15> =0 → channel data

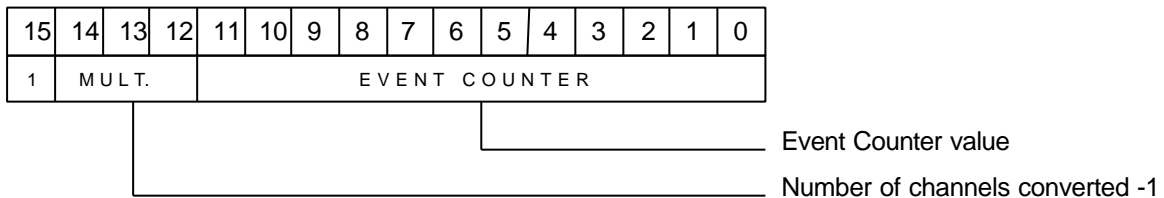


Fig. 4.4: Output Buffer Data Packet Header

EVENT CNT. 12 bit Event Counter
It counts the pulse on the GATE input; it is inhibited if the Module is Busy.

MULT Multiplicity
It indicates the number of channels in the range:
MULT+1 =number of channel, i.e., the packet length (MULT=0: one channel).

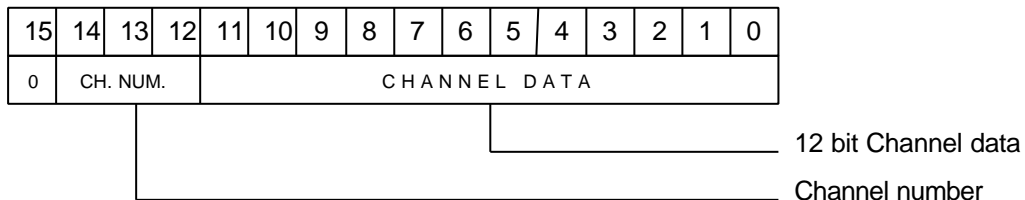


Fig. 4.5: Mod. V556 Output Buffer Channel Data

The following figure shows an example of the Output Buffer structure:

- The first datum written is HEADER 5;
- In the Trigger n. 5 two channels (2 and 5) were in the selected range;

- In the Trigger n. 6 and n. 7 no channel was in the selected range;
- In the Trigger n. 8 three channels (0, 1 and 3) were in the selected range.

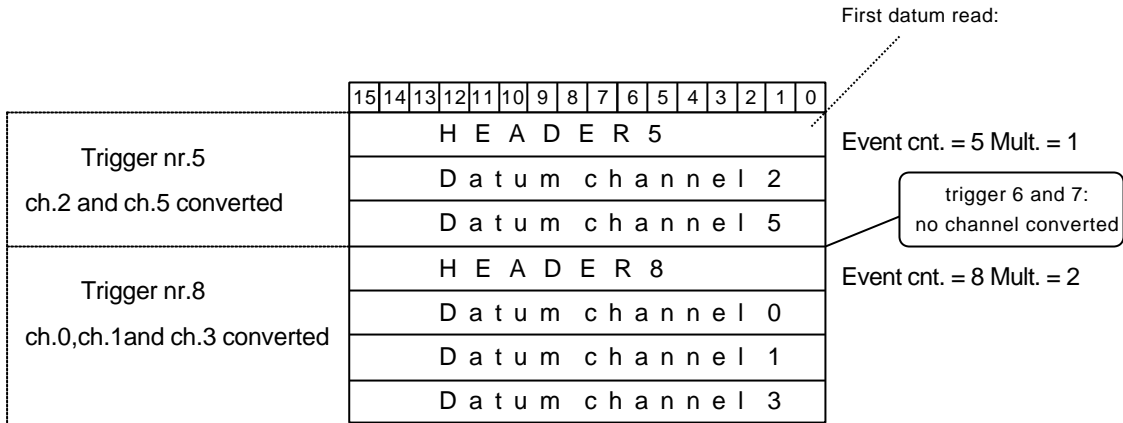


Fig. 4.6: Mod. V556 Output Buffer Data Packet FIFO Structure

4.8.FF REGISTER

(Base address + %16 read/write)

A VME access (read or write) to this location set the Output Buffer in the FF mode: the mode is available at the bit 12 of the Delay Register.

- Delay Register <12>=0 HF mode
- Delay Register <12>=1 FF mode

4.9.DELAY REGISTER

(Base address + %14 read/write)

The bits <7..6> of the Delay Register enable to program a delay value between the end of the GATE and the start of conversion. The programmable values are from 700 ns to 4.7 μs, in steps of 0.5 μs. This delay allows the generation of the FAST CLEAR:

Bit 12 is read only. The status of the bit 12 shows the Output Buffer operating mode.

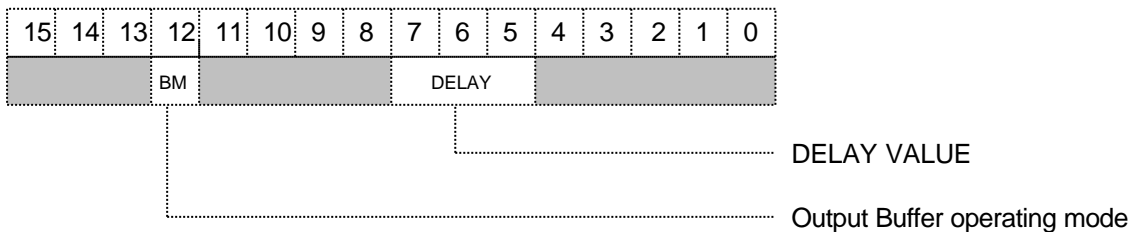


Fig. 4.8: Mod. V556 Delay Register

BM Output Buffer operating mode.
 =0 HF mode
 =1 FF mode

4.10. THRH REGISTER

(Base address + %12 write only)

This register (High Threshold Register) allows to set the 8 bit value of the High Threshold. This value can range from 0 to 4 V (%00 to %FF), with a resolution of approximately 16 mV/count.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								HIGH THRESHOLD.							

Fig. 4.9: Mod. V556 THRH Register

The usable range of the analog input of the ADC is $\approx 0.15 \text{ V}..3.75 \text{ V}$. The conversion of an analog input that is greater than the upper limit could lead to an unpredictable digital output coding in the range from 0 to 255. The User should use the High Threshold to maintain the analog input of the ADC under this upper limit.

The recommended High Threshold values are less than %C7 (hex).

4.11. THRL REGISTER

(Base address + %10 write only)

This register (Low Threshold Register) allows to set the 8 bit value of the Low Threshold. This value can range from 0 to 4 V (%00 to %FF), with a resolution of approximately 16 mV/count.

N.B.: this value must be lower than the High Threshold value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								LOW THRESHOLD.							

Fig. 4.10: Mod. V556 THRL Register

4.12. INTERRUPT REGISTER

(Base address + %0 read/write)

This register contains the value of the interrupt level and the STATUS/ID that the V556 INTERRUPTER places on the VME data bus during the interrupt acknowledge cycle. (Bits 8 to 11 are unused and are read as "one" on the VME data bus).

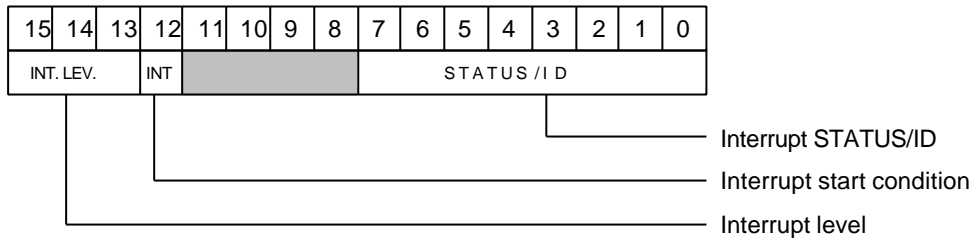


Fig. 4.11: Mod. V556 Interrupt Register

INT Interrupt start condition:
 = 0 Interrupt on Output Buffer HALF FULL;
 = 1 Interrupt on Output Buffer NOT EMPTY.

5. MOD. V556 INTERRUPTER

5.1. INTERRUPTER CAPABILITY

The Mod. V556 houses a VME RORA INTERRUPTER D08(o) type. This implies the following:

- it responds to 8 bit, 16 bit and 32 bit interrupt acknowledge cycles providing an 8-bit STATUS/ID on the VME data lines D00..D07;
- it removes its interrupt request when some on board registers are accessed by a VME MASTER (RORA: Release On Register Access).

5.2. INTERRUPT LEVEL

The interrupt level corresponds to the value stored in the Interrupt Register <15..13>. The register is available at the VME address Base + % 00.

5.3. INTERRUPT STATUS/ID

The interrupt STATUS/ID is 8 bit wide, and it is contained in the Interrupt Register<7..0> (address Base + % 00).

5.4. INTERRUPT GENERATION

Via VME it is possible to program the Interrupt Generation on the Output Buffer HALF FULL or on the Output Buffer NOT EMPTY; this is controlled by the bit 12 of the Interrupt Register:

- Interrupt Register<12> = 0 Interrupt on Output Buffer HALF FULL;
- Interrupt Register <12> = 1 Interrupt on Output Buffer NOT EMPTY.

5.5. INTERRUPT REQUEST RELEASE

The V556 INTERRUPTER removes its Interrupt request depending on the selected operating mode, according to the following:

1. If FIFO NOT EMPTY mode is selected, by reading out the FIFO until it doesn't become EMPTY;
2. If FIFO HALF FULL mode is selected, by reading out the FIFO until it doesn't become less than HALF FULL.

5.6. INTERRUPT SEQUENCE

```
{  
- if the FIFO becomes NOT EMPTY or HALF FULL (according to selected mode):  
  {  
  - it requests interrupt by driving an Interrupt Request line IRQ1..7 low according  
    to the Interrupt Register <15..13> value;  
  
  - during the subsequent acknowledge cycle it places on the VME data lines  
    D00..D07 the STATUS/ID; it is the byte contained in the 8 LSB of the Interrupt  
    register (address Base +% 00);  
  }  
  
- if a VME MASTER accesses the FIFO it releases the VME interrupt request line once  
  the Interrupt condition is removed (FIFO EMPTY if FIFO NOT EMPTY mode was  
  selected or FIFO NOT EMPTY if FIFO HALF FULL was selected).  
}
```

6. REFERENCES

[1] C. Cottini, E. Gatti, V. Svelto, " A sliding scale analog to digital converter for pulse height analysis", in Proc. Int. Symp. Nuclear, Paris, Nov. 1963.

[2] VMEbus Specification Manual Revision C.1, October 1985.

[3] G. Bianchetti et al., "Specification for VMEbus CRATE Type V430", CERN-EP, January 1990.