CERN-NP CAMAC Note 8-00
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PATTERN A
TYPE 021

ELECTRONICS II

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PATTERN UNIT A - TYPE C21

1. INTRODUCTION

1.1 General

The CAMAC system proposed (Rome 1968) by quite a large number of laboratories and institutes (including CERN), is a system well adapted to electronics for data handling. It is going to be used in CERN-NP in the field of "electronics" or "counter" experiment.

The basic documents to work with on CAMAC are the

- CAMAC ESONE report
- Euratom EUR report No. 4100.

All units to be described, as well as the logic systems, must follow the CAMAC compatibility rules as noted in these two fully-equivalent documents (EUR 4100 being a final document appearing after the ESONE report), and also the CERN-NP CAMAC options (Leaflet 1-00).

1.2 CERN-NP CAMAC notes

The CAMAC CERN-NP notes are intended to give an up-to-date state of what is currently done, preferred, or requested by CERN-NP in this field. This information is tentative and is meant to improve contacts with laboratories, industry and colleagues in an informal and simplified way, since experience has shown that complete detailed information is extremely difficult to provide in time. Most of the CAMAC "leaflets" (or "notes") will be devoted to particular plug-in units, and very often this will be the basis for tenders. The descriptions will therefore contain complete indications to allow for the detailed design of the unit. The information will also be such that interchangeability of plug-in units,

made according to the specifications, is guaranteed. This interchangeability is a very important feature for useful contacts with other laboratories.

All CAMAC rules must, of course, be followed as well as CERN options; therefore, only information pertinent to the described module shall be given.

2. DESCRIPTION OF THE UNIT (See block diagram).

The purpose of this unit is to record a pattern of fast signals (INPUTS 0 to 15) during a time given by the gate signal (gate).

This gate and all the input signals must be d.c. coupled. Any pulse length may therefore be used. The gate signal does not trigger any internal circuit for predetermined time values; therefore the internal effective gate corresponds to the input gate within the given specifications.

Some important points are : the absence of cross-talk between inputs, and between inputs and gate (even at max. drive), and also the time relation between inputs and gate.

3. FRONT PANEL

3.1 General

- Selector lamp It indicates that the plug-in has been selected. (N).
- Test button When pressed this injects artificially a 1 into all 16 inputs. Gate-open switch must be in position "open".
- Gate/Open switch Position GATE conditions the inputs by the "EXT. GATE". Position OPEN makes gate ∞, (i.e. inputs are not gated).
- Reset button It resets all 16 memories of the 16 input channels.

- Indicators They display the recorded input signals. Despite the fact that inputs are independent, the recorded bits (16) are considered by the read-out logic as a word. Input 15 corresponds to bit 15 or most significant.

3.2 Inputs

They have the same characteristics, which are as follows :

- Input impedance 50 Ω
- Reflection on a 1 nanosecond (10%-90%) rise or fall time with a -18 mA pulse) $< \left| \pm 15\% \right|$
- d.c. coupling (fastest rise/fall-time to ∞ slow
- Sensitivity AEC NIM/ESONE : 0 (-4 to 20 mA)
  1 (-12 to-36 mA)

Minimum pulse for input is 12 nsec at -4 mA
and flat at -12 mA during (max.) 10 nsec.

Standard -16 mA

Max. input level for proper standard functioning -36 mA

The max. rate which may be applied to the inputs without modifying the above limit is 50 MHz. The inputs must not record pulses which are between +20 mA and -4 mA (gate open).

- Measurements and definitions for delays, gate, inputs must be according to the following specifications :

gate : same as for inputs but

gmini = 16 nsec flat at -12 mA (20 nsec at -4 mA)

geff = g input ± 0,2 g input

Δg = gate effective delay - Input delay < 6 nsec $^{+2}_{-6}$

(State Δg on front panel besides gate input)

Δg should be held as small as possible. The measurement of Δg is made with standard -16 mA inputs (10 nsec at -12 mA) and gate (16 nsec at -12 mA).

4. CAMAC logic

- The word obtained by juxtaposing the 16 possible gated bits is w (2^{15} is input 15, 2^{14} is input 14, etc...)

  w is read by $F_{\text{read }(0)} \cdot N$

  or by $F_{\text{read and clear }(2)} \cdot N$

  w is cleared by :

  $$C.S_2 + F_{\text{clear }(9)} \cdot N + F_{(2)} \cdot N$$

- A test can be made which loads 1 in all 16 memory-bits. This is done by :

  $$F_{(25)} \cdot N \rightarrow w = 111 \ldots . 1$$

- Q has to be generated for $F_0 + F_2 + F_6 + F_9 + F_{25}$

- "Module characteristic" is read by

  $F_{(6)} \cdot N$ and produces 021/1 on the data lines (see CAMAC options 1-00).

5. VARIOUS

- Strongly recommended is the use of micrologics throughout, also particularly for the "fast" gate-input circuitry.

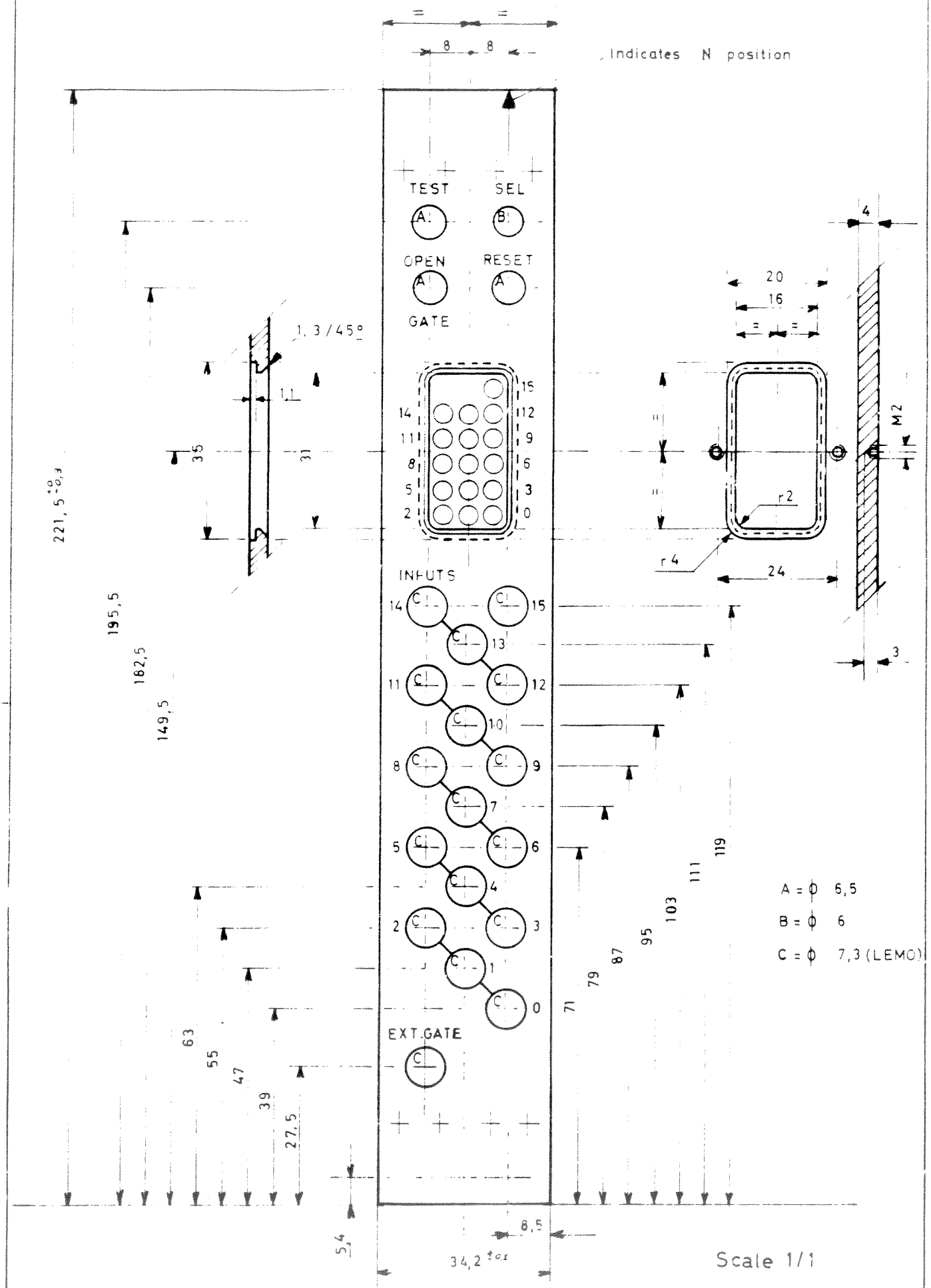
- Shorter input and gate times should be obtained if possible (using micrologics).

- The power dissipation of the complete double-unit must not exceed 12W for any continuous operation.

- The exact N position is marked with an arrow on the front panel.

6. ADDENDUM

Sub-address $A_{(0000)}$ -at least bit 2^0- has to be used with all functions so that sequential addressing be possible. (CAMAC Esone preprint p. 13).



FRONT PANEL - WIDTH 2, CAMAC

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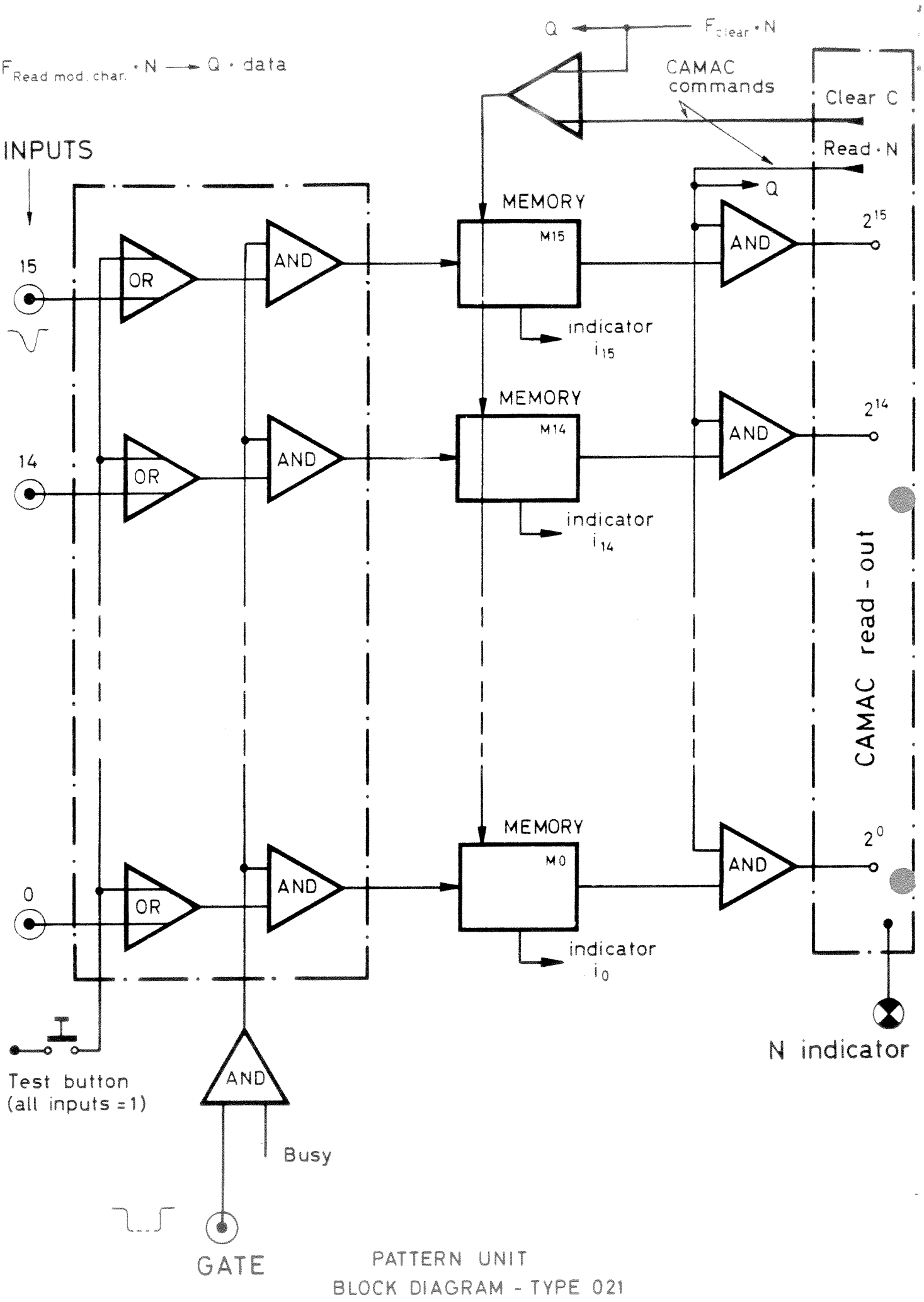
021 - 1A4



PATTERN UNIT
BLOCK DIAGRAM - TYPE 021

CERN - NP
021 - 2A4
18.12.68