MEDEA

GAN'ELEC

CONSTANT FRACTION DISCRIMINATOR FCCS

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SUMMARY

1- Introduction

The CAMAC discriminator FCC8 includes features such as timing based on ***constant fraction discrimination*** for eight input channels. It also provides information upon the number of triggered channels, i.e. the ***multiplicity***. The design of this discriminator results from a joint development by the Service Electronique Physique de l'Institut de Physique Nucléaire d'Orsay, (France), which is part of IN2P3 (CNRS), and GANIL, a French joint laboratory IRF (CEA), and IN2P3 (CNRS). This product is manufactured and commercialized under a license from CNRS/IN2P3/GANIL.

Experimental set-ups include today a great number of detectors. This number has been continuously increasing for the last few years and this evolution should continue. This module, with eight input channels, type constant fraction discrimination, is intended to serve the users' need for electronic signal-processing modules which are very compact and easy to control. Remote control functions (threshold set-up, output signal width adjustment, multiplicity level selection) can be hence managed through flexible computing procedures.

The features of this discriminator meet the needs of multichannel equipment with high-resolution timing requirements. It was possible to meet such high quality standards by applying the SMD technology which allows large-scale integration.

The availability of signals for both timing and multiplicity for event characterization, is greatly advantageous for the control of data to be acquired within a decision time as short as possible.

2- FCC8 Description.

2.1- Main performances.

Timing.

- Walk : ± 150 ps typically, for an input with 5 ns rise time, and variable from 12 mV to -5 V. Internal delay is set to 8 mV in this case. The threshold is set to 8 mV.
- Output Jitter : 40 ps for a -50-mV input with a rise time of 5 ns.
- I/O[1] Counting Rate : Maximum 25 MHz at output B for a minimum pulse width.
- Double Pulse Resolution : < 30 ns.

The walk does not require any adjustment.
The walk will be constantly optimized by sampling closed-loop control where the performance is almost independent of the counting rate.

- Dead Time : Equal to the adjusted ECL output pulse width. It is possible, at factory, to achieve higher dead times for specific applications.
- Fraction : It is set to 20% at factory. We should be consulted before any modification can be considered.
- Delay : Adjustable by steps of 1/10 of the total delay.

[1] I/O means Input/Output.

Multiplicity.

- Analog Output : 25 mV/channel.
- Time Overlapping : Minimum 10 ns.

2.2- Inputs and Outputs.

- 8 channels in one 1/25 CAMAC unit.
  LEMO 00 connectors on the front panel.
  Input impedance : 50 Ω.
  Input dynamical range : - 10 mV to -5 V.
  DC input signals.
- (2 x 8) outputs in differential ECL
  2 x 8 pin connectors.
  Impedance : 110 Ω .
  Differential ECL : (-0,8 V and - 1,7 V)
  Typical rise time : 2 ns.
  Typical decay time : 2 ns.
  Twisted two-wire pair type cables.
  A and B output pulse width : 25 ns to 220 ns.

  An ECL signal is present at the output when an analog input signal is higher than the adjusted threshold level[2]. A green LED per channel on the front panel indicates the presence of this signal. For the output, twisted two-wire pair type ribbon cables will be required to avoid interchannel crosstalk.
- Delay:
  Integrated delay line with located constants
  11 internal adjusting steps per jumper.

Multiplicity.

- Analog multiplicity.
  2 LEMO 00 connectors on the rear panel.
  Enable to chain several FCC8.
  Impedance : 50 Ω (to be matched at both extremities of the chain).
  This chain line provides an analog signal as wide as that adjusted to the ECL output, A, and which height is proportional to the number of channels[3] triggered (25 mV per channel activated).

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[2]Threshold adjustment is detailed in paragraph 3.4.

[3]Provided that all channels have an equal width and are in the same time window.

- 1 logic output (differential ECL), internal Multiplicity M/8

  2 x 1 pin connector on the front panel.
  Impedance : 110 Ω.
  Typical rise time and decay time : 2 ns
  Twisted two-wire pair type cable.
  Minimum pulse width : 100 ns.
  Maximum pulse width : follows A-output adjustment.

- 1 logic output, total Multiplicity M/T.

  2 x 1 pin connector on the front panel.
  Impedance 110 Ω.
  Typical rise time and decay time : 2 ns.
  Twisted two-wire pair type cable.
  Minimum pulse width : 100 ns.
  Maximum pulse width : follows A-output adjustment.

Inhibition.

- 1 "Inhibition" input in NIM with a 50-Ω load

  The (2 x 8) outputs will be inhibited in the presence of a -0,8 V signal.
  LEMO 00 connector on the rear panel.

Notes.

- Power Supply.

+24 V	0,2 A
-24 V	0,1 A
+6 V	0,6 A
-6 V	2,5 A

- FCC8 modules should be fed in fan-cooled crates.

2.3- Remote Control. CAMAC features.

Threshold Adjustment.

threshold of channel 0	F16 A0	0≤data≤255	writing of channel 0
	F 0 A0		readout of channel 0
threshold of channel 1	F16 A1	0≤data≤255	writing of channel 1
			writing
	F 0 A1		readout of channel 1
threshold of channel 7	F16 A7	0≤data≤255	writing of channel 7
	F 0 A7		readout of channel 7

The data value is equal to the selected threshold value divided by the conversion gain which is 3.8 mV per bit.

During threshold writing/readout by CAMAC, the LED of the concerned channel will light and the milli-voltmeter on the front panel will indicate the threshold value .

ECL output width adjustment.

A-output width	F16 A8	0≤data≤255	A-output writing
	F 0 A8		A-output readout
B-output width	F16 A9	0≤data≤255	B-output writing
	F0 A9		B-output readout

During control on the front panel, the milli-voltmeter will continuously indicate 0. The visual inspection of the pulse width will be performed using an oscilloscope.

Multiplicity.

Decision threshold for Internal Multiplicity	F16 A10	0≤data≤255 data - 36,5 (M-1) 1≤ M ≤ 8	internal multiplicity writing
	F 0 A10		internal multiplicity readout
Decision threshold for Total Multiplicity	F16 A11	0≤data≤255 data - 5,12(M -1) 1≤ M ≤ 50	total multiplicity readout
	F 0 A11		total multiplicity readout

2.4- Control and front panel presentation.

All adjustments and controls of the FCC8 (except the Multiplicity level) may be performed in either local or remote control mode. The front panel is shown in Figure 1.

Control Key.

This is a three-position key with one function per position :

- Transitory lower position. Every time this position is passed through, the number of the channel with the threshold being indicated and which is accesssible in the local control mode, will be incremented by one.
- The middle position ("visu") allows the threshold value of the channel selected in either local or CAMAC remote control mode to be indicated on the milli-voltmeter.
- The upper position inhibits the local control mode and clears both threshold indication and n-channel selection. In this configuration, only CAMAC orders will be able to control the FCC8.

Data Key.

When the control key is in the middle position ("visu"), data key depression will increment (+) or decrement (-) either threshold or width values, according to the selection. When the key is depressed for less than 0.5 seconds approximately, a one-step incrementation or decrementation is performed. When depressed for a longer time, this key will allow fast sweeping

Red LEDs indicate the selected channel, *when the control key is in the middle position.*

Green LEDs denote that a channel has been triggered, *in any circumstances.*

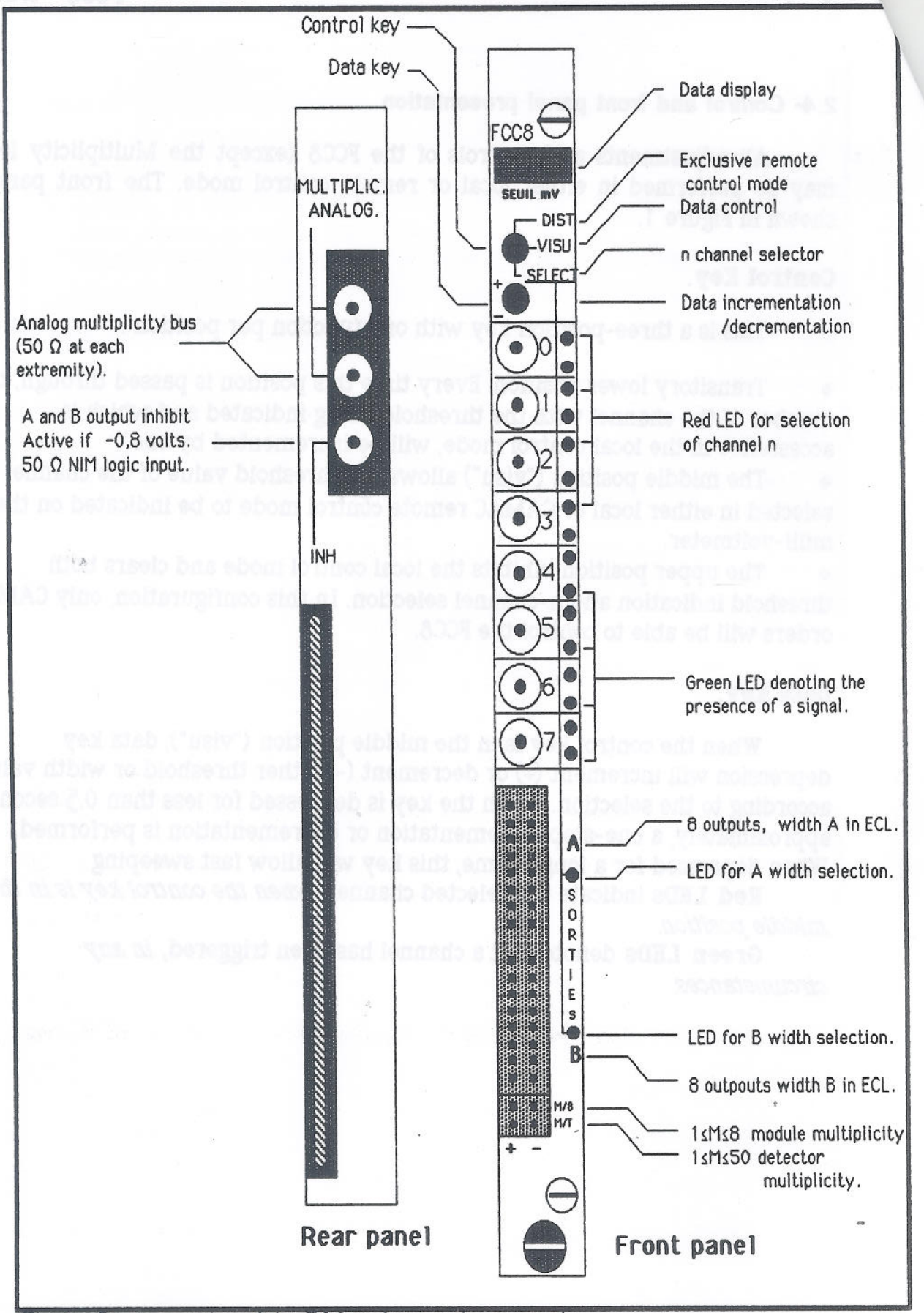


Fig. 1 - Representation of the FCC8's front and rear panels.

3- Timing.

3.1- Necessity.

The pulse rise time is not equal to zero. Thus, this pulse intersects the trigger threshold at a time which depends upon the pulse amplitude.

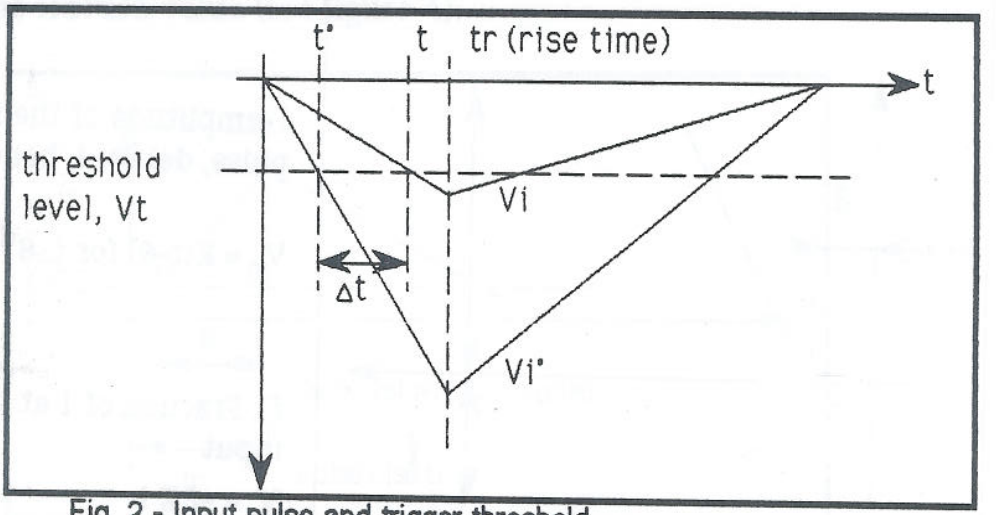


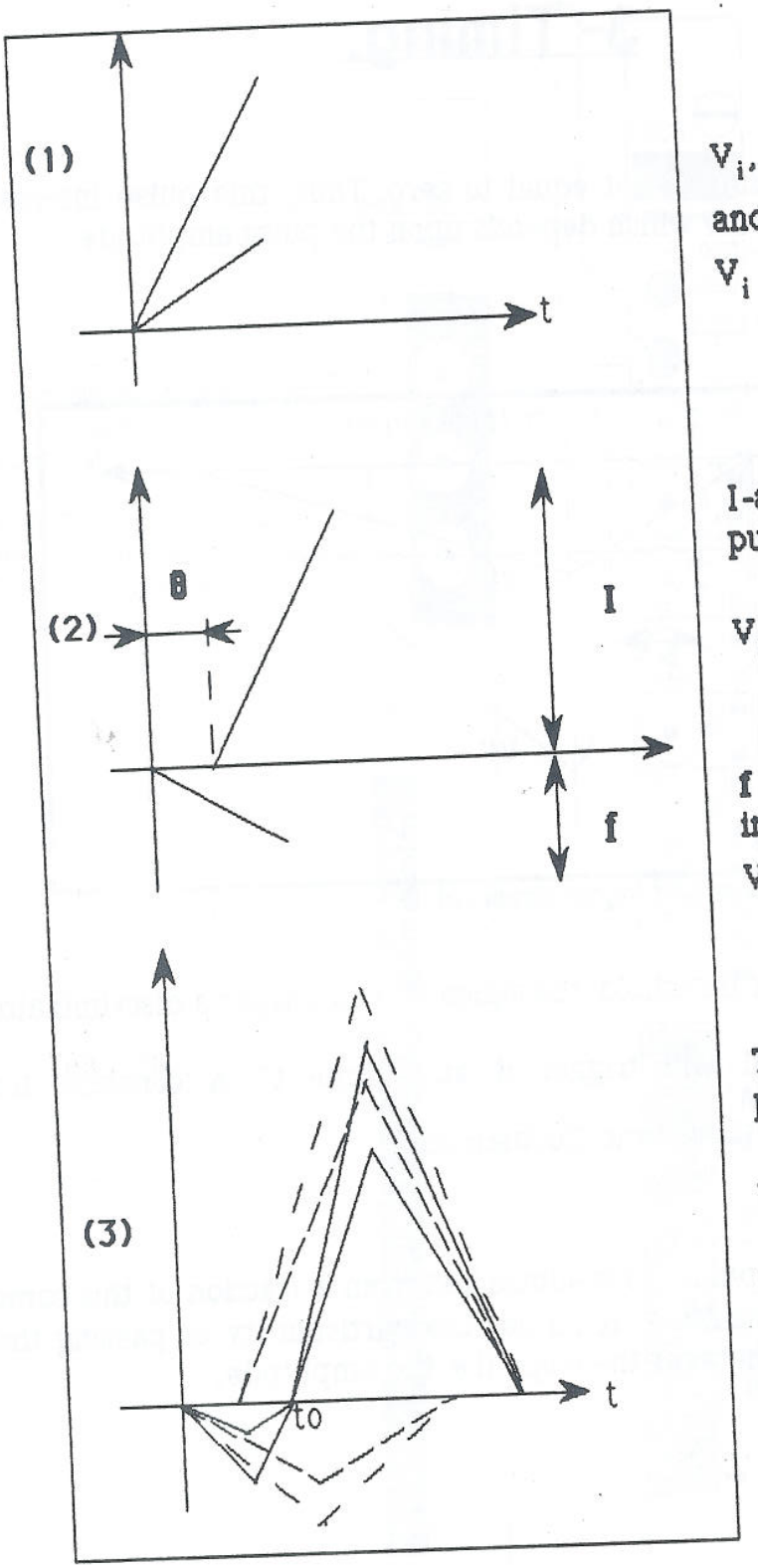
Fig. 2 - Input pulse and trigger threshold.

For a given trigger threshold, the signal v_i will trigger a discriminator at a time t, while v_i° signal will trigger it at a time t°. A constant fraction discriminator minimizes these time fluctuations[4].

3.2- Theory of operation.

The θ-delay input pulse (1) is subtracted from a fraction of this same non delayed pulse (2). The resulting signal has the particularity of passing through zero at the same time, whatever the slope (i.e. the amplitude)

[4] Additional time fluctuations occur due to the lack of pulse homothety and electronics imperfectness.



V_i, function of amplitude and time

$V_i = K \cdot t$

I-amplitude of the input pulse, delayed, hence:

$V_0 = K(t-\theta)$ for $t \geq \theta$

f : Fraction of I at the input

$V_I = -f K t$

The resulting pulse will pass through zero for :

$V_I + V_0 = 0$

i.e. :

$$t_0 = \frac{\theta}{1-f}$$

Fig. 3 - Schematic operation of the constant fraction discrimination.

The time at which the signal passes through zero is independent of the pulse slope, **dv/dt**. Bipolar pulse generation will be therefore determined by the selection of the fraction **f** and the delay **θ**.

3.3- Delay Selection.

3.3.1- Theoretical Selection.

According to the principle described in paragraph 3.2, the fraction and the delay will have a specific value every time the pulse passes through zero. The fraction of FCC8 is fixed to 0.2 at factory. The corresponding theoretical delay is thus equal to the input pulse rise time (100%) minus the rise time required to reach the fraction value (see figure 4).

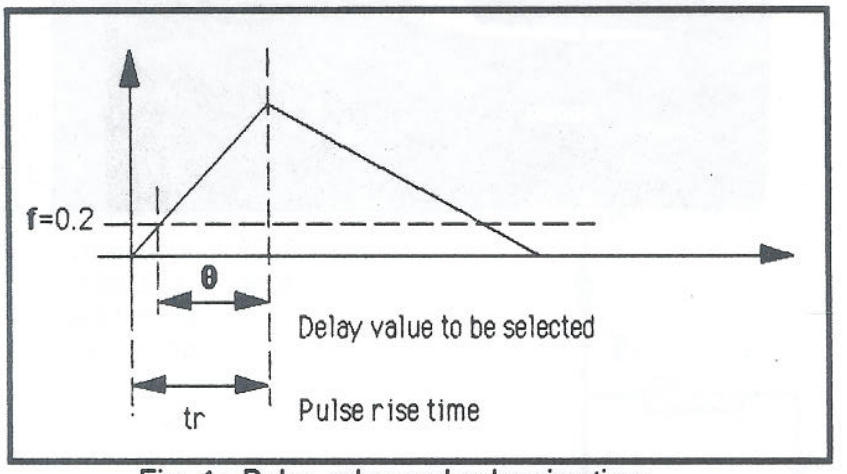
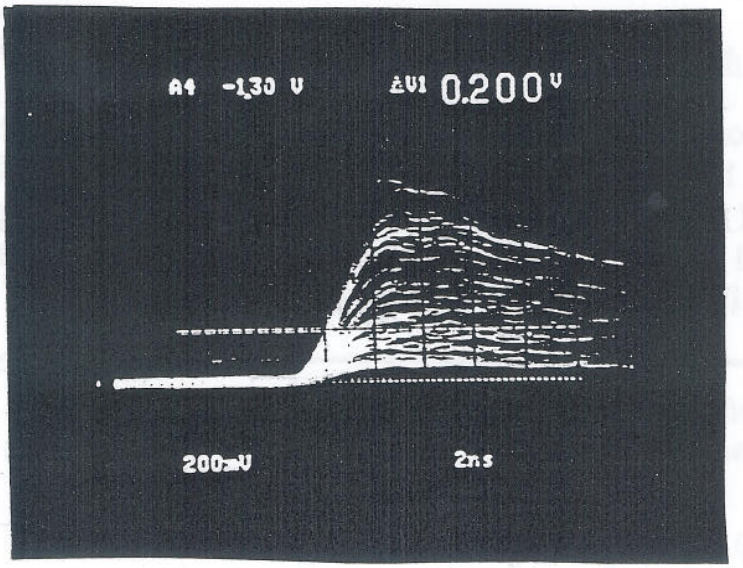


Fig. 4 - Delay value and pulse rise time.

The value θ should be first measured with a wideband oscilloscope (e.g., Textronix, type 2467), using the mobile indexes ΔV (Fig. 5.A) and Δt (Fig. 5.B).

A)-



B)-

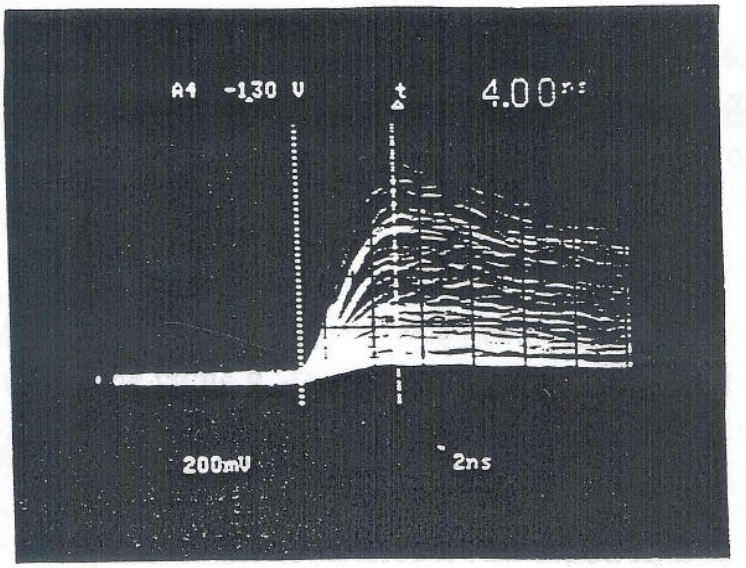


Fig. 5 - Fraction and delay : A)- Fraction measurement ; B)- θ .Delay measurement.

3.3.2- Application set-up.

The set-up shown in Fig. 6 allows bipolar pulse shaping to be reproduced on the oscilloscope.

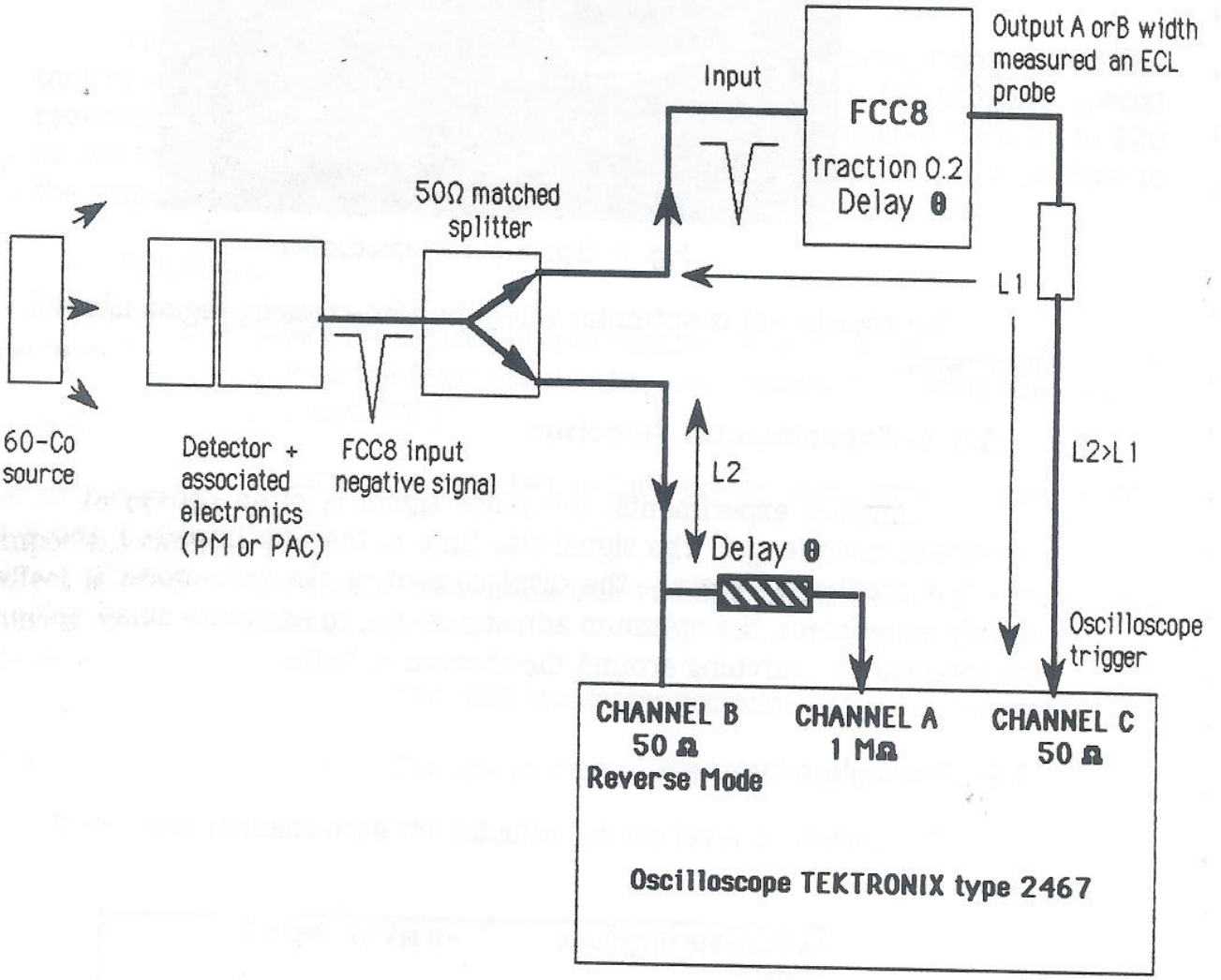


Fig. 6 - Electronic set-up diagram showing the operation of constant fraction discrimination[5].

Simply assign the value θ which has been previously measured, to the delay line, *l*, and to the FCC8 channel concerned (See Fig 5.B).The oscilloscope is thereby triggered by either output A or output B of the FCC8 (transposed to the NIM standard). Input A of the oscilloscope is calibrated to a level equal to five times the level of input B of the oscilloscope. This input, A, is in High Impedance and summed. Input B is 50-Ω matched and in reverse mode.

The oscilloscope reproduces the bipolar signal shaping performed by the FCC8 (Fig. 7).

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[5] PM means photo-multiplier and PAC means charge pre-amplifier.

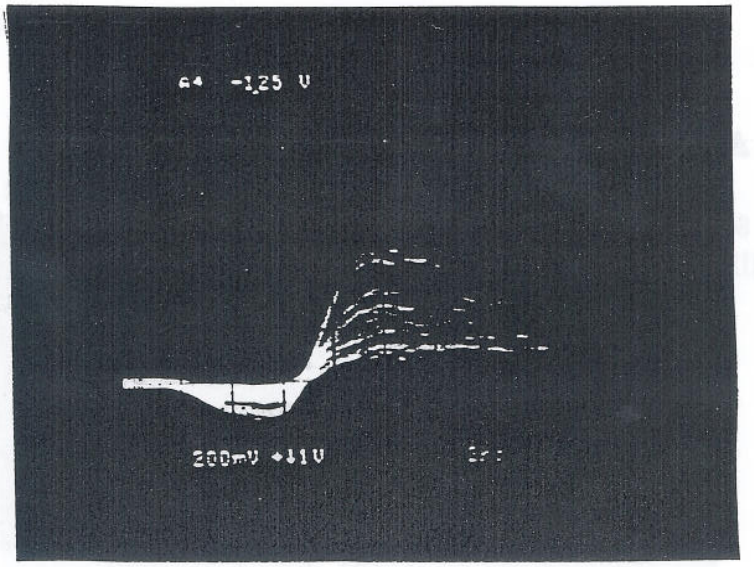


Fig. 7- Bipolar pulse reproduction.

The adjustment is optimum when the zero-crossing region is at its narrowest.

3.3.3- Experimental Selection.

In physics experiments, the pulse signal is often conveyed through an important cable length. The signal rise time is thereby impaired and a trailing effect is produced, causing the displacement of the zero-crossing point. Thus, during experiment, the optimum adjustment for an adequate delay value, θ, will be obtained by searching around the theoretical value.

3.4- Threshold adjustment.

The threshold level can be adjusted for each channel separately.

Adjustable threshold range	- 8 mV to - 980 mV
Resolution	8 bits
Threshold value in mV	(CAMAC data) x 3,85

Procedure :

- Select the desired channel with the control key on the front panel by keying the low position or using the CAMAC function. (S2.3).
- Read the threshold value on the milli-voltmeter or increment/decrement this value using the data key or the CAMAC function (S2.3).

Note :
The cut-off level in the pulse spectrum is usually higher than the displayed threshold value for small delay values, θ.

3.5- ECL Output Width Adjustment.

The width of each ECL output (A or B) is adjustable, using either the control keys on the front panel, or the CAMAC function (S2.3).Unless special requirement on ordering, the width of A and B can be adjusted from 25 to 220 ns. Maximal dispersion for each signal width is of the order of 10% relative to the manufactured modules.

Procedure :

1- Select the desired output channel (A or B), by setting the control key on the front panel to the lower position, or using the CAMAC function (S2.3).

2- Observe the selected output on an oscilloscope, using a ECL probe.

3- Increment/decrement this value, using the data key or via the CAMAC function.

- The milli-voltmeter permanently indicates zero.
- The law of variation is shown in Fig. 8 :

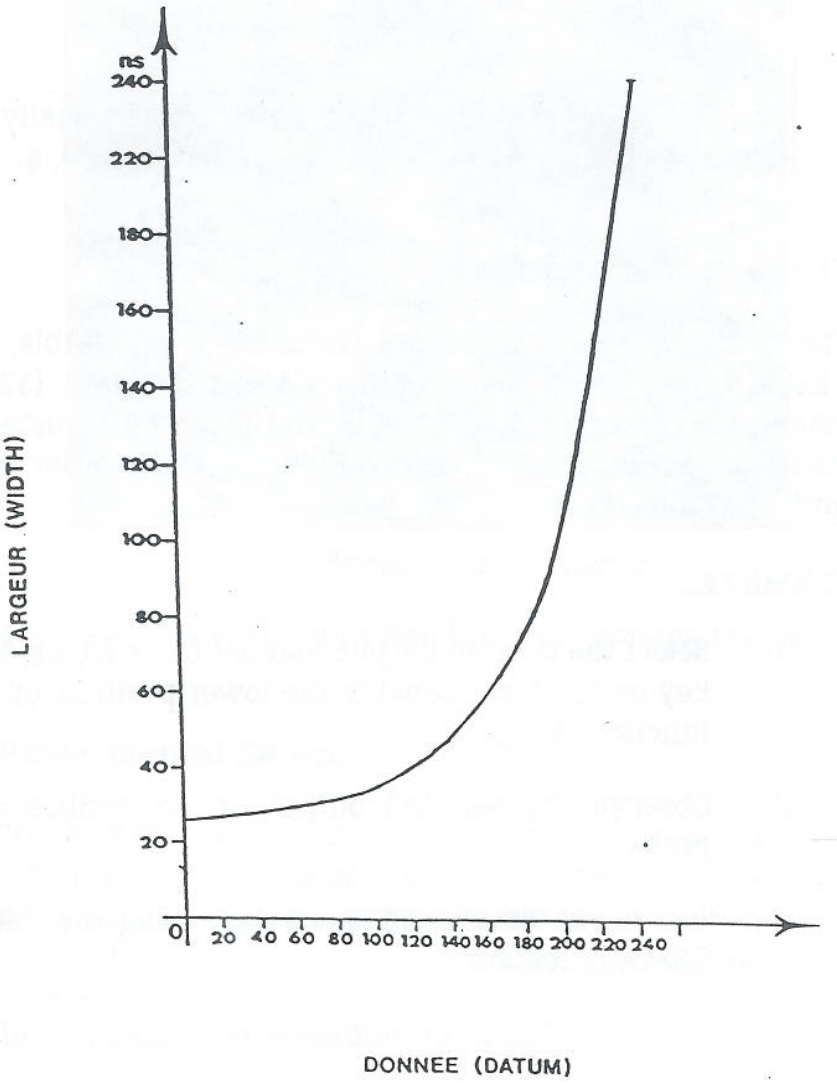


Fig. 8- Output width variation.

4- Multiplicity.

4.1- Introduction.

Physics experiments implementing a great number N of detectors (several hundreds) involve a so-called multiplicity decision, i.e. the acceptance of the events for which the M channels appear at the same time in a given time window.

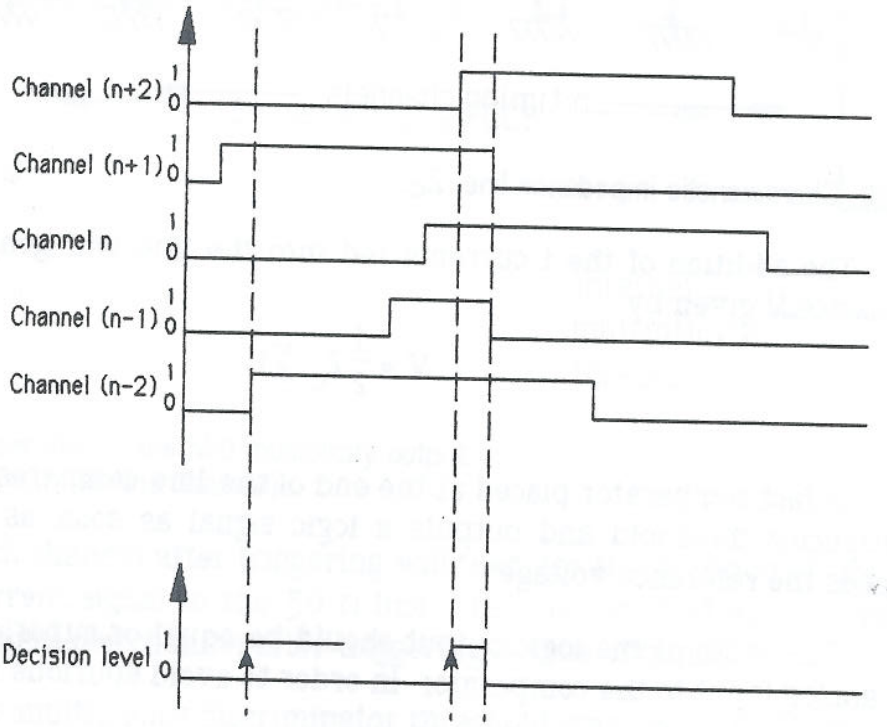


Fig. 9- Timing diagram showing the principle of the multiplicity.

In this timing diagram, the trigger time will occur in :

t_1 if $M \geq 2$

t_2 if $M \geq 5$

M is selected by the user.

The FCC8 provides ECL logic signals when multiplicity thresholds are reached. The multiplicity is analysed at two levels :

- on the 8 channels of a FCC8;
- on all channels of chained FCC8.

4.2- Principle.

Any triggered channel will feed a calibrated current to an analog summing line (Fig. 10).

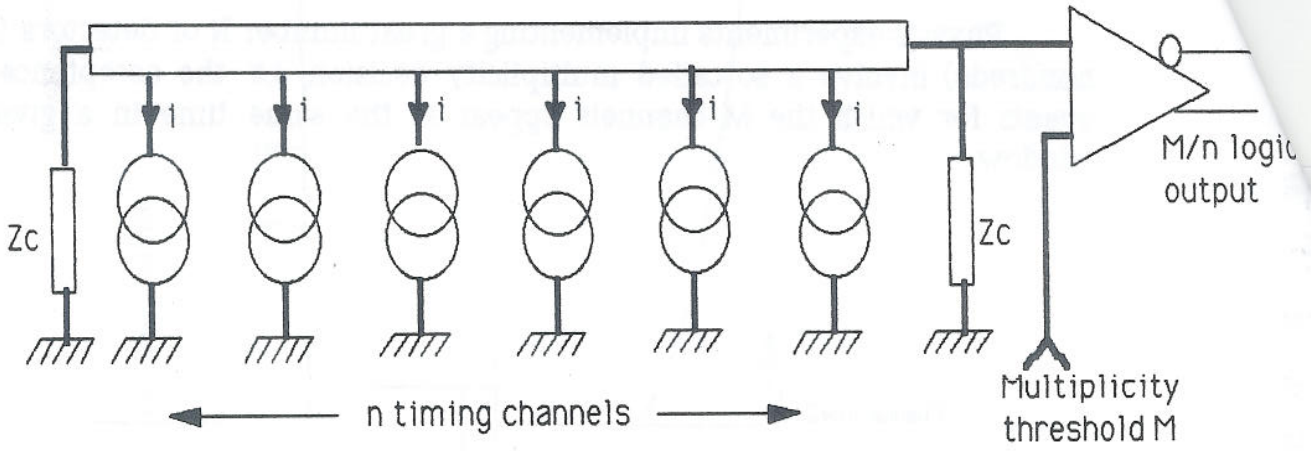


Fig. 10- Characteristic impedance line, Z_c.

The addition of the i currents fed into the line will generate a potential difference V given by :

$$V = \frac{1}{2} Z_c \sum i$$

A fast comparator placed at the end of the line compares V to the desired Multiplicity threshold and outputs a logic signal as soon as the line voltage exceeds the reference voltage.

The width of the logic output should be equal or superior to the width of the analog input to the comparator in order to avoid spurious re-triggering.

4.3- Multiplicity for a module, M/8.

This is the multiplicity for the 8 channels of a FCC8. The block diagram is given in Fig. 11.

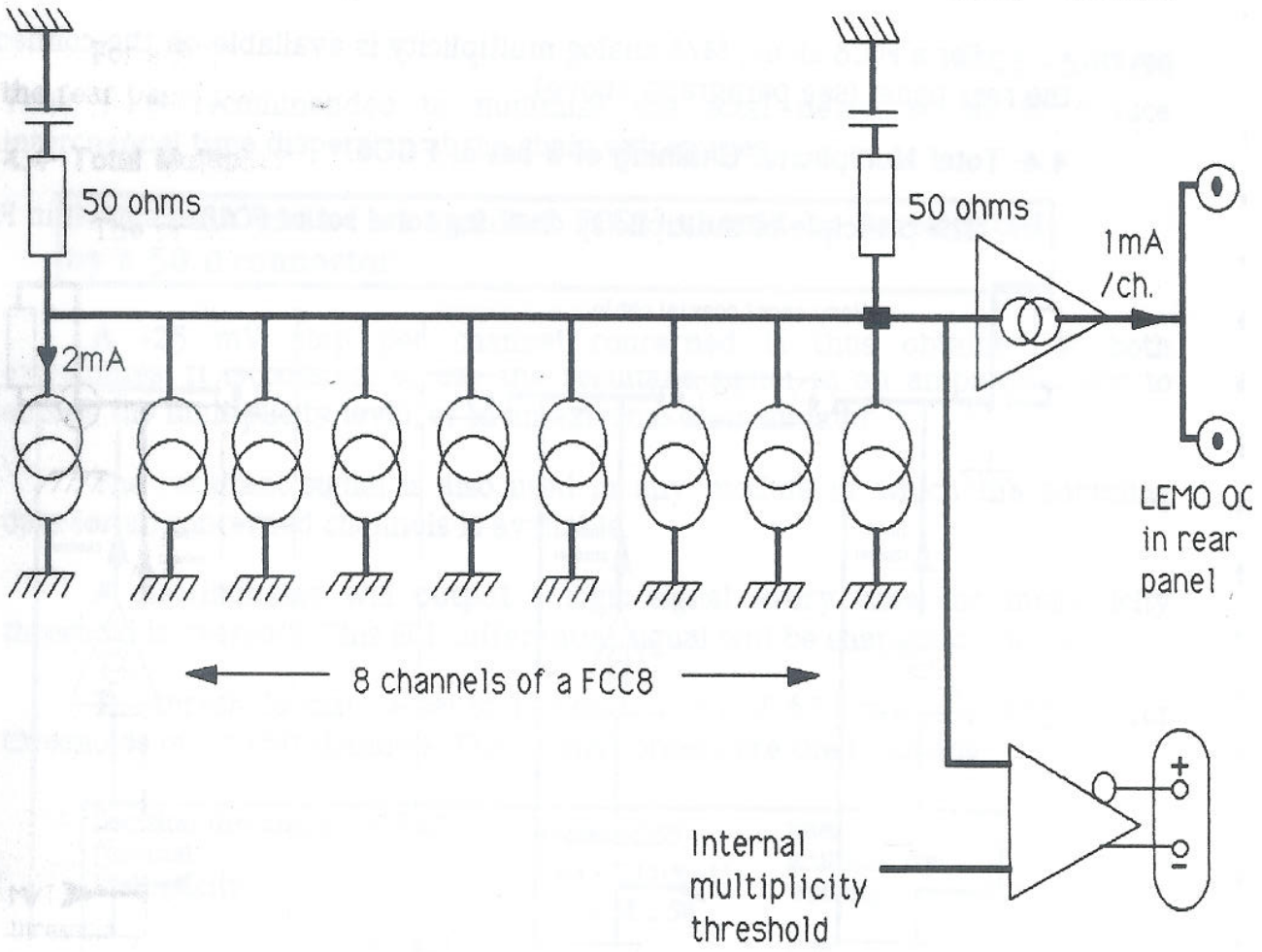


Fig. 11- Operation of the M/8 multiplicity output.
(ch. means channel).

Each channel after triggering will feed, for the duration of the output, A, a 2-mA current signal to the 50 Ω line which is matched at both extremities. A 50-mV signal per channel after triggering is thus obtained.

The multiplicity discriminator threshold may be set to 25 mV, 75 mV, 325 mV for multiplicity thresholds of 0, 2, ... 7, 8.

Threshold adjustment is controled by CAMAC, **exclusively** :

Decision threshold for internal multiplicity	F16 A10	0≤data≤255 data - 36,5 (M-1) 1≤ M ≤ 8	internal multiplicity writing
	F0 A10		internal multiplicity readout

The minimal width for the logic output is 100 ns and the maximal width equal to that of channel A.

For a FCC8 alone, M/8 analog multiplicity is available on the connecto the rear panel (see paragraph above).

4.4- Total Multiplicity. Chaining of a set of FCC8.

The principle of multiplicity chaining for a set of FCC8 is shown in Fig. 12.

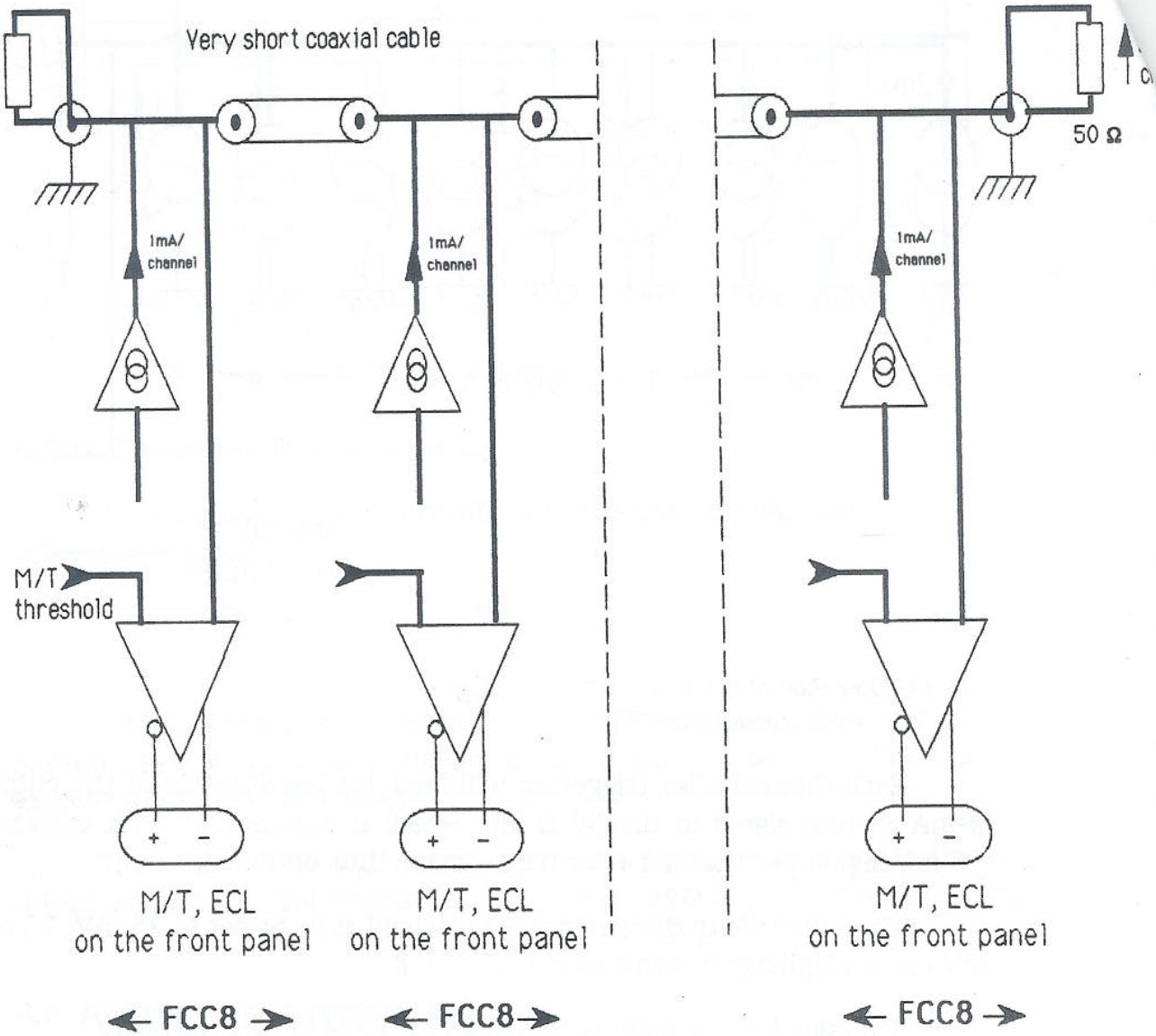


Fig. 12- Diagram showing the chaining of a set of FCC8.

A current amplifier (required to separate the summing lines) feeds 1 mA per channel concerned, to the general summing line.

The set of FCC8 should be chained from the rear panel via 50 Ω cables as short as possible (0.3 to 0.5 ns). Note that the summation is performed on a line.

Thus, it is recommended to minimize the total delay, so as to reduce interchannel time dispersion at the chain extremities.

Both chain ends (1st and last FCC8) should be terminated by a 50 Ω connector.

A +25 mV step per channel concerned is thus obtained at both extremities. It is possible to use the resultant signal in an amplitude ADC to encode the multiplicity level, or in an external discriminator.

The resultant signal is also used in any module in which the summing data for all concerned channels is available.

A discriminator will output a logic signal every time the multiplicity threshold is overshot. This ECL differential signal will be shaped to 100 ns.

The threshold may be set to 12,5 mV, 37,5 mV, 62,5 mV .... 1237,5 mV for thresholds of 1 to 50 channels. The CAMAC orders are the following :

Decision threshold for total Multiplicity	F16 A11	0≤data≤255 data = 5,12(M - 1) 1≤ M ≤ 50	total multiplicity writing
	F0 A11		total multiplicity readout

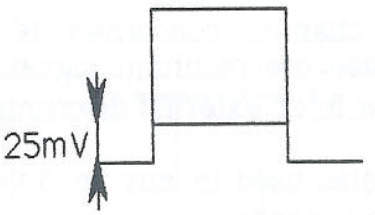
The data "sum of channels concerned" is accessible by any FCC8. It is possible to fix a different threshold for each module, so as to simplify multiplicity level encoding via a bit pattern.

If only one FCC8 is used to detect the general multiplicity level, it is recommended to use the module located in the middle of the summing line.Time dispersions are thereby reduced by a factor 2, according to the channels concerned. In this conditions, an interchannel dispersion of ± 4 ns may be expected with 40 FFC8 chained via 0.3-ns coaxial cables.

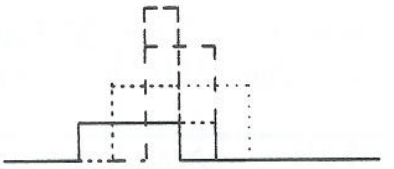
4.5- Remarks upon the use.

The following three diagrams show the characteristic shapes of an analog multiplicity signal. It clearly appears that such a signal cannot be used as a timing signal (see Fig. 11)

A)- 4 Channels with equal A- width, activated at the same time :



B)- 4 Channels with equal A-width, activated at different times:



C)- 3 channels with different A-width, activated at the same time :

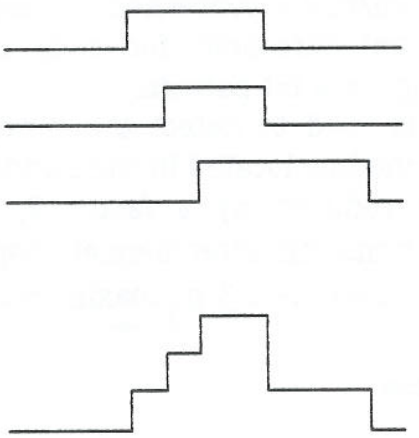


Fig. 13- Principle of the analog Multiplicity summation.

5- Maintenance.

Three types of components can be easily exchanged by the user (Fig. 13), i.e.:

- the eight double input comparators for the eight channels;
- the double Multiplicity comparator;
- the eight delay lines.

5.1- The comparators.

During an experiment, surge voltages may occur at the input of the FCC8 (due to an intense ionisation in the vacuum chamber caused by an accidental vacuum ascent for instance, etc) which are **capable of destroying the input comparator**. This component[6] is mounted on a socket and can be easily replaced.

The multiplicity comparator has the reference Double comparator HONNEWELL, type HCMP 9687 0. This comparator can be replaced by the SP 9687 DG-type, from PLESSEY.

5.2- Delay Lines.

The FCC8 are supplied with a delay line which should be chosen on ordering. It is possible to change the total line delay. You can consult us for advice on your choice.

[6] Double comparator, type SP 9687 DG, from PLESSEY.

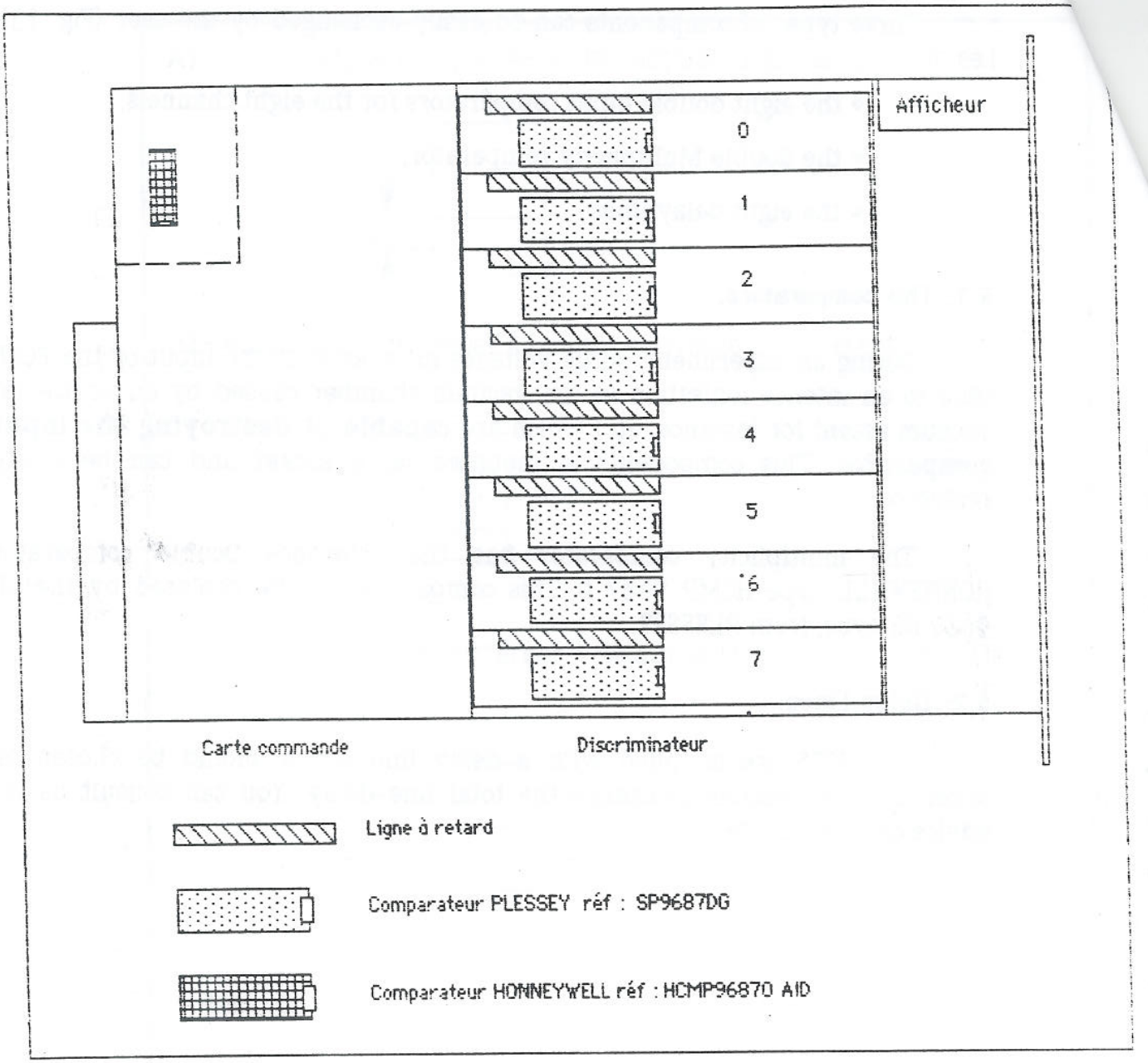


Fig. 14- Location of the components on the PC board, which can be replaced in case of trouble.

Figure caption