<b>JOERGER</b>	ENTERPRISES.	INC.	
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VISUAL SCALER
MODEL VS

#### WARRANTY

ALL EQUIPMENT MANUFACTURED BY JOERGER ENTERPRISES, INC. IS WARRANTED AGAINST DEFECTS IN MATERIAL AND WORKMANSHIP FOR A PERIOD OF ONE YEAR FROM THE DATE OF SHIPMENT. JOERGER ENTERPRISES, INC. WILL REPAIR OR REPLACE AT THEIR OPTION ANY EQUIPMENT DEFECTS FOUND IN WORKMANSHIP OR MATERIAL. THIS WARRANTY IS APPLICABLE TO THE ORIGINAL PURCHASER AND ONLY COVERS EQUIPMENT JUDGED BY JOERGER ENTERPRISES, INC. TO HAVE RECEIVED NORMAL AND PROPER USE.

ALL REPAIRS WILL BE PERFORMED AT THE JOERGER ENTERPRISES, INC. FACTORY. NO EQUIPMENT WILL BE ACCEPTED FOR REPAIR WITHOUT PRIOR APPROVAL BY THE FACTORY. EQUIPMENT MUST BE RETURNED PREPAID AND WILL BE RESHIPPED WITH TRANSPORTATION CHARGES COLLECT. THE WARRANTY ON EQUIPMENT RETURNED FROM OUTSIDE THE CONTINENTAL U.S.A. IS LIMITED TO REPAIR OF THE EQUIPMENT AND DOES NOT COVER SHIPPING, CUSTOMS CLEARANCE, OR ANY OTHER CHARGES.

ANY EQUIPMENT PURCHASED BY JOERGER ENTERPRISES, INC. FOR RESALE WILL CARRY ONLY THE ORIGINAL EQUIPMENT MANUFACTURERS WARRANTY.

EQUIPMENT THAT IS NO LONGER COVERED UNDER WARRANTY WILL BE REPAIRED AT COST. AN ESTIMATE OF THESE REPAIRS WILL BE SUBMITTED TO THE CUSTOMER AND AFTER RECEIVING HIS WRITTEN APPROVAL REPAIRS WILL PROCEED.

JOERGER ENTERPRISES, INC. DOES NOT ASSUME OR AUTHORIZE ANY OTHER PERSONS OR REPRESENTATIVES TO ASSUME ANY OTHER LIABILITIES IN CONNECTION WITH THEIR EQUIPMENT.

EVERY EFFORT WILL BE MADE TO REPAIR DEFECTIVE EQUIPMENT AS SOON AS POSSIBLE. A CLEAR DESCRIPTION OF THE MALFUNCTION ACCOMPANIED WITH THE UNIT WILL SPEED THE TURN-AROUND TIME.

#### MODEL VS

#### NIM, DUAL CHANNEL 150MHZ VISUAL SCALER

CHANNEL I

CHAN I

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CARRY

**(9)** 

JOERGER

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GATE

#### FEATURES:

- · HIGH COUNTING SPEED, 175MHZ MIN.
- EASY READING LED DISPLAYS
- INTERNAL TEST FEATURES
- LOW POWER CONSUMPTION

The Joerger Enterprises Inc. Model VS is a high speed scaler packaged in a double width NIM module. It contains two identical eight digit counters. Visual readout is provided on two eight digit LED displays. Character height is .375 inches and leading zero suppression is incorporated thus providing a very readable display. A gate light and overflow light are provided for each channel. Testing features are provided to test the displays (display all 8's) and also to test the counters. The counters are tested by switching on an internal test oscillator which injects a test signal into each channel. When the test oscillator is switched off the two channels should track within +1 count verifying correct operation. This test input is inserted after the counting gate so that the module may be tested in the presence of external inputs simply by gating off the scaler. A three position gate switch is provided to "Enable", "Disable", or allow the channel to be remotely gated by an external gate signal. Reset is accomplished either manually or externally, a carry output signal is provided for each channel.

# SPECIFICATIONS (Identical for each channel)

### INPUTS

Signal

Impedance
Pulse Repetition Rate
Pulse Pair Resolution

Sensitivity
Pulse Width

50 ohms +10% D.C. coupled 200MHZ typical, 175MHZ minimum

Less than 7nsec

-500mv 3nsec min.

Gate (bridged high impedance NIM input)

Impedance

5K ohms min.

Sensitivity

-500mv to gate channel off

Response Time

Less than 10ns

Reset (bridged TTL input, biased to logic "0", +2.5v min.)

Amplitude Logic "1", .5v max.

#### OUTPUTS

Carry Out (note carry out is inhibited during reset)

Amplitude

-700mv min., into 50 ohms

Pulse Width

250nsec typical

DISPLAYS

Data

Displayed on eight .375 LED displays with

leading zero suppression.

Gate

An LED is provided to indicate when the

counting gate is open.

Overflow

An LED is provided to indicate when that

channel has overflowed.

MANUAL CONTROLS

Gate

A three position switch is provided to open

(enable), close (disable), or allow gating from

an external input (remote).

Reset

A pushbutton is provided to reset each channel. This switch is also used to test the display.

When the switch is depressed all eights will

appear on the display.

Test

A test switch is provided that injects test signals into each channel after the counting

gate. Both channels should track during test

within +1 count.

POWER REQUIREMENTS

200ma reset condition

600ma both displays all eights, test mode

-6v 480 ma

+12v 285ma

SIZE

#2 NIM module

TEMPERATURE RANGE

00C to 500C

JEI0487

CIRCUIT DESCRIPTION (REFERENCE SCHEMATIC VS-200)

### COUNTER -

THIS IS A DESCRIPTION OF ONE (CHANNEL 1) OF THE TWO IDENTICAL COUNTING CHANNELS. THE INPUT IMPEDANCE OF 50 OHMS IS ESTABLISHED BY R1. RESISTOR R2 AND DIODES CR1 AND CR2 PROVIDE TRANSIENT PROTECTION AGAINST BOTH POSITIVE AND NEGATIVE TRANSIENTS. THE NIM INPUT LEVEL IS CONVERTED TO ECL LEVELS BY EMITTER FOLLOW Q1. THE SIGNAL IS THEN SHAPED IN 1C12-10, 11, 14, WHICH IS CONNECTED AS A SCHMITT TRIGGER WITH A THRESHHOLD OF APPROXIMATELY 200MV. THE SIGNAL IS THEN INVERTED IN IC12-12, 13, 15, WHICH ALSO PROVIDES ADDITIONAL SHAPING. THE SIGNAL AT 1012-15 IS NEGATIVE GOING AND IS DIFFERENTIATED AND GATED IN 1C11-9, 10,11. DIFFERENTIATION IS ACCOMPLISHED BY TAKING THIS NEGATIVE GOING SIGNAL, INVERTING AND DELAYING IT IN IC12-4,5,2 AND R10, C1 AND GATING IT WITH ITSELF. THIS HAS THE EFFECT OF ONLY ALLOWING THE LEADING EDGE OF THE PULSE TO PASS THROUGH AND DOES NOT SUFFER FROM HAVING A TRAILING EDGE PULSE ASSOCIATED WITH NORMAL DIFFERENTIATORS. THIS ALLOWS HIGHER SPEED TO BE ACHIEVED. GATING OF EACH CHANNEL IS CONTROLLED BY A GATE INPUT AND A GATE SELECTION SWITCH. THE SWITCH HAS THREE POSITIONS; ENABLE, DISABLE AND REMOTE. ENABLE OPENS THE COUNTING GATE AND DISABLE INHIBITS THE COUNTING GATE FROM PASSING INPUT SIGNALS. IN THE REMOTE POSITION, THE GATE IS CONTROLLED BY THE GATE INPUT SIGNAL. THIS SIGNAL IS APPLIED TO A BRIDGED PAIR OF LEMO CONNECTORS. THE INPUT IMPEDANCE IS HIGH SO THAT THESE CONNECTORS MAY BE "DAISY CHAINED" TO OTHER GATE INPUTS. GATE SIGNAL MUST BE TERMINATED IN 50 OHMS, HOWEVER, AND IF IT IS BEING BUSSED, THEN THE LAST POSITION SHOULD CONTAIN THE TERMINATION. GATE SIGNAL INPUT IS PROTECTED BY R15 AND CR3 AND 4. IT'S NIM LEVEL IS CONVERTED TO ECL LEVELS BY EMITTER FOLLOWER Q2. THIS SIGNAL IS EFFECTIVELY GATED BY THE DIFFERENTIAL INPUT OF IC12-6,7,3. SWITCH CONTROLS ONE BASE. IN THE ENABLE POSITION THE BASE IS BIASED AT -VE AND THE GATE SIGNAL HAS NO EFFECT. SIMILARLY, IN THE DISABLE POSITION THE BASE IS BIASED MORE POSITIVE THAN THE GATE SIGNAL CAUSING IT TO HAVE NO EFFECT. IN THE REMOTE POSITION, HOWEVER, THE BASE IS BIASED IN THE ACTIVE REGION OF THE GATE SIGNAL AND SO THE GATE SIGNAL CONTROLS THE COUNTING GATE. WHEN THE GATE INPUT (WHICH IS MORE ACCURATELY TERMED INHIBIT SIGNAL) IS HIGH, THE OUTPUT OF IC12-351S LOW, ENABLING THE COUNTING GATE IC11-11. WHEN THE GATE SIGNAL IS LOW THIS PUTS THE OUTPUT OF IC12-3 HIGH, DISABLING THE COUNTING GATE. VISUALLY INDICATE THE STATE OF THE COUNTING GATE A FRONT PANEL LED IS PROVIDED. THIS IS DRIVEN BY A DIFFERENTIAL AMPLIFIER Q3 AND Q4 WHICH SENSES THE OUTPUT OF IC12-3.

THE OUTPUT OF THE COUNTING GATE IS "ORED" WITH THE TEST SIGNAL IN IC11-4,5,2. THE TEST SIGNAL IS DERIVED FROM AN OSCILLATOR USING IC22. THIS OSCILLATOR IS APPROXIMATELY 3MHZ AND IS CONTROLLED BY THE FRONT PANEL TEST SWITCH. A FLIP-FLOP IS PROVIDED FOR THE SWITCH TO ELIMINATE CONTACT BOUNCE AND THUS INSURE A CLEAN, RELIABLE PULSE TRAIN. BECAUSE THE TEST SIGNAL ENTERS THE COUNTER AFTER THE COUNTING GATE, THE UNIT CAN BE TESTED IN THE PRESENCE OF EXTERNAL INPUTS BY INHIBITING THE INPUTS. THIS IS AN IMPORTANT FEATURE AND ALLOWS TESTING WITHOUT REMOVING THE INPUT CABLES.

THE OUTPUT OF IC11-2 THEN GOES TO THE FIRST BCD DECADE MADE UP OF IC'S 10 AND 21. THESE ARE EACH DUAL HIGH SPEED FLIP-FLOPS GATED IN SUCH A WAY SO AS TO COUNT IN BCD. THE OUTPUT OF EACH OF THE FOUR ECL STAGES IS CONVERTED TO TTL LEVELS. FOR BITS 1, 2, AND 4, THIS IS DONE SIMPLY BY BIASING THE ECL LEVELS POSITIVE IN A RESISTOR NETWORK THAT DRIVES THE BASE OF A TRANSISTOR (Q9, 10, 11). BECAUSE BIT 8 MUST BE USED TO DRIVE THE NEXT DECADE IT'S SPEED AND WAVESHAPES ARE IMPORTANT. A CURRENT MODE SWITCH (Q12, 13) IS PROVIDED FOR THIS WHICH IS DRIVEN BY THE Q AND Q OF BIT 8. IT'S OUTPUT IS USED TO TRIGGER THE NEXT DECADE, IC8. THE REMAINING SIX DECADES ARE CONNECTED AS A RIPPLE THE OUTPUT OF THE LAST DECADE, IC2, IS DIFFERENTIATED AND USED TO TRIGGER THE OVERFLOW FLIP-FLOP IC1. IT IS ALSO USED TO GENERATE THE CARRY-OUT SIGNAL AFTER BEING GATED WITH THE RESET PULSE IN IC1-4,5,6. THIS INSURES THAT DURING RESET A CARRY-OUT IS NOT ERRONEOUSLY GENERATED. THE OUTPUT OF THIS GATE IS USED TO DRIVE A CURRENT MODE SWITCH (Q19,20) WHICH GENERATES A HIGH SPEED CURRENT OUTPUT PULSE OF APPROXIMATELY 250NSEC. A VISUAL OVERFLOW INDICATION IS PROVIDED WHICH SENSES THE STATE OF THE OVERFLOW FLIP-FLOP AND DRIVES A FRONT PANEL LED VIA Q21.

THE COUNTER MAY BE RESET EITHER ELECTRICALLY OR MANUALLY. A TTL LEVEL INPUT IS USED TO RESET THE CHANNEL. IT IS VIASED TO A LOGIC "O" (HIGH) BY PULLUP RESISTOR R26. RESISTOR R27 AND DIODES CR5 AND 6 PROVIDE TRANSIENT PROTECTION. THIS SIGNAL IS "ORED" WITH THE MANUAL RESET INPUT IN IC9-1,2,3. THE MANUAL RESET IS TRIGGERED BY A FRONT PANEL PUSHBUTTON SWITCH. A FLIP-FLOP IS PROVIDED TO ELIMINATE CONTACT BOUNCE. THE OUTPUT OF THE OR GATE TRIGGERS A MONOSTABLE MULTIVIBRATOR, IC41. IT'S OUTPUTS ARE USED TO RESET THE COUNTERS AND THE OVERFLOW FLIP-FLOP. IN ADDITION, THE RESET SIGNAL ALSO TESTS THE DISPLAYS. DURING RESET ALL EIGHT DIGITS ARE FORCED TO DISPLAY ALL 8'S, WHICH TESTS ALL SEGMENTS OF THE DISPLAYS.

### VISUAL DISPLAY

THE VISUAL DISPLAY FOR EACH CHANNEL IS PRESENTED ON AN EIGHT LED DECIMAL READOUT. THE DISPLAYS ARE DRIVEN WITH A MULTIPLEXING TECHNIQUE SO THAT IN EACH CHANNEL EACH DIGIT IS ON FOR 1/8 OF THE TOTAL TIME. THE CLOCK USED FOR CONTROL IS A FREE RUNNING OSCILLATOR (IC32) OF APPROXIMATELY 4KHZ. THIS CLOCK DRIVES A 3 BIT BINARY COUNTER IC30. IT'S THREE OUTPUTS ARE DECODED IN IC31 TO PROVIDE EIGHT OUTPUTS SEQUENCED IN TIME. EACH OUTPUT ACTIVATES ONE DECADE FROM EACH CHANNEL. THE DECADE IS ACTIVATED BY ENABLING IT'S FOUR OUTPUTS IN AN OPEN COLLECTOR GATE. THE OUTPUTS OF THESE GATES FOR THE EIGHT DECADES ARE WIRE "ORED" TO A COMMON SEVEN SEGMENT DECODER IC23. AT THE SAME TIME AS A DECADE IS ENABLED, IT'S CORRESPONDING DISPLAY IS ENABLED. THE DISPLAY IS ENABLED BY GROUNDING IT'S COMMON ANODE INPUT PIN 1,6. THE DATA FROM THE DECADE IS DECODED AND DRIVES IT'S SEVEN SEGMENTS VIA TRANSISTOR DRIVERS Q33-39. IN THIS WAY EACH DIGIT IS STEPPED THROUGH, BEING ENERGIZED IN TURN.

TO MAKE THE DISPLAY MORE READABLE, LEADING ZERO SUPPRESSION HAS BEEN ADDED. THIS IS ACCOMPLISHED BY MONITORING THE DATA FROM THE DECADES ON THE BUS. THE DECADES ARE ENABLED STARTING WITH THE MOST SIGNIFICANT DIGIT GOING TOWARD THE LEAST. THE FOUR BITS ARE "ORED" IN 1C25-1,2,4,5. WHEN THE FIRST NON-ZERO DECADE IS DETECTED, A FLIP-FLOP (1C27) IS SET UNBLANKING THE DISPLAY. THE FLIP-FLOP IS RESET WITH THE LSB DIGIT AFTER THE COMPLETION OF EACH CYCLE. UNBLANKING IS CONTROLLED BY OR GATE 1C25-9,10,12,13. IN ADDITION TO THE NORMAL CYCLE, THERE ARE 3 OTHER INPUTS THAT WILL UNBLANK THE DISPLAYS. THE DISPLAY IS ALWAYS UNBLANKED FOR THE LSB DIGIT TO GIVE SOME ASSURANCE OF THE DISPLAY. THE DISPLAY IS

ALSO UNBLANKED WITH THE OVERFLOW FLIP-FLOP. THIS IS TO INDICATE AN OVERFLOW HAS OCCURRED AND HAS IN EFFECT BECOME THE MOST SIGNIFICANT BIT. THE THIRD WAY THE DISPLAYS ARE UNBLANKED IS TO TEST THEM. THIS IS DONE WITH THE RESET COMMAND. WHEN THE UNIT RECEIVES A RESET, MANUALLY OR ELECTRICALLY, THE DISPLAYS ARE UNBLANKED AND ALSO FORCED INTO DISPLAYING ALL 8'S. THIS IS DONE BY USING THE TEST INPUT OF THE DECODER IC23.

EXTENSIVE USE OF LOW POWER IC'S HAS BEEN INCORPORATED IN THIS UNIT. IN ADDITION, IC POWER HAS BEEN TAKEN FROM BOTH +6 AND +12 VOLTS TO MAKE MAXIMUM USE OF POWER AVAILABLE IN THE CRATES. THIS HAS PRODUCED A UNIT THAT CAN BE USED IN ANY 6 VOLT NIM BIN WITH THE BIN POWERING SIX OF THESE UNITS. THE -6 VOLTS IS USED FOR THE HIGH SPEED FRONT END WHICH IS ECL. THE +6 VOLTS IS USED TO POWER THE DISPLAY LOGIC AND DRIVE THE LED DISPLAYS. THE +12 VOLTS IS REGULATED TO +5 VOLTS BY Q55 AND DRIVES BOTH COUNTER CHANNELS.

# PARTS LIST

# MODEL VS

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PC BOARD #VS-200	REFERENCE DESIGNATION	DESCRIPTION
INTEGRATED	IC 1,44,9,52 IC 2-6, 45-49 IC 7,8,50,51 IC 22 IC 10,21,42,54 IC 11,43 IC 12,55 IC 13-20, 34,40, 53 IC 23,29 IC 24,26,32,33 IC 25,28 IC 27 IC 30 IC 31 IC 41	SN74LS00 SN74LS90 SN74LS196 SN7400 MC10131P MC10105P MC10115P SN74LS03 SN74LS47 SN74LS04 SN74LS04 SN74LS20 SN74LS02 SN74LS197 SN74LS197 SN74LS155 SN74LS123
TRANSISTORS	Q 1,2,5,6,12,13,17,18 Q 3,4,7-11,14-16,19-32 Q 33-39,48-54 Q 40-47 Q 55	2N3563 2N5134 2N5139 2N3641 2N3053
DIODES	CR 1-4,6-10,12 CR 5,11 CR 13 CR 14,15	1 N91 4 1 N748 1 N5234 1 N4001
INDUCTORS	L 1,2	.47ин
CAPACITORS	C 1,7 C 2,3,8,9,11,12,15,19,20,22-34 36,37,38,40-46,48-53 C 4-6,10,14,16,18 C 13,17 C 21,35,39,47,54,55	10PF .1UF 470PF 220PF 4.7UF
RESISTORS (ALL W, 10% UNLESS OTHERWISE SPECIFIED)	R 1,2,39,40 R 3,17,41,56 R 4,18,34,36,43,58 R 5,44,161-168 R 6,15,22,45,44,61,117,137 R 7,9,11,12,13,21,47,48,50-52,60,70-75,104-109 R 10-49 R 14,53,119,121,130,142,145,148,151,154,157,160,171,174,177,	51, 5% ½W 33K 560 68 220 680 22
	180,183,186,189 R 16,30-33,54,65,66,82-84,90,93, 95,97 R 19,57	100 10k 390

# PARTS LIST MODEL VS CONTID.

	REFERENCE DESIGNATION	DESCRIPTION
RESISTORS CONTID.	R 20,25,37,59,69,114,134 R 23,62,85,87,99,103,113,139 R 24,68 R 26,63,111,112,132,133,141,144,	1.5к 330 2.7к
	147,150,153,156,159,170,173, 176,179,182,185,188 R 27,29,64,88,110,120,131,140, 143,146,149,152,155,158,169, 172,175,178,181,184,187,192,	4.7ĸ
	193 R 28,67 R 35,115,116,135,136	1к 6.8к 3.3к
	R 38,76-78,89,91,100-102,118, 122-129,138 R 79-81,92,94,96 R 86,98 R 190 R 191	2.2K 5.6K 470 15,2W 10
DISPLAYS	I 1-4 D 1-16	T1L209 FND70
CONNECTORS	J 1-12	LEMO RA00250
SWITCHES	SW 1,4 SW 2,5 SW 3	C&K 7103K C&K 8121P C&K 7101K