MODEL 222/222N

DUAL GATE GENERATOR

May,1989

(ECO 1012)

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

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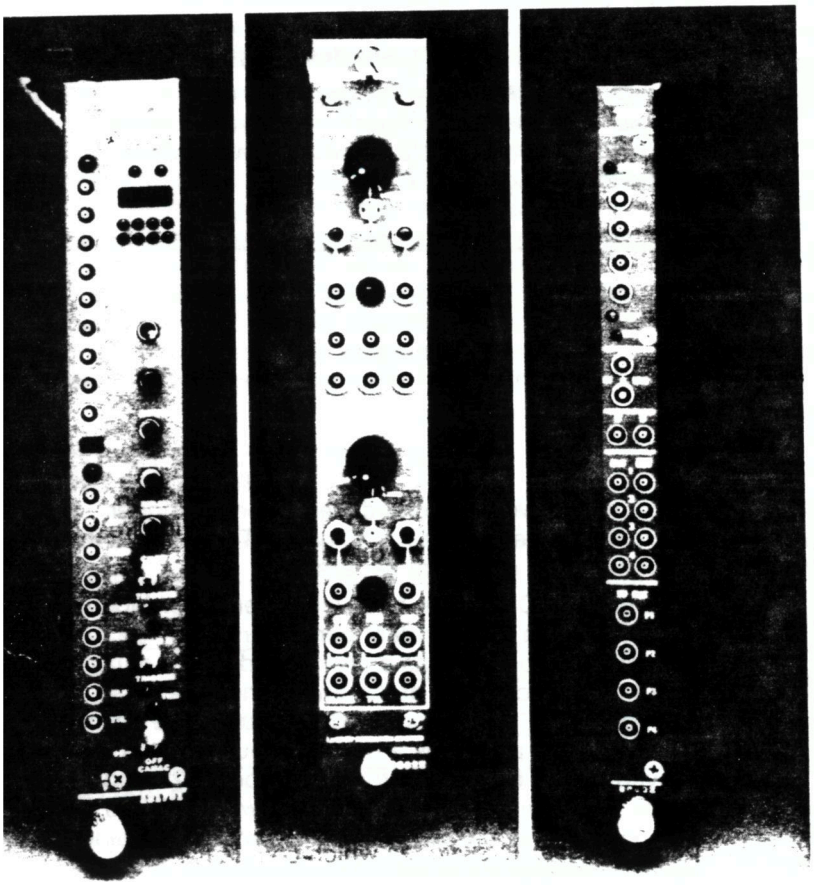


- **Gate, Delay and Delayed Gate Functions**
- **High Precision, Wide Range**
- **NIM and CAMAC Packaging**
- **NIM, TTL, and ECL Level Compatibility**
- **Minimum Deadtime**
- **Manual and CAMAC Programming Options**

PRECISE TIME PERIODS GENERATED

Gate and Delay Generators are designed to provide precisely timed logic windows and level transitions. Applications employing Gate and Delay Generators may require that a logic transition occur immediately and have a given duration. Others require that a delay elapse prior to the logic transition, or that a precise gate be generated after some fixed delay. All these functions of Gate Generator, Delay Generator, and Delayed Gate Generator are performed by any LeCroy Gate and Delay Generator module.

FEATURES

Versatile Product Family— Two of the most popular modular instrumentation standards used are NIM and CAMAC. Continuous manual control and high resolution programmable digital delay adjustment are selected by choice of Modules.

Minimum Deadtime— Any of these Gate and Delay Generators may be retriggered immediately after the delay has elapsed.

Delayed Outputs— At the end of any gate, a delayed output issues a pulse.

Independent Gate and Delay Functions— Each LeCroy Gate and Delay Generator provides precision gate lengths which can be used as a precision delay as well. Since each unit has at least two such gate generators, one can be used as a delay which starts the second generator that provides the gate signal.

Wide Dynamic Range— Ranges from under 100 nsec to 10 sec are provided by either the Model 222 or 2323A. Model 4222 maintains 1 nsec resolution up to its range of 16.7 msec.

FUNCTIONAL DESCRIPTION

LeCroy Gate and Delay Generators allow both manual and CAMAC programmability for gate durations ranging from a few nanoseconds to several seconds. NIM Standard compatibility is provided by the Model 222 while CAMAC IEEE-583 (See LeCroy Application Note AN-33) is employed for the Models 2323A and 4222.

Each of these modules has its own unique advantages that enhance its service in certain applications. For example, Model 222 has manual pushbuttons for Start and/or Stop. When a "trigger" is not available, these may be used to simulate missing signals. Model 2323A has an ECL output for compatibility with LeCroy ECLine trigger processor and data handling modules. Model 4222 has four time generators in a single-width module, making it a superior choice in high density systems where space is at a premium.

Arbitrary gate widths are provided for in the Models 222 and 2323A via a latch-mode operation where the gate duration is determined by externally applied Start and Stop signals. Further versatility is incorporated into these modules by including a delayed output pulse which occurs at the end of each gate output pulse and has a preset width.

Precision delayed gates can be produced with any LeCroy Gate and Delay Generator Module. Gate signals can be used to set coincidence time windows, provide veto signals, or generate fast clear signals after some preset delay. Latch Mode operation, available in either the Model 222 or the Model 2323A, permits gating-off front-end electronics after receipt of a valid trigger signal and maintaining this state until data acquisition is complete. For example, discriminators may be vetoed immediately after the trigger electronics generates the ADC gates. This insures that no further ADC gates are generated.

Since each LeCroy Gate and Delay Generator Module has at least two independent generators, one generator can be used as a precision delay. A delayed output pulse, occurring at the end of the gate pulse, is applied to the Start of a second generator. The second generator then produces a precision pulse that is delayed by the first generator. Both Model 222 and Model 2323A may be configured this way. Delayed gate operation of the Model 4222 is provided by side-panel accessible switches which couple two channels together, providing either one or two such generators.

NIM MODEL 222

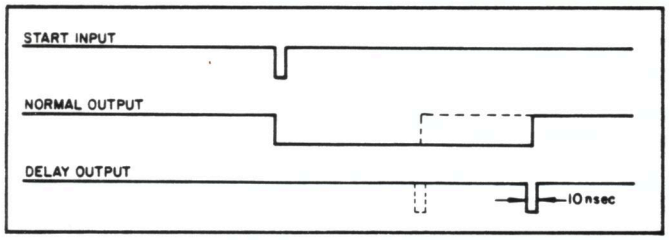
The LeCroy Model 222 Dual Gate and Delay Generator provides two complete delay/gate channels in a single NIM module. This combines many important features formerly requiring separate expensive circuits into one compact package.

The Model 222 eliminates the problems exhibited by previously available gate generators. There is negligible recovery time associated with the unit at any width setting; it may be retriggered immediately after the gate returns to its quiescent state in all ranges. Each channel of this single module can also be used to provide delays and gate outputs and to drive bin gates in its own NIM bin (LeCroy Model 1403) and

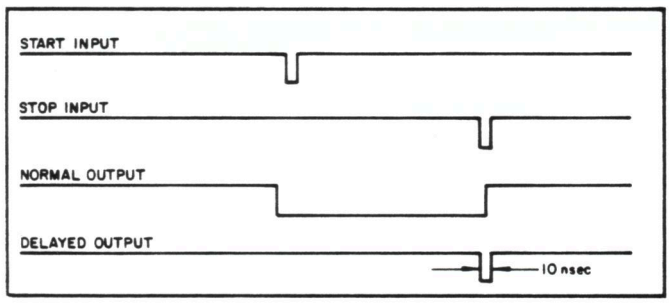
several external bins. In addition, an OR input for each channel permits the gate and delay interval to be extended by an external input.

The Model 222 provides a range switch and a screwdriver-adjustable potentiometer to permit continuous adjustment of gate durations from less than 100 nsec to greater than 11 seconds. A front-panel LED remains on when gate output is present, even if extended by the OR input. The approximate gate setting may be easily determined without an oscilloscope by means of the front-panel monitor point, which provides a DC voltage related to the gate duration. A conversion graph is enclosed with the unit. In addition to preset width ranges, the range switch has a "Latch" position to provide a continuous gate controllable by either the "Start" and "Stop" inputs or by the "Start" and "Stop" pushbuttons. Front-panel "Start" and "Stop" pushbuttons permit manual operation when full scale switch is set on "latch", and single-shot presettable operation when full scale switch is in any other position.

MODEL 222 DUAL GATE GENERATOR
TIMING DIAGRAMS



PRESETTABLE WIDTH MODE



LATCH MODE

Each channel has one rear-panel Lemo connector that drives external bins using either normal or inverted logic (switch selectable). A rear-panel 3-position switch (A/B/OFF) determines which channel drives the bin in which the Model 222 is located.

CAMAC MODEL 2323A

LeCroy's CAMAC Model 2323A is a fully programmable Gate and Delay Generator packaged with 2 channels in a double-width CAMAC module. Its Gate duration is programmable over the range 100 nsec to 10 seconds, covering a dynamic range of eight orders of magnitude. Moreover, outputs as short as 50 nsec can be selected at the expense of accuracy and stability. All settings may be programmed under CAMAC control or via front-panel controls. The settings of the instrument are battery backed-up, so the unit does not have to be reprogrammed after turning the crate off/on or after a power failure. The Model 2323A offers excellent stability and jitter properties with 0.2% of Full Scale accuracy in the gate setting.

The Model 2323A offers both Start and Stop inputs. This allows the output pulse width to be determined by the Start-Stop time difference in the latched mode or by the internal timer in the preset mode. A Blanking NIM input causes a notch to be taken out of the gate, equal in duration to the Blanking input. This is especially useful to gate off data acquisition during spurious periods. Conversely, a NIM OR input causes all outputs to be set to True for the duration of the OR inputs.

The unit offers NIM and NIM outputs equal in duration to the gate width selected. In addition, a DELAY output is produced at the trailing edge of the Gate pulse. The Model 2323A also provides a differential ECL output and a TTL output capable of driving a NIM Bin Gate. Both the ECL and TTL outputs may be driven from either the Gate or Delay circuit. These options are selected by board-mounted shorting plugs.

The Gate duration and the width of the Delayed output are both programmable under CAMAC control. Each of the two channels are programmed independently. All values which are loaded into the Model 2323A may also be read back via CAMAC. Programming the delay involves a 10-bit "mantissa" and a 3-bit "characteristic".

The Start input is normally configured to accept NIM signals. A bridged high impedance input is employed to allow the trigger of more than one channel of 2323A. The front end of the Start input consists of a comparator circuit, factory adjusted to trigger at – 400 ±50 mV. A front-panel accessed multiple turn potentiometer allows the user to adjust the threshold over the range – 3 V to + 3 V. This allows the unit to be triggered by NIM, ECL, TTL or other standard logic signals. A front-panel accessed switch selects either the positive-going or negative-going edge as the trigger. The stop input accepts NIM standard pulses.

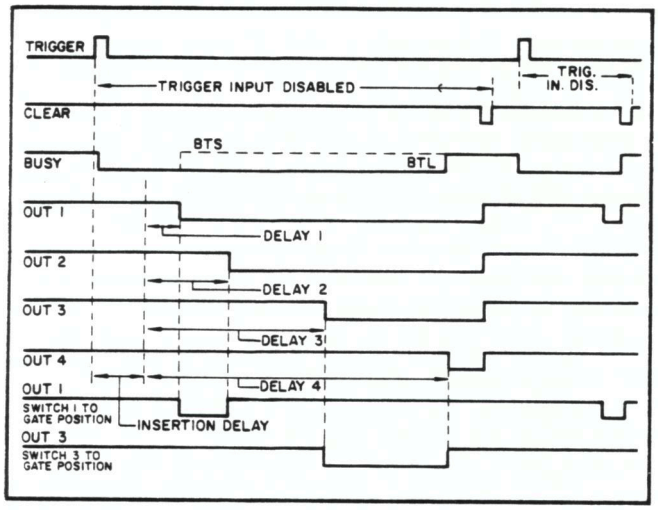
Timing diagrams for the Model 2323A are similar to those of the Model 222.

CAMAC MODEL 4222

The LeCroy Model 4222, Quad, Wide Range, Gate and Delay Generator, produces long, precise time delays and time intervals synchronously with a random Trigger input. All 4 channels of the Model 4222 are started by a common Trigger input. Each channel provides a programmable time delay of up to 16.7 msec in 1 nsec increments. All programming is under CAMAC control.

Three outputs are provided for each channel. One output provides NIM-level signals which go "True" after the programmed time delay and is reset by the Clear. Another output gives complementary NIM logic output. Each channel has a corresponding delayed pulse output that provides a 5 V fast risetime signal into 50 Ω occurring after the programmed time delay.

MODEL 4222 TRIGGER TIMING DIAGRAMS

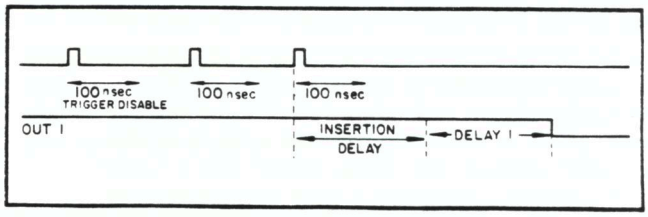


NON-RETRIGGER MODE

(RETRIGGER ACTION switch: SET TO RETRIGGER DISABLED)

The Model 4222 may be set to Retrigger Mode (side switch selectable) permitting the unit to retrigger without being reloaded. In Retrigger Mode, a second side switch permits two options:

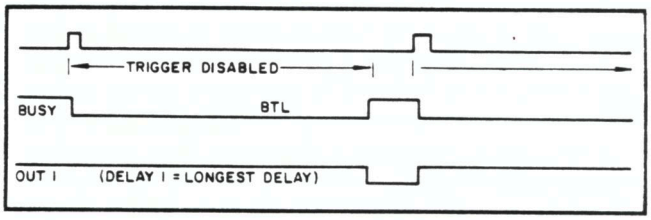
The unit may be retriggered any time 100 nsec after the last trigger, or any time after the longest delay has elapsed.



RETRIGGER BEFORE END OF DELAY

(RETRIGGER ACTION switches: SET TO RETRIGGER ENABLED RETRIGGER BEFORE END)

Synchronization of many Model 4222 Gate and Delay Generators is possible. An external clock may be used to feed several Model 4222 modules with an identical time base. Stability and accuracy are then determined by the external clock.



RETRIGGER AFTER END OF DELAY

(RETRIGGER ACTION switches: SET TO RETRIGGER ENABLED RETRIGGER AFTER END)

CAMAC COMMANDS AND FUNCTION CODES

Model 2323A Dual Programmable Gate and Delay Generator

CAMAC Commands:	**C or Z:**	Stops channels A and B gates.
	X:	X response is generated for each valid function.
	Q:	Q response is generated for each valid function unless otherwise specified.
CAMAC Function Codes:	**F(1)•A(0):**	Read channel A programming word.
	F(1)•A(1):	Read channel B programming word.
	F(9)•A(0):	Stop channel A gate.
	F(9)•(1):	Stop channel B gate.
	F(17)•A(0):	Write channel A programming word.
	F(17)•A(1):	Write channel B programming word.
	F(25)•A(0):	Start channel A gate.
	F(25)•A(1):	Start channel B gate.

Model 4222 Quad, Wide Range Gate and Delay Generator

CAMAC Commands:	**Z:**	Initializes module, resets all channels, disables trigger input and enables CAMAC access (does not reset data registers).
	C:	Resets all channels (does not reset data registers), equivalent to front-panel Clear input.
	I:	Disables trigger input when present.
	X:	X response is generated for each valid function.
	Q:	Q response is generated for each valid function unless otherwise specified.
CAMAC Function Codes:	**F(0)•A(0-3):**	Reads selected programmed delay for channels 1-4 in 24 bits; Q = 1 always; 24-bit unsigned integer convention.
	F(1)•A(0):	Reads status via Read Lines 1-4: R1 = 1 if shortest delay elapsed; R2 = 1 if longest delay elapsed; R3 = 1 if Model 4222 is ready for trigger; R4 = 1 if CAMAC access enabled. All states are strobed by the leading edge of the CAMAC N signal.
	F(9)•A(0):	Resets all channels (does not reset data registers) equivalent to external Clear input.
	F(16)•A(0-3):	If CAMAC access enabled, writes delay to selected channel 1-4 in 24 bits. Q = 1 if CAMAC access enabled; Q = 0 otherwise. 24-bit unsigned integer convention.
	F(24)•A(0):	Disables unit; enables CAMAC access.
	F(25)•A(0):	Triggers the unit (OR'd with the external front panel Trigger input): Q = 1 if unit was ready for Trigger; Q = 0 otherwise.
	F(26)•A(0):	Enables unit; disables CAMAC access.

TECHNICAL INFORMATION

MODEL	222	2323A	4222
General			
Packaging	Single-Width NIM	Double-Width CAMAC	Single-Width CAMAC
START Input:	NIM or TTL	−3 V to +3 V	−1.5 V to +1.5 V
STOP Input:	NIM	NIM	NIM (Clear input)
GATE WIDTH			
Range:	100 nsec to 11 seconds or Latch Mode	100 nsec to 10 seconds or Latch Mode	1 nsec to 16.777215 msec
Jitter:	0.05% of setting	<0.3% of setting	150 psec RMS max.
Accuracy:	—	±0.2% of full scale	±200 psec ±time base error
Resolution:	continuous	0.1% of full scale	1 nsec
Input to Ouput Delay:	14 nsec	24 nsec	170 nsec typical
DELAYED OUT			
Width:	10 nsec	10, 30, 100 or 300 nsec	100 nsec ±10%
Occurs:	Approximately at trailing edge of gate signal	Trailing edge of gate pulse	At end of delay
Risetime:	2.5 nsec max.	2 nsec max.	1 nsec
Signal:	NIM into 50 Ω	NIM (−16 mA)	5 V into 50 Ω
ADDITIONAL OUTPUTS			
TTL:	Quiescent 0 V; >+2.5 V into 50 Ω during pulse.	FET open drain output (+35 V Max, 250mV, 0.5W Max)	—
ECL:	—	Differential ECL (−0.8 V and −1.6 V)	—
TTL/ECL:	Selectable by internal jumpers to correspond to either the NIM or DELAYED outputs or their complements.		
GENERAL			
Power Consumption:			
24 V	+45 mA/−80 mA	+50 mA/−75 mA	+40 mA/-130 mA
12 V	+95 mA/−180 mA	—	—
6 V	+235 mA*/−0 mA	+1.8 A/−1.3 A	+1.3 A/−2.5 A
	7.7 W	21.6 W	26.9 W

*Taken from +12 V if +6 V unavailable.

SECTION I

SPECIFICATIONS

1.2 Input Characteristics

1.2.1 START and STOP Inputs

The START and STOP inputs respond to either fast NIM* or TTL level inputs. Since the Model 222 input circuit automatically responds to either type of signal, no switch selection or internal change is necessary. A fast NIM input drives an impedance of 50 Ω, however the input is high impedance for TTL levels. A TTL input requires 5 mA at +2.5 V, increasing slightly as the input voltage is increased (i.e., 5.75 mA at +3.5 V). Protection is provided for currents of up to ±5 A for 1 μsec by a 47 Ω series-terminating resistor, clamping at 0 V for negative pulses and at +6 V for positive pulses.

It is important to note that the STOP input (or STOP pushbutton) is only intended for use with the FULL SCALE WIDTH switch in the LATCH mode. However, if a Stop is applied while an output is present with the FULL SCALE WIDTH switch set at a finite range, the output pulse will nevertheless be terminated, but only after a short delay.

1.2.2 BLANK Input

The BLANK input responds to fast NIM level* inputs. Input impedance is 50 Ω and input protection extends to at least ±5 V. The blanking input suppresses only the portion of the Model 222 output pulse occurring during the blanking interval. The delayed output pulse is also suppressed on the standard unit.

1.2.3 OR Input

The OR input responds to fast NIM level* inputs, has a 50 Ω impedance, and is protected to at least ±5 V. Its specific function is to enable the user to easily extend the preset output width on the basis of external criteria, (e.g., extending an input inhibit to scalers or other data acquisition modules while a computer readout is still in progress).

* Fast NIM Levels:	−12 mA	{ Logical 1 {	−36 mA
TTL Levels:	+2.0 V	{ Logical 1 {	+5.0 V

1.3 Output Characteristics

1.3.1 Gate Outputs

General:

The Model 222 provides one standard fast NIM level output (quiescently 0 V, -750 mV during pulse) of approximately 2 nsec risetime, one complementary fast NIM level output (quiescently -750 mV, 0 V during pulse), and one TTL level output (quiescently 0 V, <+2.5 V into 50 Ω during pulse). The falltime of the fast NIM outputs is generally similar to the risetime, except at large output widths where the Model 222 timing stage causes a slight degradation of the falltime.

Gate Durations:

Preset output durations extend from <100 nsec to >11 sec and are determined by a combination of the FULL SCALE WIDTH selector switch and the screwdriver-adjustable vernier. On the BNC version (Model 222N), a lock-in potentiometer replaces the switch and vernier, giving direct visual indication of output width setting. On the LEMO Model 222, a DC level available at the front panel test point gives an indication of the output width setting as a percentage of the FULL SCALE WIDTH switch setting, from approximately 10% to 110%. The conversion chart representing this test point output is shown in Fig. 1.1.

When the output width range selector switch is set in the LATCH position, the output width of the Model 222 is determined by either the START and STOP pushbuttons, or the START and STOP inputs. Once "started", the Model 222 output will stay on indefinitely until "stopped" or until power is turned off.

1.3.2 Delayed Output

The delayed output (DEL) delivers a 10 nsec FWHM (Full Width Half Maximum) fast NIM level signal into 50 Ω. The leading edge of this output occurs shortly before the trailing edge of the normal gate output pulse. In other words, its leading edge occurs a few nsec before the normal gate output is fully completed.

The delayed output is normally suppressed by the BLANK input, but this feature may be disabled by factory option. This output is often useful for creating a "delay and gate generator" using two channels of the Model 222. In this case, either the delayed output or the complementary output of Channel 1 can be fed into the START input of Channel 2 of the Model 222 to create an output pulse of specified width occurring at a time determined by the output width setting of Channel 1. More standard applications involve using the delayed output to trigger a computer readout cycle, as a reset pulse, or as a "flag" pulse to indicate the completion of a data acquisition interval.

1.3.3 Bin Gate Driver Outputs

For Remote Bins:

The Model 222 provides a rear panel LEMO connector output which switch-selectably drives external bins in either the normal or inverted direction. For the normal direction, the Model 222 will clamp 200 mA for a Logical 1 (less than 1 volt). A Logical 0 is a high-impedance open-collector-type output. A 2 kΩ resistor provides pull up to +5.2 V.

NOTE: The NORMAL position disables the driven bin for the duration of the Model 222 output. The INVERTED position enables a normally disabled bin during the gate output interval.

For Driving the Local Bin:

Either Channel 1 or Channel 2 of the Model 222 can drive the bin from which the unit is powered. A rear panel 3-position switch selects which channel, with the third position (OFF) available to disassociate the local bin from the influence of the Model 222. The NORMAL position serves to disable the driven bin for the duration of the Model 222 gate output.

1.4 Recovery Time

With the Model 222, it is possible to get a second gate output immediately after the first gate output. In this respect, no delay period (deadtime) is required before the Model 222 can be retriggered. This feature is made possible by the OR'ing of two internal signals to create one output signal with a width corresponding to the front panel rotary switch setting and vernier.

1.5 BUSY Indicator

The Model 222 provides a front panel LED (light-emitting diode) indication when a gate output is present. This LED lights whenever an output is present, even if extended by an OR input. Because no mechanism is provided to slow down the turning on and off of the LED for each gate output, at short output widths or high rates, the LED will appear to the eye as a steady "on" condition.

1.6 Packaging

The Model 222 is packaged in a standard NIM module conforming to the standards outlined in AEC-NIM Report TID 20893, Rev. 3. The LEMO connector version has a #1 front panel width, while the BNC version utilizes a #2 width due to the size of the front panel lock-in potentiometer and the BNC connectors.

1.7 Current Requirements

The Model 222 dissipates 7.5 watts and requires the following NIM voltages and currents:

-24 V at 80 mA
-12 V at 160 mA
+ 6 V at 235 mA*
+12 V at 95 mA*
+24 V at 45 mA

* It is important to note that the Model 222 will automatically draw an additional 235 mA from the +12 V supply if +6 V is unavailable. For this reason, a +6 V NIM bin is NOT necessary to power the Model 222. When only the +12 V supply is a %%%

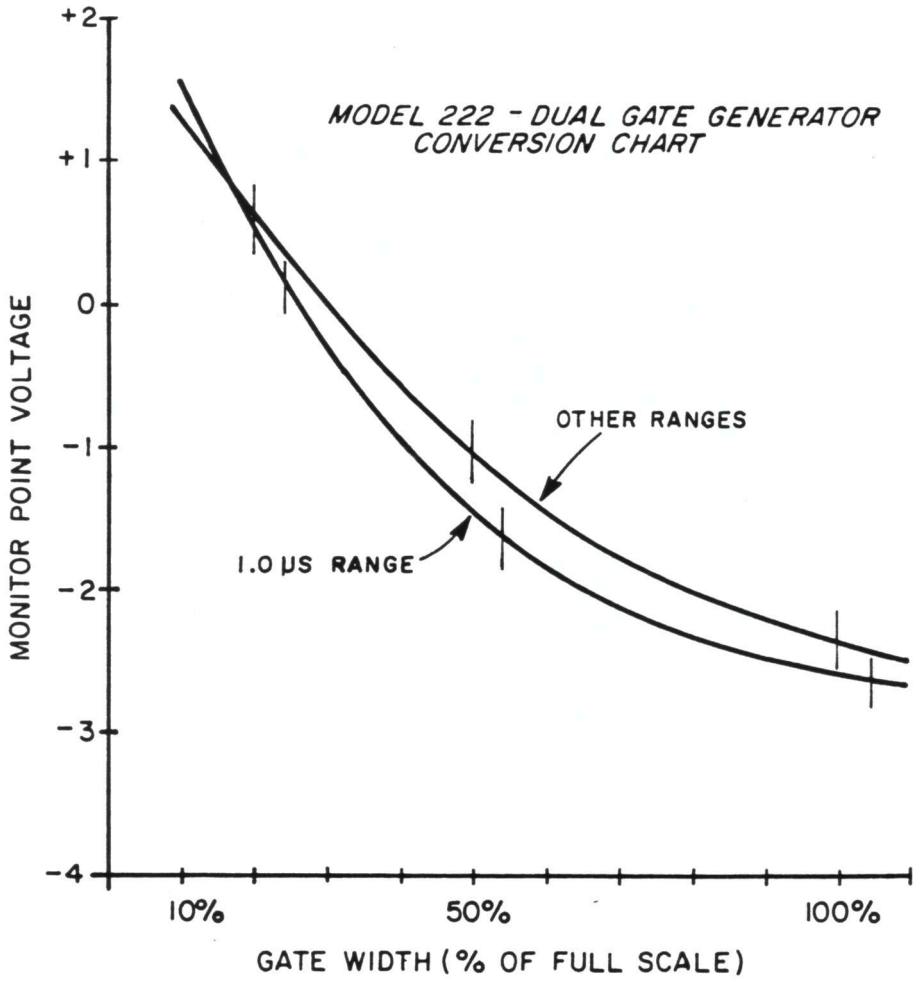

MODEL 222 - DUAL GATE GENERATOR
CONVERSION CHART
+2
+1
0
-1
-2
-3
-4
MONITOR POINT VOLTAGE
OTHER RANGES
1.0 µS RANGE
10%
50%
100%
GATE WIDTH (% OF FULL SCALE)

Figure 1.1

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 General

The Model 222 is a two-channel NIM module. It can be divided into three major sections:

The Start-Stop, Latch and OR'ing stages
The Ramp and Ramp Level Detector stages
The Output and Blanking stages

Each of these will be discussed briefly. The reader should refer to the circuit schematic (located in the rear pocket of this manual), the functional block diagram (Figure 2.1) and the timing waveform diagrams (Figure 2.2).

2.2 START-STOP, Latch and OR'ing Stages

The Start and Stop input stages are identical. Each is composed of a special input stage capable of accepting a low-impedance NIM input (-500 mV into 50 Ω) or a high-impedance TTL input (+2.5 V at 5 mA) using the same input connector. This is accomplished by requiring the input NPN transistor to provide a low-impedance path for negative signals and routing the input current of the negative input signal to the inverting input of the MC10115 receiver, causing it to go low. The same effect is accomplished with a positive input pulse, which turns off the input PNP transistor, enabling the 2 kΩ resistor on the MC10115 to pull the input low. A third method of causing a Start or Stop is via the respective pushbutton which, when depressed, causes circuit operation similar to that for the positive input.

When the inverting input of either the Start or Stop receivers (MC10115) is pulled more negative than the non-inverting input, the output will go high. Even for slow marginal inputs, the output is fast due to both AC and DC positive feedback to the non-inverting input.

From this point on, the Start differs from the Stop. The Start is first differentiated and the resulting "leading-edge" pulse is shaped by an emitter-coupled logic (ECL) receiver (which is inhibited if the Ramp section is already busy). The resulting pulse is then used to set the Latch, (composed of a heavily fed-back section of ECL receiver), by forcing the Latch output positive. (See "Presettable Width Mode" timing diagram in Figure 2.2). This pulse is present for the duration of the Latch and is fed to the Ramp section to start the ramp cycle as well as to provide a prompt input to the final OR stage which is used to drive the output stage.

Once a ramp is generated (see Section 2.3), the Ramp Detector output is fed to the OR along with the Latch output to hold the output stage "on" and inhibit the Start input for the entire ramp duration. At the maximum amplitude of the ramp, the Stop-level Detector (in the

Ramp section) will reset the Latch, but the output of the final OR will still be present until the ramp is totally recovered, at which point the Ramp Detector will return to its quiescent level, removing drive from the output stage.

The STOP input is intended primarily for use in the LATCH mode of operation. In this mode, the Ramp section is disabled, so the output stage follows the Latch output only. (See "Start-Stop Mode" timing diagram in Figure 2.2). A Stop input will reset the Latch previously set by the Start. Therefore, the output stage will be driven only for the time from Start to Stop. If a Stop input is generated when operating in any of the preset modes, it will reset the Latch before the end of the ramp, causing the ramp to be shortened, but because the output stage follows the total ramp duration, the output width will not be promptly terminated, but will be extended by the ramp recovery time (which depends on both the range setting and the amount of preset time which had already elapsed before the Stop was generated).

The input OR stage converts NIM levels to offset ECL levels required to drive directly the final OR stage, independent of the states of the Start-Stop stage, the Latch, the Ramp stage, etc. Thus it provides a final output width equal to the input OR width (or to the overlap of it and the Start-Stop Latch and/or the Ramp Detector).

2.3 Ramp and Ramp Detector Stages

The Ramp stage is composed of a capacitor, C_n (n=1,2...8, as selected by the FULL SCALE WIDTH switch), resistor R1 (paralleled by R2 on the 1.0 μsec range), and a 10 mA current source (transistor Q15). The current source is quiescently on, causing the ramp to be clamped at about +3 V by the 1N702 zener diode and the base-emitter drop of Q2. When the Start-Stop Latch is set by a Start pulse, the Q15 current source is disabled and the ramp begins to discharge toward -3 V at a rate determined by R1 (15 kΩ, or 7.5 KΩ when paralleled by R2 on 1.0 μsec range) and C_n which is determined by the FULL SCALE WIDTH switch setting. (See "Presettable Width Mode" timing diagram in Figure 2.2)

As soon as the current source is turned off, the integrated circuit comparator used as the Ramp Detector is enabled because the collector of Q15 goes to zero. When the ramp reaches the voltage level set by the 2 kΩ front panel vernier width potentiometer, the Stop-level Detector comparator I.C. resets the Start-Stop Latch. This enables the current source and the ramp is returned to its quiescent level at a rate determined primarily by the 10 mA of the current source and the value of C_n. When the ramp reaches the clamp level determined by transistor Q2, the current is shunted to Q2 collector, the Ramp Detector turns off, the output drive to the ECL final OR and the inhibit to the Start stages are removed, and the unit can be retriggered.

2.4 Output and Blanking Stages

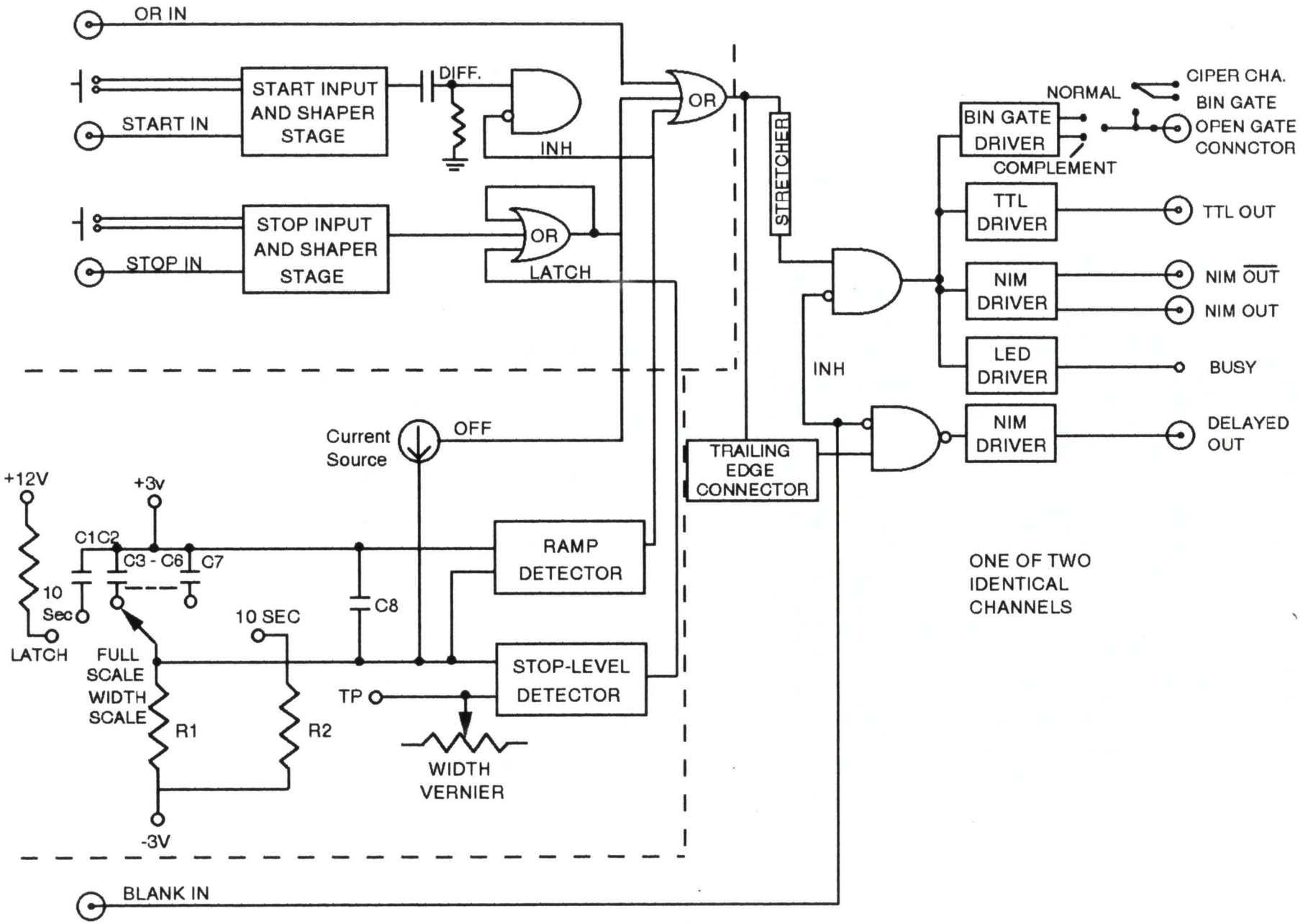
The NIM driver output stage is a 16 mA differential stage operating

from the output OR (with a 5 nsec stretcher stage) via a 1N706 zener diode to provide level shifting. Both the normal and complementary outputs are made available and they are individually clamped at -1 V if no output load is present.

The TTL and Bin Gate output stages and the BUSY LED driver are driven from a stage the same as above except that the collectors are referenced to positive voltages. The TTL stage uses a double emitter-follower to provide stiff drive for either logic level. The Bin Gate output uses one of two switch-selectable, stiff, clamp-to-ground inverting transistors. One provides a normal level to inhibit modules on the bin gate bus for the duration of the output. The other provides an inverted level to inhibit quiescently and to enable only during the output duration. The Busy driver holds the BUSY LED on for the duration of the output, stretching short pulses enough to provide a visual indication.

The Delayed Output stage is also similar to the NIM driver stage, except that only the normal output (quiescently zero, -16 mA during pulse) is available and the stage is driven from a trailing-edge differentiator-shaper stage to generate a 10 nsec wide pulse.

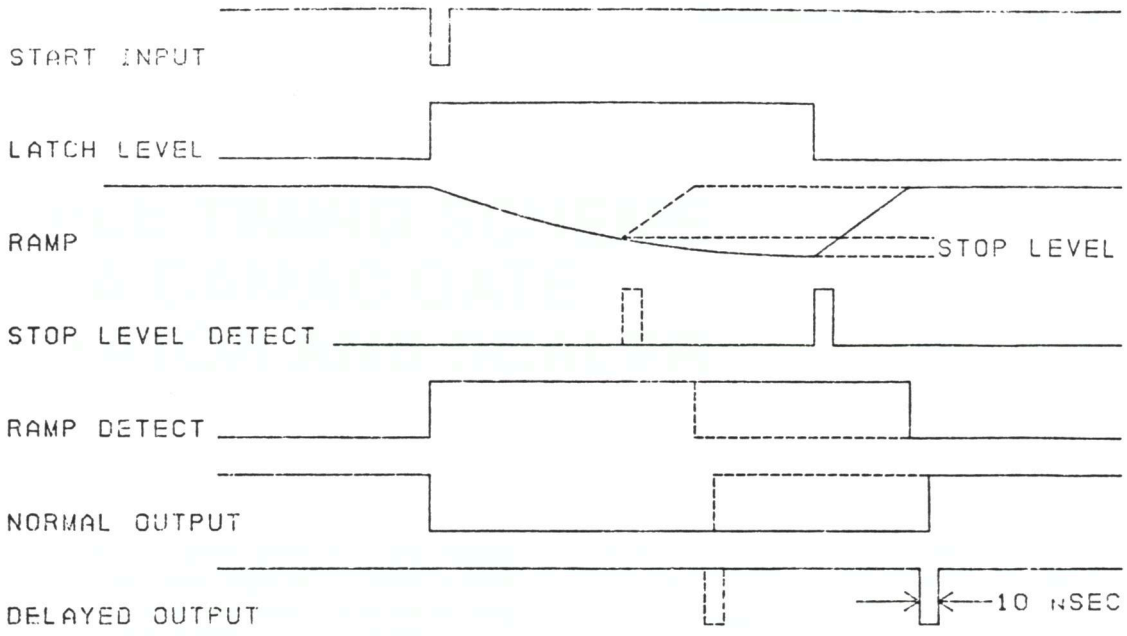
The Blanking input converts a NIM level input to a proper level to disable the three differential stages, and therefore all outputs and the BUSY LED, for the duration of the Blanking input.



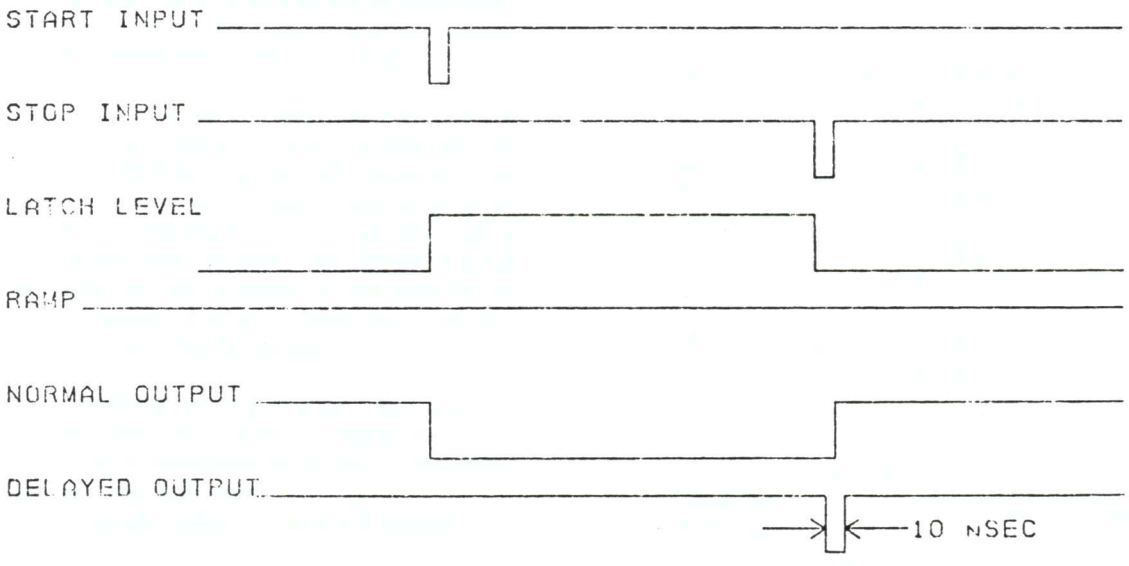
FUNCTIONAL BLOCK DIAGRAM MODEL 222 DUAL GATE GENERATOR

Figure 2.1

MODEL 222 DUAL GATE GENERATOR
TIMING DIAGRAMS



PRESETTABLE WIDTH MODE



START-STOP MODE

Figure 2.2

APPLICATION NOTE

LeCroy

Innovators in Instrumentation

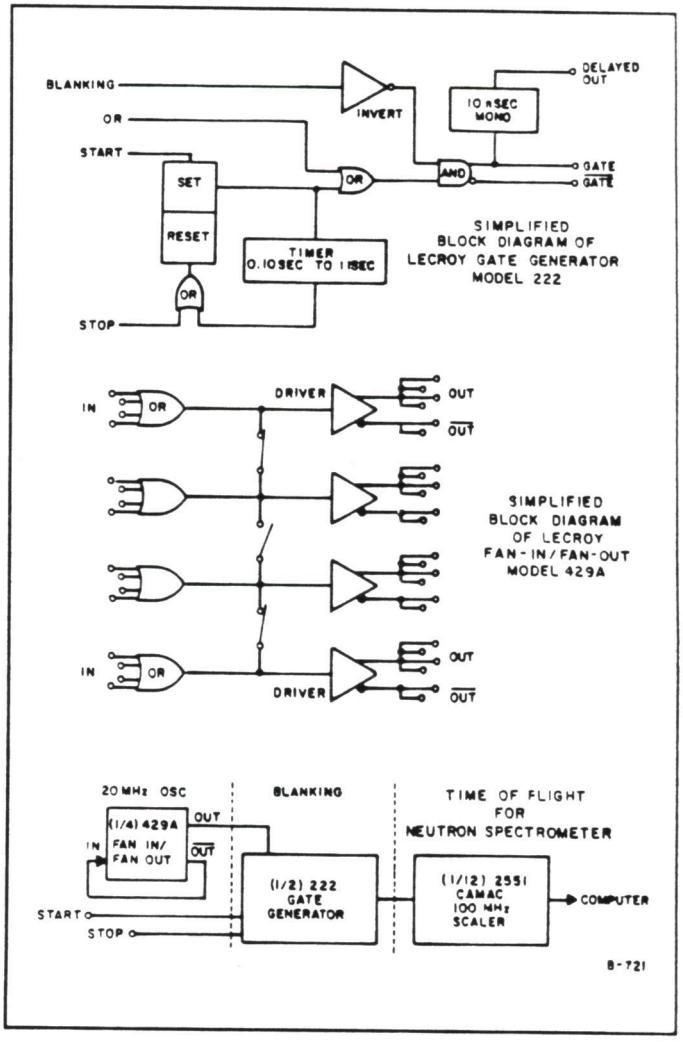
AN-4

A SIMPLE TIMING SCHEME USING A CAMAC GATE GENERATOR AND SCALER

The LeCroy Models 222, gate generator, and Model 2551, scaler, may be used together to form a time digitizer capable of 20 nsec resolution for times as long as 200 msec. If a signal is applied to the start input of the Model 222 and a second signal is applied to the stop input, the Model 222 puts out a gate pulse of duration equal to the time between the start and the stop input pulses or the preset gate time, whichever is smaller. In this way, a gate equal to the time of interest is generated with a provision for overflow. This feature is often necessary when no stop pulses are to be expected.

The blanking input of the Model 222 sets the output of the module to a logical zero state for the duration of the blanking signal. The minimum pulse width to which the blanking input will respond is 10 nsec. Thus, a 50 MHz clock may be applied to this input. In this case, the output of the Model 222 when used as described above will be a 50 MHz pulse train for the duration of the time to be measured. These pulses may be counted by a LeCroy Model 2551 12-channel CAMAC scaler.

Such a system consisting of one Model 2551 and 12 Model 222s may be used for a variety of applications including neutron time-to-flight spectroscopy. The common start (stop) signals and the clock signals may be fanned out using a Model 429A in the 2 x 8 mode.



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European Headquarters: Route du Nant-d'Avril 101 CH-1217 Meyrin 1-Geneva, Switzerland, Tel: (022) 82 33 55 Telex: 28230

TECHNICAL INFORMATION

(SCHEMATICS, PARTS LISTS)

PART NUMBER	DESCRIPTION REMARK	QTY PER
102145503	CAP CERA DISC 12V .05 UF	2
102245103	CAP CERA DISC 25V .01 UF	25
102245103	CAP CERA DISC 25V .01 UF	48
102444101	CAP CERA DISC 100V 100 PF	2
102444101	CAP CERA DISC 100V 100 PF	3
102444330	CAP CERA DISC 100V 33 PF	12
102745511	CAP CERA DISC 500V 510 PF	2
102944033	CAP CERA DISC 1KV 3.3 PF	2
102944075	CAP CERA DISC 1KV 7.5 PF	4
102944100	CAP CERA DISC 1KV 10 PF	8
102944100	CAP CERA DISC 1KV 10 PF	9
103327102	CAP CERA MONO 50V .001 UF	9
106435102	CAP CERA MONO .001UF	9
106443100	CAP CERA MONO 10PF	9
106443101	CAP CERA MONO 100PF	3
106443221	CAP CERA MONO 220PF	1
106443330	CAP CERA MONO 33PF	19
106443820	CAP CERA MONO 82PF	1
106445103	CAP CERA MONO .01UF	48
116000910	CAP DIP MICA SPECL 91 PF	2
116515100	CAP DIP MICA DM10 10 PF	2
116515101	CAP DIP MICA DM10 100 PF	1
116515151	CAP DIP MICA DM10 150 PF	8
116515241	CAP DIP MICA DM10 240 PF	1
116515330	CAP DIP MICA DM10 33 PF	2
116515330	CAP DIP MICA DM10 33 PF	19
116515331	CAP DIP MICA DM10 330 PF PUT IN IC BOX.	2
116515470	CAP DIP MICA DM10 47 PF	2
116515560	CAP DIP MICA DM10 56 PF	1
116515680	CAP DIP MICA DM10 68 PF	1
116525821	CAP DIP MICA DM15 820 PF	1
116545332	CAP DIP MICA DM19 3300 PF PUT IN IC BOX.	2
140173337	CAP TANT METAL CAN 330 UF PUT IN IC BOX.	2
140243336	CAP TANT METAL CASE 33 UF PUT IN IC BOX.	2
140323335	CAP TANT METAL CAN 3.3 UF PUT IN IC BOX.	2
140523334	CAP TANT METAL CAN .33 UF PUT IN IC BOX.	2
140623333	CAP TANT METAL CAN.033 UF PUT IN IC BOX	2
141854685	CAP TANT DIP CUT.300+/-75 6.8UF	31
141854685	CAP TANT DIP CUT.300+/-75 6.8UF	28
142824685	CAP TANT DIP CASE 6.8 UF	8
147147090	CAP ALUM METAL CAN 90 UF	1
147447050	CAP ALUM METAL CAN 50 UF	2
158819001	CAP VARI CERA 3.5 - 18 PF	1
161030000	RES COMP ZERO OHMS	55
161225102	RES CARBON FILM 1 K	9

PART NUMBER	DESCRIPTION REMARK	QTY PER
161225102	RES CARBON FILM 1 K	8
161225121	RES CARBON FILM 120 OHMS	3
161225220	RES CARBON FILM 22 OHMS	3
161225222	RES CARBON FILM 2.2 K	12
161225390	RES CARBON FILM 39 OHMS	10
161225391	RES CARBON FILM 390 OHMS	5
161225751	RES CARBON FILM 750 OHMS	1
161335101	RES CARBON FILM 100 OHMS	10
161335101	RES CARBON FILM 100 OHMS	19
161335101	RES CARBON FILM 100 OHMS	18
161335102	RES CARBON FILM 1 K PUT IN IC BOX.	26
161335102	RES CARBON FILM 1 K	33
161335102	RES CARBON FILM 1 K	31
161335103	RES CARBON FILM 10 K	8
161335103	RES CARBON FILM 10 K	4
161335104	RES CARBON FILM 100 K	4
161335111	RES CARBON FILM 110 OHMS	2
161335121	RES CARBON FILM 120 OHMS	4
161335122	RES CARBON FILM 1.2 K	1
161335123	RES CARBON FILM 12 K	2
161335133	RES CARBON FILM 13 K	1
161335152	RES CARBON FILM 1.5 K	2
161335153	RES CARBON FILM 15 K PUT IN IC BOX.	4
161335153	RES CARBON FILM 15 K	1
161335163	RES COMP 1/4W 5% 16 K	1
161335182	RES COMP 1/4W 5% 1.8 K	8
161335200	RES CARBON FILM 20 OHMS	2
161335201	RES CARBON FILM 200 OHMS	4
161335202	RES CARBON FILM 2 K	36
161335202	RES CARBON FILM 2 K	2
161335203	RES CARBON FILM 20 K	2
161335221	RES CARBON FILM 220 OHMS	2
161335221	RES CARBON FILM 220 OHMS	4
161335222	RES CARBON FILM 2.2 K	5
161335222	RES CARBON FILM 2.2 K	4
161335223	RES CARBON FILM 22 K	3
161335241	RES CARBON FILM 240 OHMS	1
161335242	RES CARBON FILM 2.4 K	4
161335242	RES CARBON FILM 2.4 K	2
161335244	RES CARBON FILM 240 K	1
161335272	RES CARBON FILM 2.7 K	4
161335301	RES CARBON FILM 300 OHMS	4
161335332	RES CARBON FILM 3.3 K	2
161335333	RES CARBON FILM 33 K	1
161335333	RES CARBON FILM 33 K	8
161335391	RES CARBON FILM 390 OHMS	2
161335391	RES CARBON FILM 390 OHMS	1
161335392	RES CARBON FILM 3.9 K	2
161335392	RES CARBON FILM 3.9 K	3
161335393	RES CARBON FILM 39 K	1

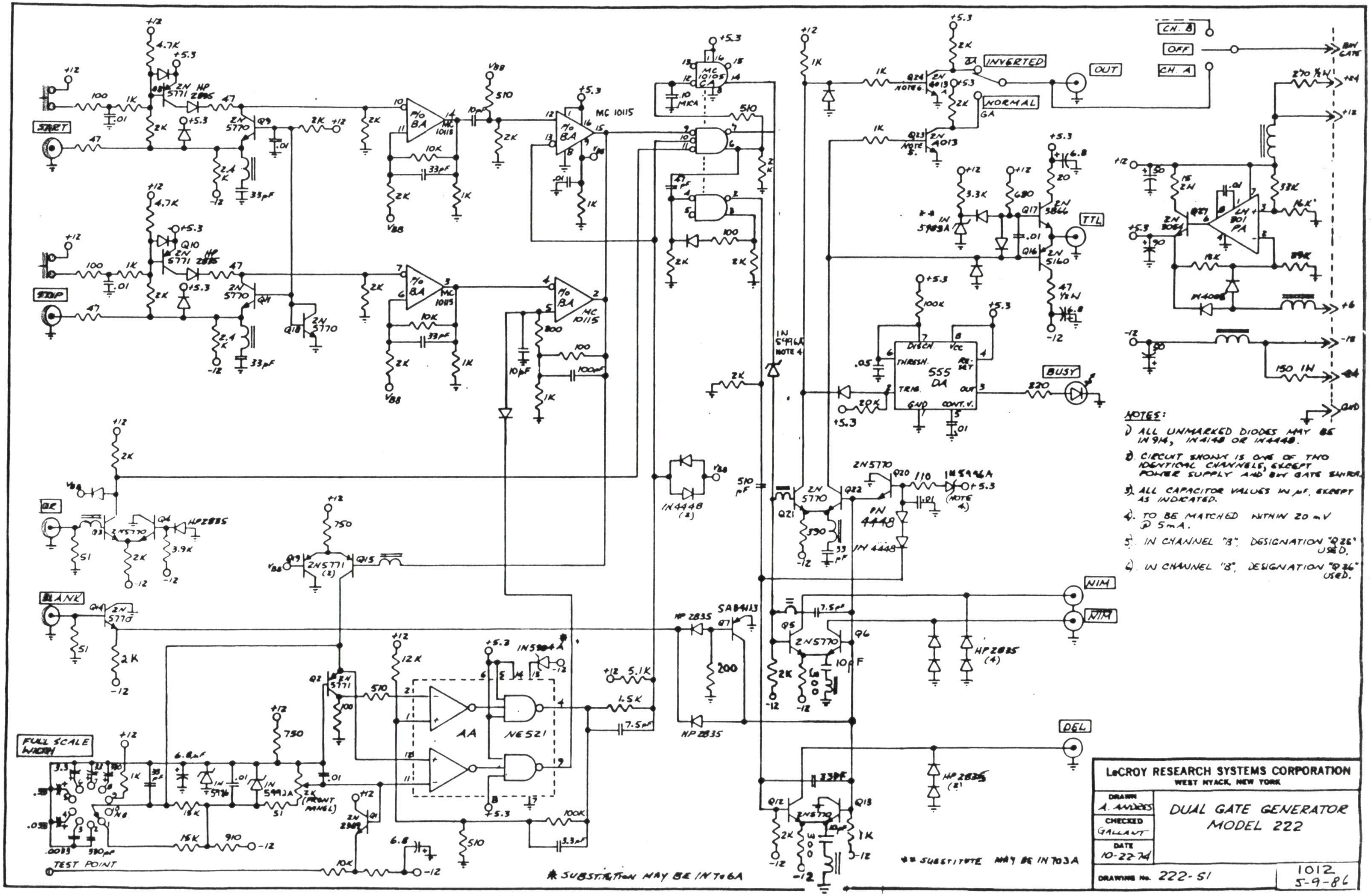
PART NUMBER	DESCRIPTION REMARK	QTY PER
161335470	RES CARBON FILM 47 OHMS	8
161335472	RES CARBON FILM 4.7 K	4
161335510	RES CARBON FILM 51 OHMS	6
161335510	RES CARBON FILM 51 OHMS	20
161335510	RES CARBON FILM 51 OHMS	8
161335511	RES CARBON FILM 510 OHMS	8
161335511	RES CARBON FILM 510 OHMS	36
161335512	RES CARBON FILM 5.1 K	2
161335512	RES CARBON FILM 5.1 K	25
161335513	RES CARBON FILM 51 K	2
161335622	RES CARBON FILM 6.2 K	1
161335681	RES CARBON FILM 680 OHMS	2
161335681	RES CARBON FILM 680 OHMS	5
161335751	RES CARBON FILM 750 OHMS	4
161335751	RES CARBON FILM 750 OHMS	3
161335752	RES CARBON FILM 7.5 K	1
161335911	RES CARBON FILM 910 OHMS	2
161445271	RES CARBON FILM 270 OHMS	1
161445470	RES CARBON FILM 47 OHMS	2
161555151	RES COMP 1W 5% 150 OHMS	1
161665150	RES COMP 2W 5% 15 OHMS	1
168531413	RES PREC RN55D 1.62 K	8
168531681	RES PREC RN55D 1.00 MEG	8
181457501	RES VARI CERMET 500 OHMS	1
181457502	RES VARI CERMET 5 K	3
182527202	RES VARI CERMET 2 K	2
182537502	RES VARI CERMET 5 K	1
190042560	RESISTOR NETWORK 56 OHMS	2
190842560	RESISTOR NETWORK 56 OHMS	1
200031011	IC J-K FLOP SN7473N	1
200031028	IC 2-INPUT NAND SN74LS00N	3
200031033	IC 2-INPUT NAND SN7403N	4
200031046	IC HEX INVERTER SN74LS04N	2
200031047	IC 3-INPUT NAND SN74LS10N	1
200031051	IC 2-INPUT NOR SN74LS02N	3
200031052	IC 8-INPUT NAND SN74LS30N	2
200041020	IC DECODER SN74LS42N	1
200041049	IC D-TYP FLOP SN74LS175N	2
200041053	IC 3GRAY-DEC DECOD N7444B	1
200042002	IC MULTIVIBRATOR 9602PC	1
200081007	IC MULTIPLEXER SN74LS151	1
204042001	IC 4-5 OR/NOR GT MC10109P	1
204042002	IC NOR GATE MC10102P	9
204042003	IC LINE RECEIVER MC10115P	2
204042003	IC LINE RECEIVER MC10115P	1
204042003	IC LINE RECEIVER MC10115P	3
204042004	IC 2-3-2-IN GATE MC10105P	2
204042015	IC LINE RECEIVER MC10114P	1
208011003	IC SINGLE OP AMP LM301AN	1
208011003	IC SINGLE OP AMP LM301AN	3
208011004	IC TIMER NE555	2
208031003	IC VOLT COMPARATOR NE521A	2

PART NUMBER	DESCRIPTION REMARK	QTY PER
208031003	IC VOLT COMPARATOR NE521A	6
208033001	IC TRANS ARRAY CA3046	8
230110005	DIODE SWITCHING 1N4448	33
230110005	DIODE SWITCHING 1N4448	12
235010005	DIODE RECTIFIER 1N4005	1
235010005	DIODE RECTIFIER 1N4005	2
240225702	DIODE ZENER 2.7V 1N5986A	2
240225702	DIODE ZENER 2.7V 1N5986A	1
240225703	DIODE ZENER 3.6V 1N5989A	2
240225705	DIODE ZENER 4.7V 1N5992A	2
240225705	DIODE ZENER 4.7V 1N5992A	4
240225706	DIODE ZENER 5.6V 1N5994A	2
240225707	DIODE ZENER 6.8V 1N5996A SEND TO RSD PROD. FOR MATCHING.	4
240425751	DIODE ZENER 5.1V 1N751A	4
253010835	DIODE SCHOTTKY HP2835	22
253010835	DIODE SCHOTTKY HP2835	2
256010102	DIODE LED (RED) DIFF LENS	2
270110001	TRANSISTOR NPN PN2369A	2
270110001	TRANSISTOR NPN PN2369A	1
270110004	TRANSISTOR NPN 2N4013	4
270140001	TRANSISTOR NPN 2N3866	2
270170001	TRANSISTOR NPN 2N5770	26
270170001	TRANSISTOR NPN 2N5770	22
270170001	TRANSISTOR NPN 2N5770	12
270190001	TRANSISTOR NPN PWR 2N3054	1
275110001	TRANSISTOR PNP 2N2907A	1
275140001	TRANSISTOR PNP PWR 2N5160	2
275170001	TRANSISTOR PNP 2N5087	8
275170002	TRANSISTOR PNP 2N5771	10
275170002	TRANSISTOR PNP 2N5771	12
275170003	TRANSISTOR PNP A441	2
300010001	BEAD SHIELDING FERRITE	14
300010001	BEAD SHIELDING FERRITE	19
300020001	BEAD SHIELDING "1/2" SIZE	2
300020001	BEAD SHIELDING "1/2" SIZE	1
300050001	CHOKE FERRITE SINGLE LEAD	3
300050001	CHOKE FERRITE SINGLE LEAD	5
302000001	INDUCTOR SPECIAL 1.00 UH	1
400010008	SOCKET IC SOLD TAIL DIP-8	3
400020014	SOCKET IC SOLD TAIL DIP-14	2
400020014	SOCKET IC SOLD TAIL DIP-14	20
400020014	SOCKET IC SOLD TAIL DIP-14	30
400030016	SOCKET IC SOLD TAIL DIP-16	4
400030016	SOCKET IC SOLD TAIL DIP-16	9
400030016	SOCKET IC SOLD TAIL DIP-16	20
400040024	SOCKET IC SOLD TAIL DIP-24	4
402030000	CONN CO-AX LEMO	18
402030000	CONN CO-AX LEMO	11
402030002	SPANNER NUT SMALL OD LEMO	18
402030002	SPANNER NUT SMALL OD LEMO	11

PART NUMBER	DESCRIPTION REMARK	QTY PER
402030003	GROUND LUG NONLOCK LEMO	8
402030003	GROUND LUG NONLOCK LEMO	11
405112001	CONNECTOR BLOCK (PIN)	1
405212002	GUIDE PIN (MALE)	1
405213001	GUIDE PIN (MALE)	1
405312001	GUIDE PIN (FEMALE)	2
405410016	CONNECTOR PIN (MALE)	7
405613001	CONNECTOR HOOD	1
405812002	SOCKET STRIP SOLDR 20 POS	9
408063005	WIREWRAP PIN 1-WRAP	12
410112102	SWITCH TOGGLE SPDT	2
410112203	SWITCH TOGGLE SPDT	1
412111002	SWITCH ROTARY 1P10T	2
412141505	SWITCH ROTARY PC MTG 1P5T	3
416110001	SWITCH PUSHBUTTON NO SPST	4
433220002	FUSE PICO II 125V 3 AMP	2
454713016	HDR SOLD TAIL/MALE 16	2
468622002	TEST POINT (JACK) BLU	1
468911001	TEST POINT (JACK) WHT	2
500120002	TRANSIPAD "LARGE"	4
500510004	INSULATOR MICA FOR 8-PIN	3
519110002	BUSHING LED BLK MP 52	2
520000510	STANDOFF GLASS 8MM	50
521000004	SPACER HEX 2-56X.417	4
521400022	SPACER ROUND #4 11/16	2
521400024	SPACER ROUND #4 3/4	2
536142004	KNOB ASSY, 3-PIECE BLACK	2
540103102	SIDE COVER NIM LEFT	1
540103103	SIDE COVER NIM RIGHT	1
540105001	BRACKET NIM WRAP SIZE #1	2
540109100	SWITCH HOLE PATTERN COVER	1
540203001	SIDE COVER CAMAC STD(LIP)	1
540206078	RAIL CAMAC STD TOP W/LIP	1
540206178	RAIL CAMAC STD BOT W/LIP	1
540209101	REAR PANEL CAMAC SIZE 1	1
555430003	CAPTIVE SCREW ASSEMBLY	1
555611001	CAPTIVE SCREW 6-32	2
555621002	CAPTIVE SCREW RETAINER	2
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	4
560440004	SCREW PHILIPS 4-40X1/4	2
560440005	SCREW PHILIPS 4-40X5/16	6
560440014	SCREW PHILIPS 4-40X7/8	2
567256004	SCREW FLAT PHIL 2-56X1/4	4
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
568440003	SCREW FLAT PHIL 4-40X3/16	10
577400001	WASHER SHAKEPROOF SIZE 4	4
580440001	NUT HEX STANDARD 4-40	2
585141237	RIVET "POP" ALU 1/8X.237	2
590001022	WIRE TEFLON 7/30 BLK 22	2
590111022	WIRE TEFLON 7/30 BRN 22	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
590221022	WIRE TEFLON 7/30 RED 22	1
590331022	WIRE TEFLON 7/30 ORA 22	1
590441022	WIRE TEFLON 7/30 YEL 22	1
590551022	WIRE TEFLON 7/30 GRN 22	1
590881022	WIRE TEFLON 7/30 GRAY 22	1
590991022	WIRE TEFLON 7/30 WHT 22	8
591002130	WIRE TEF BLK SOLID AWG 30	1
591023030	WIRE TWIST BLK/RED AWG 30	2
591101022	WIRE BUS TIN-COPP AWG 22	1
591101024	WIRE BUS TIN-COPP AWG 24	1
593910001	CABLE CO-AXIAL RG178B/U	4
593910001	CABLE CO-AXIAL RG178B/U	2
594120001	TIEWRAP	3
595003018	SLEEVING SHRINK BLK 3/32"	1
595003104	SLEEVING SHRINK BLK 3/8"	1
595901022	SLEEVING TEFLON AWG 22	2
595901022	SLEEVING TEFLON AWG 22	1
710222013	PC BD PREASS'Y 222	1
712228013	PC BD PREASS'Y 2228A	1
712229003	PC BD PREASS'Y 2229	1
720222013	FRONT PNL PREASS'Y 222	1
722228013	FRONT PNL PREASS'Y 2228A	1
722229003	FRONT PNL PREASS'Y 2229	1
732228013	SIDE CAMAC LEFT 2228A	1
732229003	SIDE CAMAC LEFT 2229	1
740222013	WRAPAROUND NIM 1 222	1
SC100	2X30MHZ SCALER HYBR	4

nd of report. 373 Details encountered.


NOTES:
1) ALL UNMARKED DIODES MAY BE IN914, IN4148 OR IN4448.
2) CIRCUIT SHOWN IS ONE OF TWO IDENTICAL CHANNELS, EXCEPT POWER SUPPLY AND BW GATE SWITCH.
3) ALL CAPACITOR VALUES IN µF, EXCEPT AS INDICATED.
4) TO BE MATCHED WITHIN 20 mV @ 5mA.
5) IN CHANNEL "B" DESIGNATION "Q26" USED.
6) IN CHANNEL "B" DESIGNATION "Q26" USED.
✱ SUBSTITUTION MAY BE IN706A
✱✱ SUBSTITUTE MAY BE IN703A
START
STOP
OR
BLANK
FULL SCALE WIDTH
TEST POINT
OUT
INVERTED
NORMAL
TTL
BUSY
NIM
DEL
CH. B
OFF
CH. A
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN A. ANDES
CHECKED GALLANT
DATE 10-22-74
DUAL GATE GENERATOR
MODEL 222
DRAWING No. 222-S1
1012
5-9-86