technical information manual

CAMAC Model 2228

Octal Time-to-Digital Converter

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

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LeCroy Research Systems Corp.
West Nyack, New York

technical information manual

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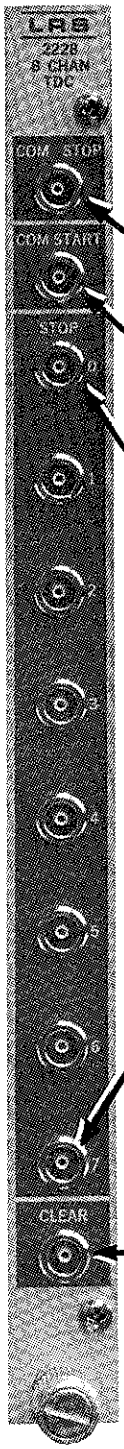
Octal Time-to-Digital Converter



CAMAC #1 module
Total Power used 8.3 watts

Common Stop Input; Z = 50 Ω; NIM level* signals; for calibration only.

Common Start Input; Z = 50 Ω; NIM level* signal.

8 Stop inputs; Z = 50 Ω; NIM level* signal.

Fast Clear Input; Z = 50 Ω; NIM level* signal; duration ≥to nsec; 1.5 sec settling time required after clear.

>-600 mV

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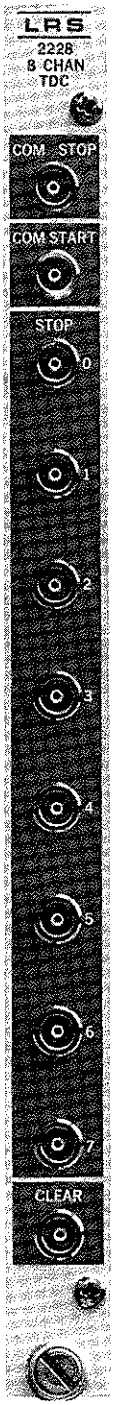
TECHNICAL DATA



CAMAC Model 2228

Octal Time-to-Digital Converter

* **8 channels in single-width module**
* **10-bit (1024 channel) resolution**
* **Switch-selectable 102 ns, 204 ns, and 510 ns full-scale time ranges.**
* **Time resolutions of 100 ps, 200 ps, or 500 ps**
* **Rejects stops before starts**
* **Fast clear input**
* **Internal test capability**
* **Common stop input for precision on-line testing**
* **Full LAM functions**
* **Fast digitizing time**
* **Q and LAM suppression**

The LRS Model 2228 Octal Time-to-Digital Converter, the state-of-the-art successor to the popular Model 2226A Quad TDC, incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals.

The Model 2228 has 8 independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Each 2228 channel disregards any stop pulses received before a start signal and will accept only one stop for every start.

Conversion begins upon receipt of the start signal and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel clear signal; or the TDC reaches full scale.

The 2228 converts the measured time intervals into a 10-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 50 microseconds. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2228 has three switch-selectable full-scale time ranges, 102 ns, 204 ns, and 510 ns, which are digitized to 10 bits (1024 channels) and provide 100 ps, 200 ps, and 500 ps resolutions respectively. Longer time ranges (up to a few microseconds) may be provided on request at slight expense of stability and accuracy.

On-line testing is facilitated by either a front-panel common stop input or F(25). A signal at the common stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of $\approx$75 ns.

In high rate experiments, excessive system deadtime due to false starts may be eliminated through use of the 2228's fast clear input. Accepting NIM level signals, this input allows the TDC to be cleared within 2 microseconds at any point in its conversion cycle and without the necessity for any dataway operations.

All standard LAM functions are available in the 2228 to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

May 1974

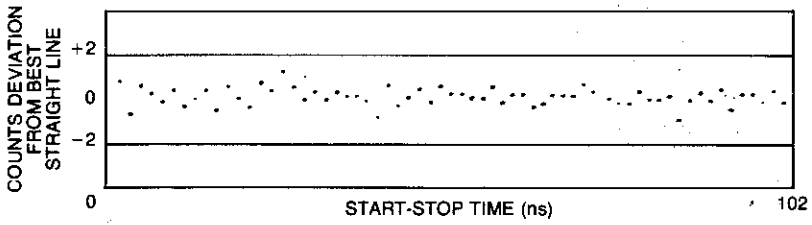
Innovators In Instrumentation

LeCROY RESEARCH SYSTEMS CORPORATION · WEST NYACK, NEW YORK 10994 · TELEPHONE: (914) 358-7900

SPECIFICATIONS
CAMAC Model 2228
OCTAL TIME-TO-DIGITAL CONVERTER

Stop Inputs:	8, one per channel; 50 Ω impedance; Lemo-type connectors; direct-coupled; input amplitude > —600 mV; ineffective unless preceded by a "Start" input.
Common Start Input:	One, common to all channels; 50 Ω impedance; Lemo-type connector; input amplitude > −600 mV.
Common Stop Input:	One, common to all channels; 50 Ω impedance; Lemo-type connector; > −600 mV; functions identical to individual "Stop Inputs" above; used for precision on-line testing.
Fast Clear:	One input common to all channels; Lemo-type connector; 50 Ω impedance; −600 mV or greater clears; minimum duration, 50 ns (requires additional 2.0 μs settling time after clear).
Full-Scale Time Range:	10-bit binary output corresponds to 102 ns, 204 ns, and 510 ns, switch selectable (with longest range field adjustable up to 1 μsec). Larger full-scales possible by factory option at slight expense of accuracy and stability, giving 1 μsec, 2 μsec, and 5 μsec as the 3 switch-selectable time ranges.
Integral Non-linearity:	± 2 counts (10 ns to full scale). Set of linearity curves for all channels supplied with each unit. (See graph below.)
Time Resolution:	100 ps on 102 ns range; 200 ps on 204 ns range; 500 ps on 510 ns range.
Temperature Coefficient:	Typically (+ 0.02% of full scale ± 0.01% of reading) per degree C.
Digitizing Time:	50 μsec; conversion is initiated by receipt of "Start" input.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Test Functions:	An internal start/stop is generated by F(25) with ≈75 ns spacing. Precision on-line testing and calibrating can be done with common start and common stop above.
Data:	The proper CAMAC function and address command gates the 10 binary bits plus overflow bit of the selected channel onto the R(1) to R(11) (2^0 to 2^{10}) Dataway bus lines.
CAMAC Commands:	Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2." I: "Start" input is inhibited during CAMAC "Inhibit" command. Q: A Q=1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. L: A Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed by empty modules.
CAMAC Function Codes:	F(0): Read registers; requires N and A. A(0) through A(7) are used for channel address. F(2): Read registers and clear module; requires N, A, and S2. Clears on A(7) only. F(8): Test Look-At-Me; requires LAM, N, and any A from A(0) to A(7) independent of Disable Look-At-Me. Q is generated if LAM is present. F(9): Clear module (and LAM); requires N and A, and S2. F(10): Clear Look-At-Me; requires N, S2, and any A from A(0) to A(7). F(24): Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). F(25): Test module; requires N, S2, and any A from A(0) to A(7). F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(7). Remains enabled until Z or F(24) applied. Caution: The state of the LAM mask will be arbitrary after power turn-on.
Q and LAM Suppression:	A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.
Packaging:	In conformance with CAMAC standard for nuclear modules. RF-shielded CAMAC #1 module.
Power Requirements:	+24 V at 20 mA; —24 V at 50 mA; +6 V at 550 mA; —6 V at 550 mA.

TYPICAL 2228 INTEGRAL LINEARITY



OPERATION

General: The LRS Model 2228 TDC contains eight complete time-to-digital converters in a single-width CAMAC module. The time-to-digital conversion is accomplished in two steps. A capacitor is charged up by a constant current source initiated by the common start pulse and terminated by the stop pulse. The total charge delivered to the capacitor is an analog representation of the time interval to be measured. An analog-to-digital conversion is then performed by using the Wilkinson rundown method. In this technique, the charge is removed from the capacitor at a constant rate during which time pulses from an oscillator are gated into a scaler. The final count is thus proportional to the time interval measured.

Inputs: The eight Stop inputs of the 2228 are terminated in 50 Ω. NIM-level pulses at these inputs (>-600 mV) define the end of the timing intervals for the eight channels. The Stop input pulses should be on the order of 5 nsec FWHM, since an accidental Stop pulse coming in before the Start would cause the channel to ignore the real Start pulse if the Stop still exists at that time. A short Stop pulse width would minimize the possibility. 5 nsec FWHM is also the recommended minimum width required to drive the 2228 Start and Stop inputs.

The Common Start and Common Stop (TEST) inputs are also terminated in 50 Ω, and accept fast NIM-level pulses (>-600 mV). A pulse applied to the Common Start input begins the timing measurement unless it is held in an inhibited condition by the CAMAC I (Inhibit) command. The Common Stop input is intended for calibration use. For on-line precision testing, a pulse applied to this input will stop all inputs together. It will terminate the timing interval 4.5 ± 0.5 nsec later than if the same pulse were applied to the separate Stop inputs.

The time relationship between the Start and Stop inputs is approximately zero nsec. However, the time difference between Start and Stop must be approximately 2.4 nsec before any counts are seen at the output. (The lowest output count is 3.) It is recommended that some time difference (say, 5 nsec) is insured by cable delay, giving some fixed output counts when Start and Stop input pulses are exactly coincident. The fixed counts can later be software-subtracted from the total output count for a true representation of the time interval. This will assure that any time differences can be measured down to the inherent accuracy of the 2228.

The actual time differences between the Start and Stop inputs that yield a full scale (10-bit) output are 100 nsec, 200 nsec, or 500 nsec, depending on the time-range-select switch setting. The full scales on the 8 channels of each 2228 are set up to match within 5% of each other.

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Fast Clear: A front-panel fast clear input accepting fast NIM-level signals (>-600 mV into 50 Ω of minimum duration, 50 nsec) forces all 8 channels of the unit to cease their conversions and be cleared and ready to accept another gate pulse after 1.2 to 1.5 microseconds. In worst-case conditions, the 2228 will clear to within 1 count after 1.2 μsec, and to 0 counts within 1.5 μsec. An internal monostable makes the 1.2 μsec period mandatory, although this can be changed by special request at a sacrifice in the extent of clearing. The fast clear feature allows TDC conversion to be initiated by a fast trigger and completed only if the event satisfies a complete trigger requirement.

Test Function: The Model 2228 offers two choices of on-line testing. The first method involves the use of the Common Stop input. A pulse applied to this input will simultaneously stop all channels. It is important to note that this common stop pulse will terminate the timing interval 4.5 ± 0.5 nsec later than if the same pulse were applied to the seperate Stop inputs.

During the precision on-line testing using this common stop input, it is still possible for the individual Stop inputs to independently stop their respective channels earlier. It is therefore recommended that the normal stop pulse sources be vetoed (inhibited) during the testing time.

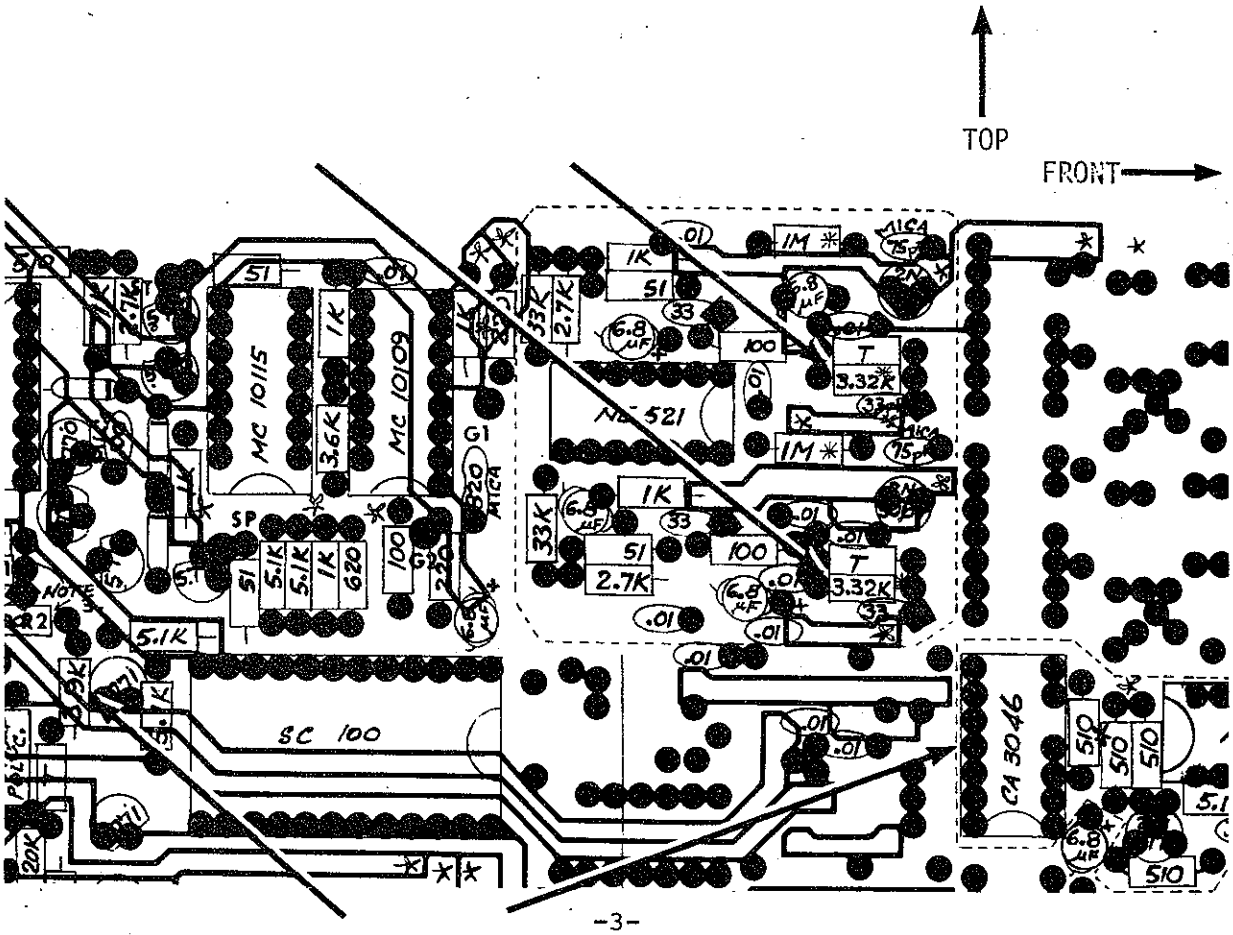
A second method of performing on-line 2228 testing is via the CAMAC function F(25). Upon application of F(25)·N·A (any A from A0 to A7) at S2 time, an internal Start and Stop is generated, defining a time increment of approximately 75 nsec for all 8 channels. Once again, a Stop input at any of the 8 channels will also terminate the time interval for that channel. For this reason, the sources of the stop pulses (logic units or discriminators) should be inhibited during testing, or multiple tests should be made to assure that no spurious pulses stopped any channel short of the full testing interval.

Full Scale Time Ranges: The full scales of the 8 channels of each 2228 are factory set at 102 nsec, 204 nsec, and 510 nsec ± 5%. The final range may be increased to 1024 nsec by readjusting the side panel potentiometer corresponding to the final time range. All three ranges may be side panel adjusted if slightly higher or lower calibration is desired.

If time measurements in excess of 1 μsec are desired, the three ranges can be changed to 1, 2, and 5 μsec respectively. This option, recommended as a factory modification only, involves the replacement of 9 resistors with values

approximately 10x the size of the standard values, and the subsequent recalibration of the unit. In each of the 8 channels, the 3.32KΩ resistor is replaced by 33.2K Ω, and the 3.9KΩ common resistor is replaced by 47KΩ as shown in the circuit board layout below. Each range must then be readjusted by applying accurate 1, 2, and 5 µsec start-stop intervals and turning the side panel potentiometers until a full scale count of 1024 ± 5% is obtained on all channels. Occasionally, one or more channels may deviate from another by more than 5%. In this case, an additional trim resistor may be put across the 33.2KΩ resistor, or the front end IC (CA3046) may be selected.

In conjunction with simply expanding the time ranges as described above, care must also be taken to reduce the inaccuracy caused by the now-expanded amount of time the rundown is taking before the oscillator starts. The ramifications of this circuit characteristic and the necessary compensating adjustments are described in the following section.



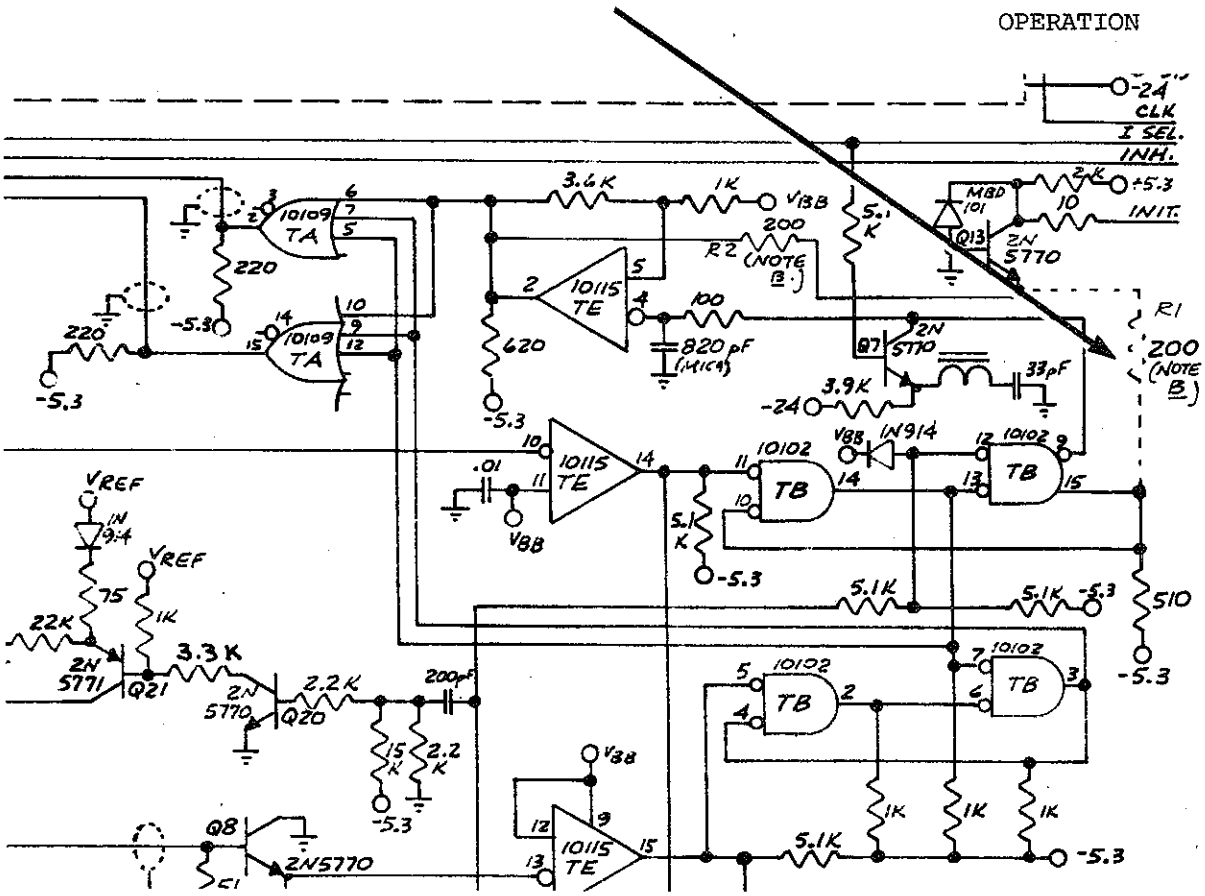
Timing Considerations for Utilization of TDC at >500 nsec Full-Scale Settings:

The Model 2228 begins charging its integrating capacitor upon receipt of the common start pulse. The constant current source rundown also begins immediately. On the standard unit, an automatic stop is generated (for channels which received no Stop inputs) and the oscillator is automatically started about 1.2 times the full-scale time range setting after the Start pulse. Since the run-down has been taking place since the Start pulse was received, a number of 5 nsec-spaced clock pulses (20 MHz clock) will not be counted. This introduces a small constant time error into the result which can be calibrated out by using different cable lengths for Start and Stop inputs (this also should be done to compensate for the larger constant errors which are introduced by the fact that a start-stop interval of approximately 2.4 nsec is required before any counts are seen at all). The effect of the 100 nsec range is about 2.5 counts out of 1000 full scale or 0.25% on the 200 nsec range, it is 5 counts of 0.5%; on the 500 nsec range, it is 12 counts or ≈1.2%.

For users desiring a 1 μsec full-scale range (achieved simply by readjusting the 500 nsec range potentiometer) such as might be needed on drift chamber applications, this effect would total 24 counts or ≈2.4%. Compensation for this would necessitate an additional 24 nsec of delay cable. To eliminate this necessity, it is possible (requiring a single resistor modification) for the 2228 to trigger the oscillator with the leading edge of the start input. The turning on of the oscillator within the timing interval now adds a small amount of noise to the integrating capacitor. Although this noise would tend to hinder the linearity measurement for a 100 nsec full-scale range, it is integrated out in the 1 μsec range and in the end contributes quite negligibly to non-linearities.

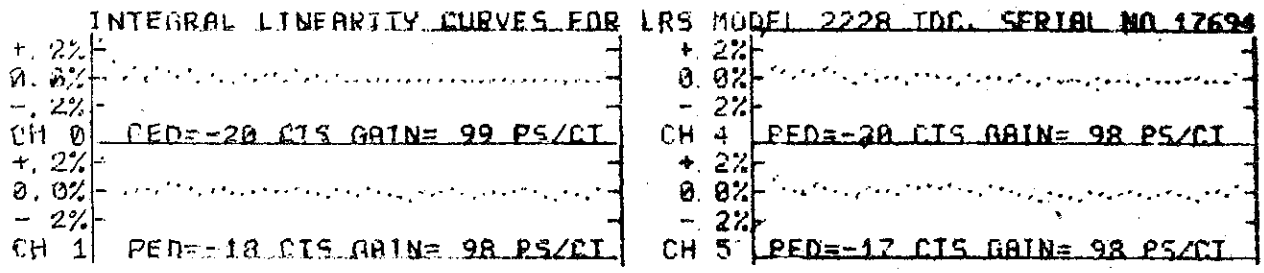
The effect described above is especially substantial in the higher range positions of units modified for 1, 2, and 5 μsec ranges. Therefore, when these optional time ranges have been factory performed, (on units with ECO* numbers greater than 801) the correct change cah be made to the oscillator-enabling circuit. The modification is shown following, and is also indicated on all LRS 2228 schematics indicating an ECO* number greater than #801.

*Engineering Change Order

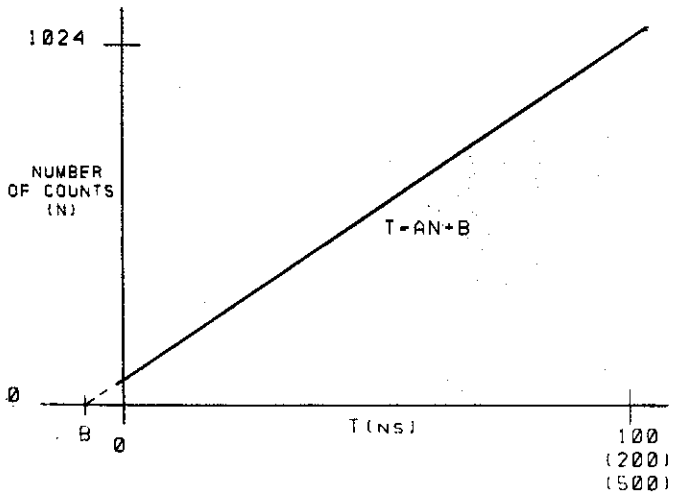


Start-Stop Input Time Jitter and Drift: Each Start and Stop input has a "threshold" level which is affected by several factors (e.g., the base-emitter drop of an input emitter follower, etc.). If these factors were to change with temperature, voltage, or time variations, the risetime of the input pulses (if not equal to zero) would cause triggering at different amplitude level, resulting in a small time jitter and/or drift. The effect naturally gets worse for input pulses of longer risetimes. However, in the 2228, the circuitry accepting the stop pulses and the start pulse is identical (i.e., in the example above, although the base emitter drop does change by some small amount (≈2 mV/°C), it changes nearly equally for both start and stop inputs). Therefore, if care is taken to use identical pulses (i.e., same risetime) for the start and stop inputs, the relative time difference between them will remain quite constant, regardless of how far the "threshold" drifted. It is worthwhile to note that reasonable voltage variations and time do not cause "threshold" drift of the inputs. The triggering level for both Start and Stop inputs is between -350 mV and -450 mV.

Linearity: The integral linearity of the 2228 is typically ±2.0 counts. This is defined in typical LRS terminology as the maximum deviation from the best straight line fit to measured points. A linearity calibration for all 8 channels is enclosed with each Model 2228 shipped from LRS. Vertical deviation is shown as 0.2% of full scale per division, but this is nearly identical to 2 counts. Samples of these plots are shown below.



These curves are obtained with a computer-controlled 16-bit digital-to-analog converter (DAC) which controls the exact time at which stop pulses are applied to the TDC channel under test. Stop pulses following the start pulses by 0 to 100 nsec in up to 2^{16} (65,536) equal increments are analyzed by the 2228 calibration. The data accumulated in this manner is linearly fit by the lease squares technique. The slope and intercept parameters (called "gain" and "time offset" respectively) are given for each channel.



B IS AMOUNT OF TIME OFFSET

T IS START TO STOP TIME

N IS TOTAL NUMBER OF COUNTS

A IS CONVERSION SLOPE:
I.E. A=(T+B)/N

Time Offset: If the input time vs. output counts is extrapolated to zero, it will be observed that it probably does not cross at the (zero, zero) intercept but has a finite value of counts (which may be a positive or negative number). The absolute value of this number will never be greater than 1 % of full scale.

Q and LAM Suppression: The 2228 was designed to permit the elimination of readout of empty modules to achieve maximum readout rate. A module in which all channels have received no stop pulses (i.e., all scalers overflowed) will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated.

Some branch drivers (interfaces between computer and CAMAC crate) require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations, the L-Suppress feature may be defeated by removing the jumper XZ and replacing it with jumper YZ. (See schematic sheet 3 or the circuit board section below.) In this situation a LAM condition is obtained after any Read commany. The Q-response suppress can be defeated by removing jumper VW and replacing it with jumper UW.

(NOTE: Older 2228's do not have all the jumper options available on the p.c. board. These limits will require that the bus be cut and a jumper added on the solder side of the board.)

Conversion Time: Since the full scales of the 8 channels of each 2228 may differ from each other by up to ±5%, the time for each channel to achieve a full-scale conversion may also differ from that of the other channels. Total conversion time is roughly 52 microseconds, but the user should be careful to allow at least 60 microseconds for conversion of all 8 channels. Other factors which contribute to the necessity of this margin in allowed conversion time are variations in clock frequency, variations in ramp currents, and necessity to allow for overflow. As a result, the 2228 clock is intentionally internally held on for a maximum time of 60 μsec (for any size conversion). Due to the fast clear feature of the 2228, however, this conversion time need only be awaited for valid events.

Data and Readout: The output data of the 2228 is standard CAMAC-compatible (TTL negative logic) in 10-bit binary format, plus overflow. The 10-bit digital resolution (100 pC/count in 100 nsec full-scale range) matches the overall TDC accuracy of 0.1%. The 10 bits of digitized information plus overflow bit are gated onto the R1 to R11 (2^0 to 2^{10}) Dataway but lines by F(0)·N·A, where F(0) signifies the read function, N signifies the 2228 to be read, and A (from A(0) to A(7)) signifies which TDC channel in the 2228 is to be read out. Generally, the unit is ready for readout when LAM appears. The function F(2), Read and Clear, may also be used to read information from chosed TDC channels. However, this readout is destructive only when A(7) is addressed, the F(2)·N·A(7) clearing all channels at one time. The F(2) command on addresses A(0) through A(6) will cause the TDC contents to be read with no clear and the input gate will remain disabled.

LAM: A LAM (Look-At-Me) signal is generated from end of conversion until a module Clear or Clear LAM (Z, C, F(2), F(9) or F(10)). LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable F(25) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM is suppressed for empty modules as indicated in "Q and LAM Suppression" section above.

The test function F(8) allows the LAM to be tested. In response to application of F(8)·N·A (where A is any A from A(0) to A(7)) independent of Disable LAM, a Q response will be generated if LAM is set. Although the LAM is disabled while the 2228 in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an F(8)·N·A is applied.

IMPORTANT! When current is applied to the 2228 (such as would occur when plugging a module in and turning the crate power supplies on), the states of the LAM latch and LAM enable are arbitrary. The unit must always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM) and an F(10) (Clear LAM).

Packaging and Power Requirements: The 2228 is packaged in a standard #1 width CAMAC module (conforming to ESONE Committee Report EUR4100). It dissipates a total of 8.3 watts of power.

CAUTION! Because of the adjacency of the various voltage bus connector contacts, plugging in any CAMAC unit may cause momentary misalignment of the unit and short the power pins to each other. This can cause severe damage to the module inserted, especially since the 24-volt pins are adjacent to the 6-volt pins. THUS, THE CRATE POWER SHOULD BE OFF WHEN A MODULE IS INSERTED OR REMOVED!

The Model 2228 consists of 8 independent identical TDC's and associated circuitry. Referring to the block diagram following, the 2228 circuitry is divided into seven basic sections:

A Common Start, Delayed Start and Common Stop circuit for distributing the start signal to the start-stop gates.

Eight Stop Input circuits.

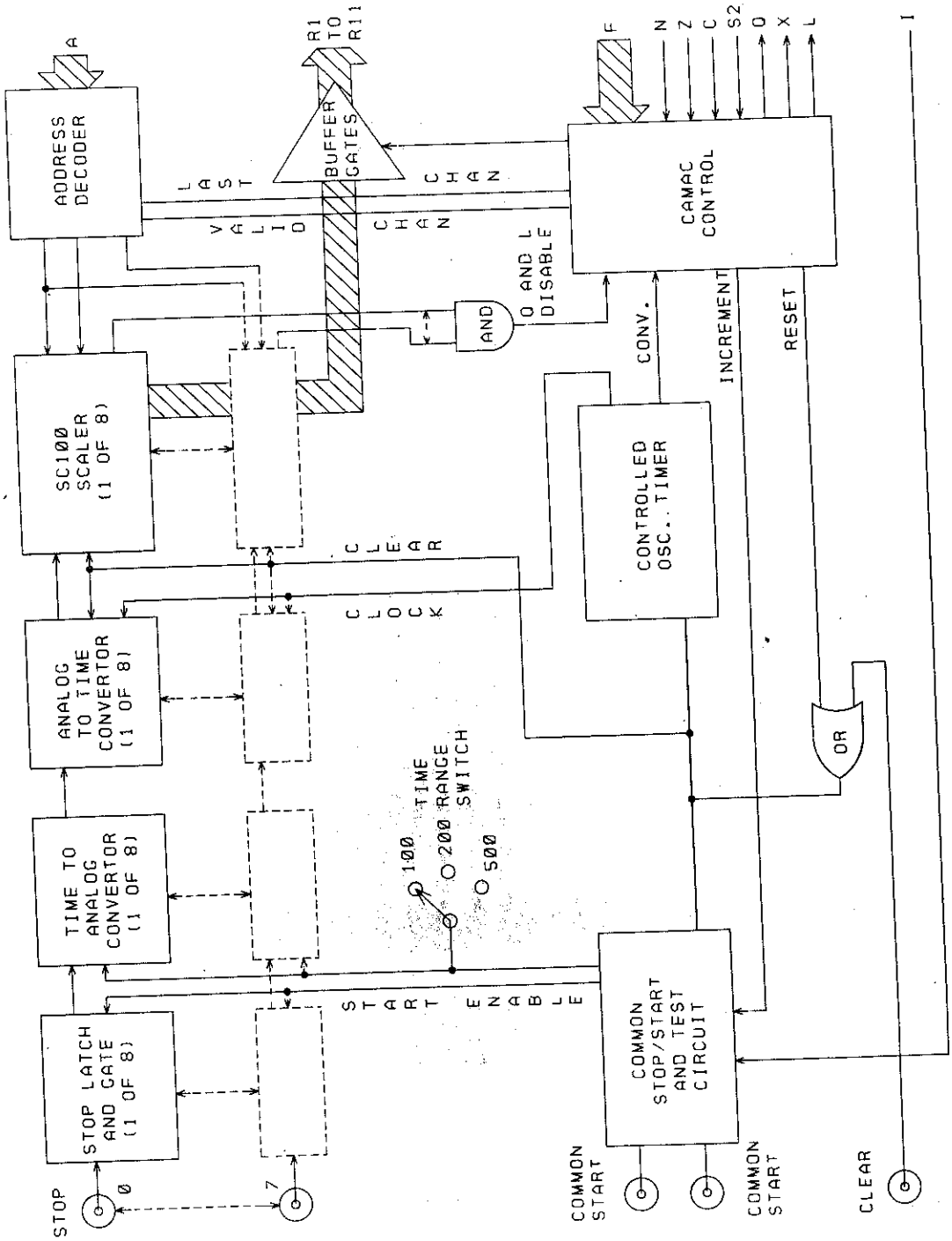
Eight Time-to-Analog Converters.

Eight Analog-to-Time Converters.

Eight Clock Synchronizers and Scalers.

A Controlled Oscillator.

A CAMAC Control Section.



BLOCK DIAGRAM - MODEL 2228 TDC

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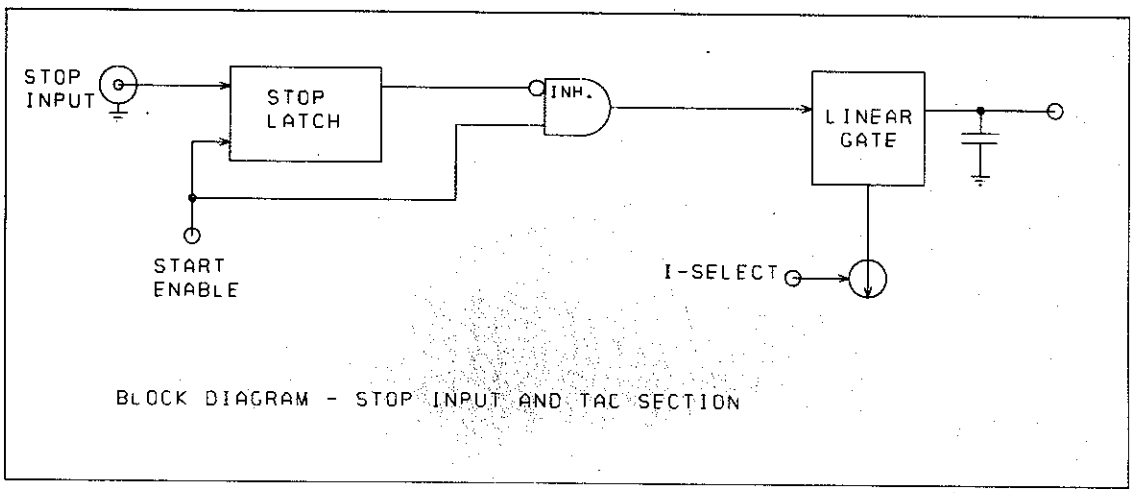
FUNCTIONAL DESCRIPTION

Start, Delayed Start, and Common Stop: The Model 2228 requires NIM-level input for the Start and Stop input, but uses ECL integrated circuits for gating and latching. This requires a -800 mV shift in logic levels which is provided by using NPN emitter followers on all inputs. Timing stability is accomplished by providing both the start channel and the stop channels with approximately the same number and type of components assembled so that delay changes (caused by temperature and voltage changes) will cancel each other.

A pulse applied to the common Start input, after receiving a voltage offset and level inversion, will set a latch (see block diagram below) formed from two ECL negative NAND gates. The latch output couples to two 3 input gates each driving the center point of 100 Ω strip line buses via 50 Ω coax. Each of the two buses provides four Stop channels with a Start Enable signal which is available until a common Stop is received, until the delayed Start occurs, or until a clear pulse is received (see next three paragraphs for explanation of three Start-Disable functions).



BLOCK DIAGRAM - STOP INPUT AND TAC SECTION

Once the Start latch is set, it will remain set until a clear pulse resets the entire module. If the common Stop latch is set, or when the delayed Start occurs (either one disabling the Start latch output), they will remain in that condition until the Start latch is cleared. Thus, once one Start pulse is received, the entire section is made immune to any further Start pulses until the entire module is properly cleared. A CAMAC Inhibit will disable the Start input emitter follower for the duration of the Inhibit.

The common Stop latch, when set, will disable the two 3-input gates, ending the Start Enable signal. The common Stop input passes through the same level shifting and inverting stages and uses the same type latch as the Start channel. The only differences are that the latch complement level is used to disable the 3 input coax drive gate and the latch is only enabled when the Start latch is set and is therefore cleared when the Start latch is cleared.

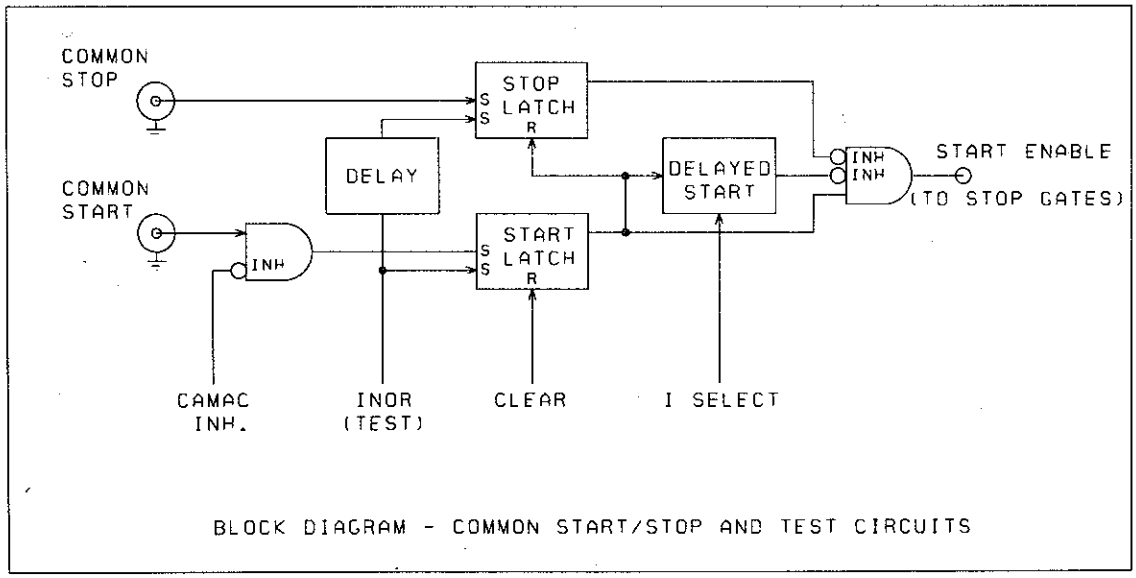
The delayed Start is a level which occurs approximately 1.2 times the full-scale time range setting. It results from a level-sensing amplifier monitoring a capacitor which is being charged via a constant current source, which was unclamped when the Start latch set. Because the current source is controlled by the I-select line, it is always proportional to the current sources in the time-to-analog circuits (see next section).

A common module clear pulse, 1.0 to 1.2 μsec long, is used to clear the Start latch and keep it clamped (therefore disabled) for the duration of clear.

The internal test capability is provided by converting the F(25)·S2 pulse to a prompt Start and delayed (approximately 80 nsec) Stop. These two pulses are emitter-ORed with the outputs of the Start input and common Stop input inverter stages.

Stop Input Circuits: The individual Stop circuits operate identically to the Common Stop (see previous section). When a Start enable signal occurs, it enables the linear gate of the Time-to-Analog Converter (TAC) stage via an ECL differential output gate. It also enables the Stop latch to be set which, until the Start enable signal appeared, was held clamped in a reset condition, preventing it from being set by a possible premature pulse at the Stop input.

Once the Stop latch is enabled, it will be set by the next Stop input pulse. (The input pulse uses the same level shifting, inverting, and latching techniques as the Start and Common Stop inputs.) When the Stop latch is set, it disables the ECL gate, thereby disabling the linear gate in the TAC.



BLOCK DIAGRAM - COMMON START/STOP AND TEST CIRCUITS

Time-to-Analog Converters: Each Time-to-Analog Converter (TAC) utilizes a constant current generator where the actual value of current is determined by the difference between the voltage on the I-Select bus and the -24 volt bus. This current is gated into an integrating capacitor for the duration of time between the common Start and a Stop; therefore the voltage on the capacitor is proportional to that time. This capacitor is then discharged by the Analog-to-Time Converter Stage.

As can be seen from sheet 2 of the schematic, the I-Select bus voltage is varied grossly to select ranges by switch selection of voltage levels of a compensated, tracking divider chain. Each range position has a fine control potentiometer which has been factory adjusted to provide the ranges shown on the side panel (and on the schematic). The 500 nsec range can be set as high as 1000 nsec (1 μsec) and used reliably.

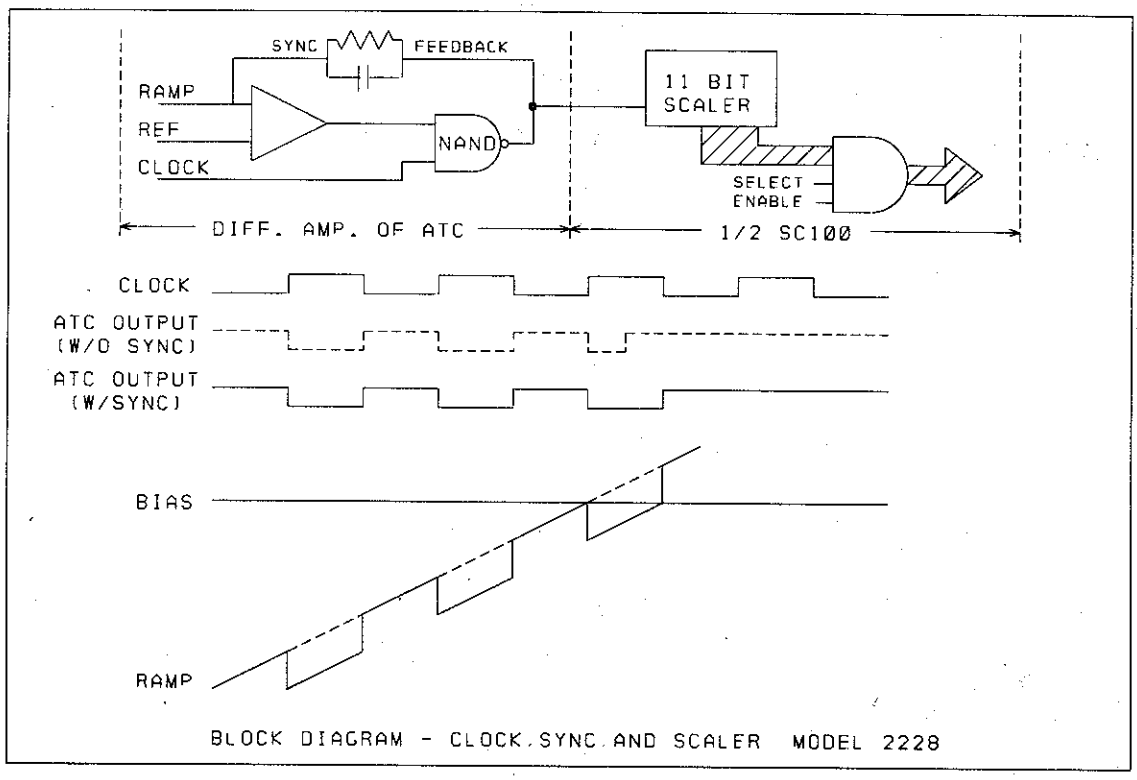
On optionally adjusted units, (for time ranges greater than 1 μsec), the resistor at the emitter of the current source is decreased (e.g., to 1/10 the indicated value for ranges of 1, 2, and 5 μsec). It is also necessary to change the emitter resistor of the current source in the delayed start circuit (see previous section) and desirable to move the 200 Ω resistor in the Initiate circuit (see Controlled Oscillator Section).

Analog-to-Time Converter: The Analog-to-Time Converter (ATC) stage is functionally the inverse of the previous TAC stage, except that the capacitor discharge rate is much slower than the charge rate was.

The charge which was delivered to the integrating capacitor through the linear gate of the TAC stage is subsequentially removed by means of a stable current source (see Block and Waveform diagram). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. (This rate is proportional to the difference between the +24 and V_{REF} inputs.) The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is more negative than a reference level (which is set by the voltage divider between +3 volts and ground). The output time duration (T_2) is therefore proportional to the input time (T_1) of the TAC where time T_2 is approximately 500 times T_1 when used in the most sensitive 100 nsec F.S. range (i.e., $T_2 = 500\ T_1$). Stable operation of the QTC is assured by the on-board stabilized V_{REF} (approximately +12 VDC) which tracks the +24 VDC supply, causing the difference (used as the current source reference) to be independent of external supply variations. Whenever necessary elsewhere in the analog circuits, tracking dividers and temperature-compensating diodes or transistors are used to remove first order drift errors.

A Clear command can be used if desired to clear the 2228 during a conversion cycle. It not only initialized all the digital control and scaler stages, but also, via a leading edge R-C differentiator, clears the analog ramp of the TAC/ATC to its quiescent level. The analog clear pulse width is about 300 nsec, leaving the 1 μsec remainder of the digital clear for settling in the analog stages.

NOTE: In earlier 2228 units, a diode was used for fast clearing the ramp. This has been replaced by a transistor for improved settling time.



BLOCK DIAGRAM - CLOCK SYNC AND SCALER MODEL 2228

Clock Synchronizer and Scaler: The output of each Analog-to-Time Converter in the 2228 is used to gate a clock into one half of an LRS hybrid SC100 Dual Eleven-Bit Scaler (see enclosed specification sheet). The oscillator is synchronously started with respect to the leading edge of the Start input pulse (see Controller Oscillator section). This insures no fractional pulses during the beginning of the rundown cycle, but care must be taken at the end of the rundown. This is done by the synchronizing output stage of the ATC. Each gate circuit (see schematic sheet 2 and block diagram) supplies an integral number of clock pulses even if the QTC output returns to its quiescent state in the middle of a clock pulse as shown in the diagram on the following page.

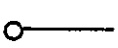
When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4, and A9 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). Along with F(0) or F(2), and N, the 11-bit data will be gated out in parallel to the CAMAC dataway.

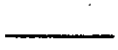
Controlled Oscillator: The clock circuit is a modified Colpitts oscillator employing a highly temperature-stable choke and a mica capacitor as its resonant elements. Its frequency is 20 MHz. The oscillator is gated on at approximately 1.2 times the full-scale range setting after the leading edge of the Start pulse. (In the optional long time range units it is gated on with the leading edge of the Start, as the clock noise becomes insignificant for long time ranges, but the value of the time offset becomes significant.) Synchronously, gating the oscillator on in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates clock noise caused by not delaying the turn-on (see block diagram). The conversion time is set to 55-60 μsec, allowing more than enough time for the nominal 50 μsec full-scale conversion to occur. This allows for the ±5% differences from channel to channel, slight temperature drifts, module-to-module variations, etc., and still insuring that an overflow can occur for oversized input pulses.

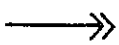
LAM and Q-Response Suppress Circuit: If none of the eight channels of the 2228 receives a Stop pulse, they will all overflow and thus there is no valid data to read out. This condition is sensed by an eight-fold transistor AND circuit (see main block diagram) and is used to clear and clamp the LAM latch (which would normally have been set by end-of-conversion) and disable the readout of the Q-response on a read function command. Disabling of the suppress function can be done for either Q-response or LAM. (See the Operation Section for more information.)

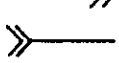
The CAMAC Control: The decoding of the CAMAC "F" functions and N if performed by a 4 line to sixteen line (an SN74154). A DC level is generated at the appropriate pin for each valid CAMAC command. Scaler addressing is accomplished using a four-line to ten-line decoder (an SN7442) on A2, A4, and A8, to enable the appropriate SC100 2-channel scaler hybrid and the A1 bit is used to select the appropriate half of the SC100. X-response is generated for all valid commands, and Q-response and LAM are generated as described in the Q and L Suppress Circuit section.

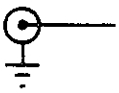
STANDARD DRAFTING SYMBOLS, ELECTRONIC


Connection to any given voltage.


Line ending at the edge of the sheet indicates continuance on another sheet.


Male pin or card edge contact.


Female pin, socket or card edge connector.


Coaxial connector.


No connection.

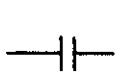

Connection.

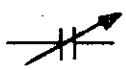

Resistor, 1/4 W, ±5%, value in ohms (unless specified otherwise).

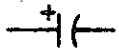
Resistor, 1/4W, ±1%, value in ohms (unless specified otherwise).

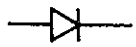

Resistor, variable, any type.

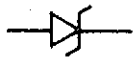

Resistor, variable, any type.


Capacitor, ceramic disc. Value in microfarads (unless specified otherwise).


Capacitor, variable. Values in Picofarads (unless specified otherwise).


Capacitor, polarized. Values in microfarads/volts (unless specified otherwise).

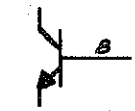

Diode, signal or rectifier.


Diode, zener.

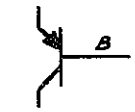

Diode, tunnel.


Diode, snap.

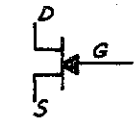

Light emitting diode (LED).



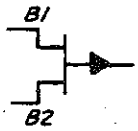
NPN Transistor.



PNP Transistor.



Field effect transistor, P Channel.

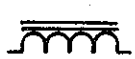


Field effect transistor, N.


Air choke.


Ferrite bead.


Ferrite core choke, Z 500 ohms when f ≥ 60 MHz (unless otherwise indicated).


Ferrite core choke, 40 uH, (unless otherwise indicated).

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West Nyack, New York

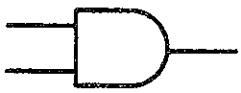
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS. TRANSISTOR - TRANSISTOR LOGIC (TTL).

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

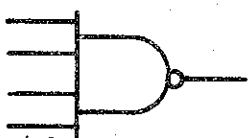
Positive logic notation is used. Logical "0" is nominally zero Volts and logical "1" is nominally 2.5 Volts.

Supply voltages of IC's are shown in a table on each schematic.

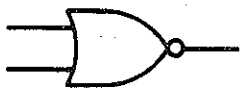
2-Input Positive NAND Gate



2-Input Positive AND Gate

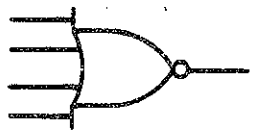


4-Input Positive NAND Gate

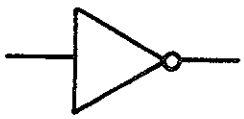


2- Input Positive NOR Gate

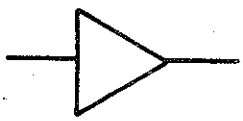
2 -Input Positive OR Gate



4-Input Positive NOR Gate



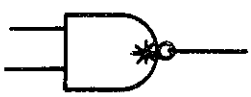
Inverter or Inverting Buffer



Non-Inverting Buffer

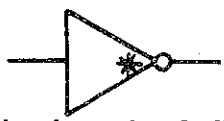
Exclusive OR Gate

Open collector outputs are identified by an asterisk (*) on the output connection.



2-Input Positive NAND Gate W/Open Collector

2-Input Positive OR Gate W/Open Collector



Non Inverting Buffer W/Open Collector

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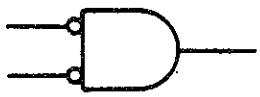
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS EMITTER - COUPLED LOGIC (ECL)

The drafting symbols used are patterned after MIL STD 806, with some modifications. Shown below are some of the more commonly used symbols. Letter designations in the IC symbols correspond to those on the printed circuit layout. (In the case of multi-channel circuits, the designation will normally consist of two letters, the first one being channel identification.) Pin connections are identified by the number located on input and output lines. (For outline drawing, see next page).

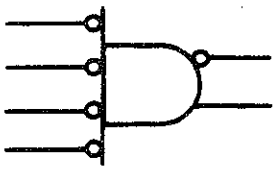
Logical "0" is nominally -0.8 Volts and logical "1" is nominally -1.6 Volts.

Supply voltages of IC's are shown in a table on each schematic.

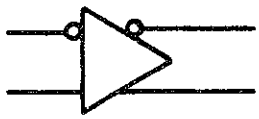
2 - Input Gate.
Negative AND (Positive OR) Gate.



2 - Input Gate.
Negative NAND (Positive NOR) Gate.

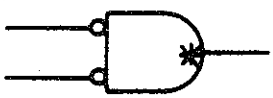


4 - Input Gate.
Negative AND/NAND (Positive OR/NOR) Gate.

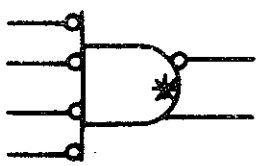


Differential
Amplifier.

Open emitter outputs are identified by an asterisk (*) on the output connection.



2 - Input Negative NAND Gate.
With Open Emitter.



A - Input Gate.
Negative AND/NAND (Positive
OR/NOR) Gate.

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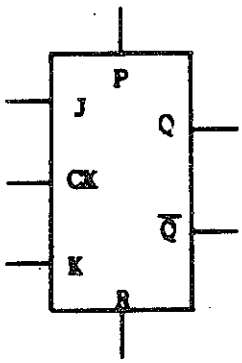
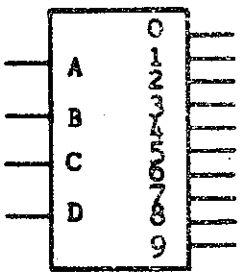
STANDARD DRAFTING SYMBOLS, INTEGRATED CIRCUITS.
TRANSISTOR - TRANSISTOR LOGIC (TTL) OR
EMITTER COUPLED LOGIC (ECL).

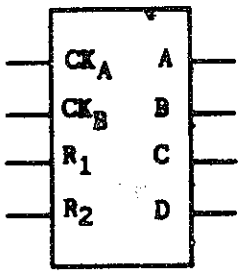
Flip-Flops and other MSI integrated circuits are generally drawn as a rectangular box with connections marked inside the outline. Some abbreviations are: R - Reset (or Clear), P - Preset (or Set), CK or CLK - Clock, etc. Some typical examples are shown below. See the manufacturer's specification for additional information.



J-K Master-Slave
Flip-Flop

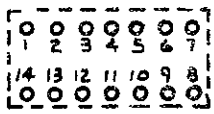


BCD-To-Decimal
Decoder-Driver



Binary Counter

Orientation of pin numbers of any DIP (Dual-In-Line-Package) is shown below. Pin 1 will normally be identified on the printed circuit board.



Bottom View

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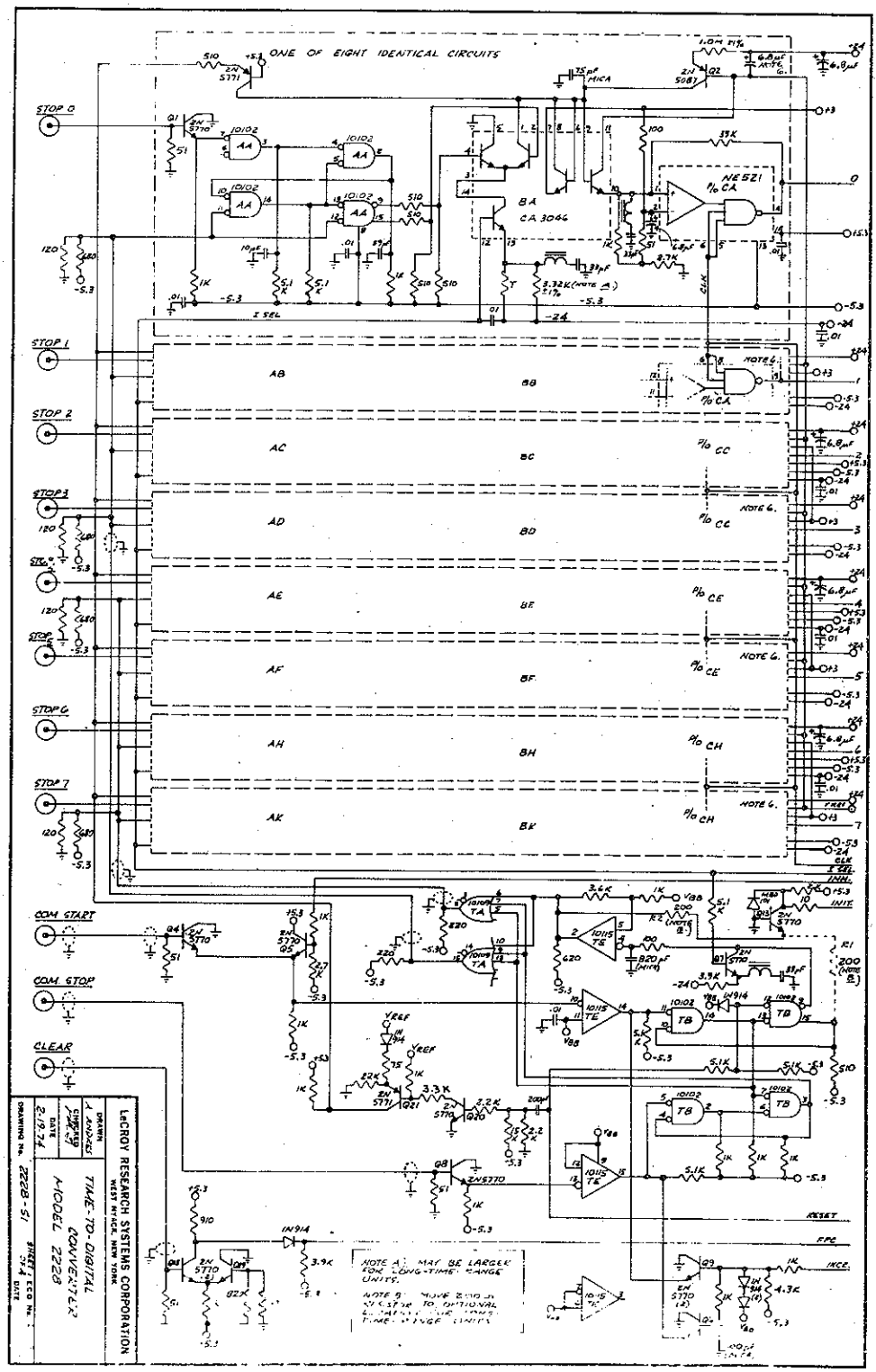
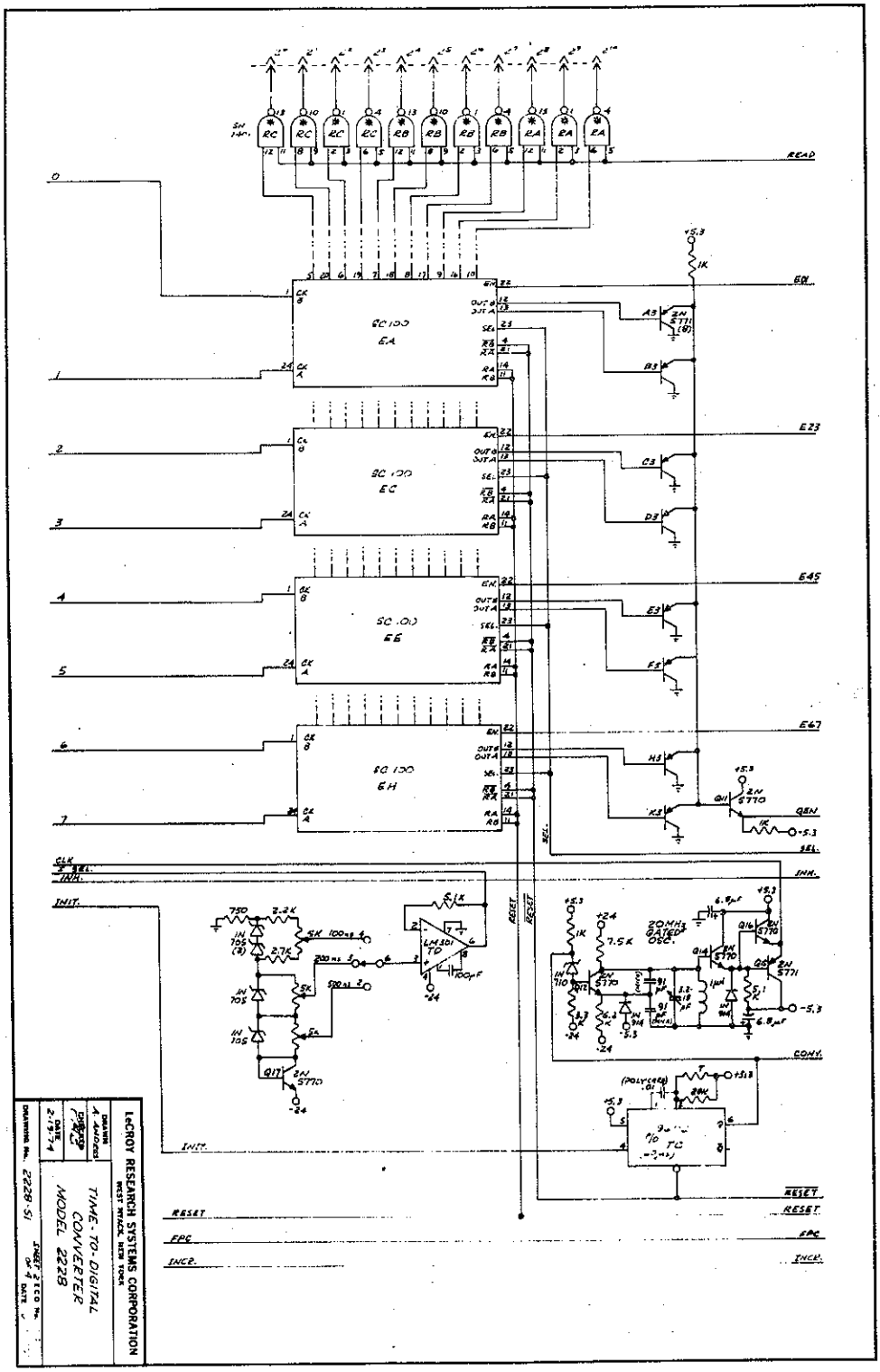
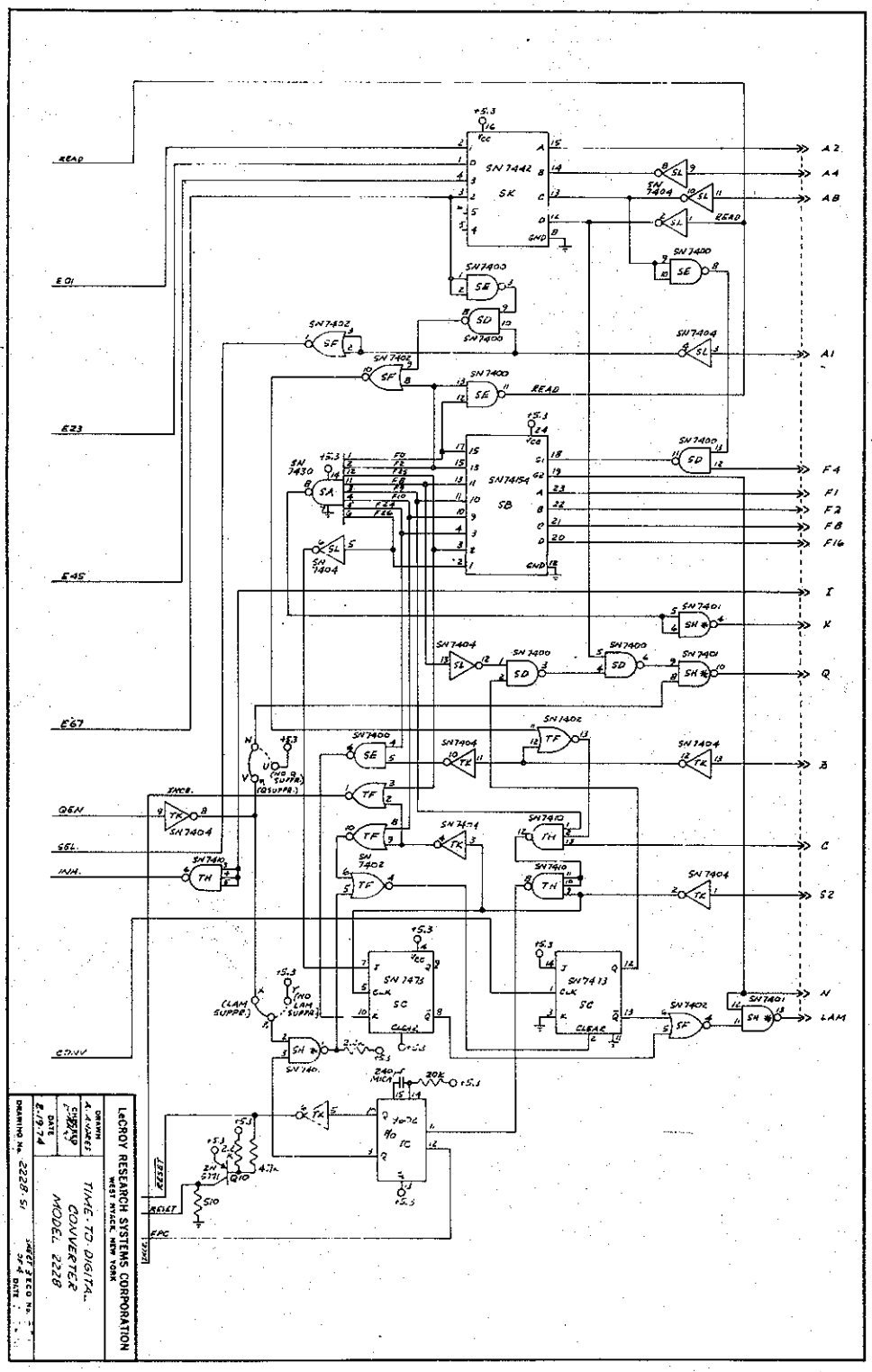

ONE OF EIGHT IDENTICAL CIRCUITS
STOP 0
STOP 1
STOP 2
STOP 3
STOP 6
STOP 7
COM START
COM STOP
CLEAR
AB
BB
AC
BC
AD
BD
AE
BE
AF
BF
AH
BH
AK
BK
NOTE A
NOTE B
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
TIME-TO-DIGITAL CONVERTER
MODEL 2228
2228-51


READ
EN
E23
E45
E67
GEN
SEL.
INH.
INIT.
RESET
EPC
INCR.
CONV.
SC 100
EA
EC
EE
EH
LM301
TO
2N 5770
2N 5771
2N 3711
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
TIME-TO-DIGITAL
CONVERTER
MODEL 228
DRAWING No. 2228-51
DATE 2-19-74



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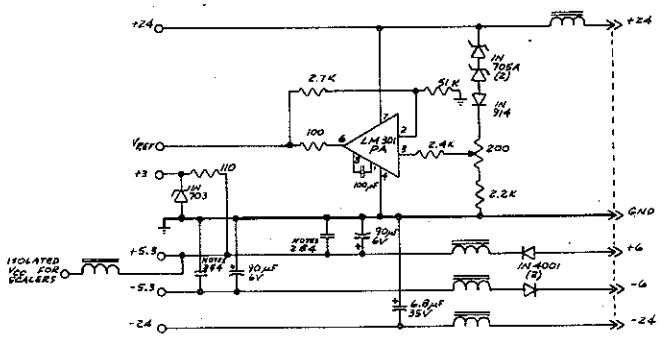
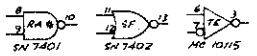
West Nyack, New York

I.C.	DESIGNATION	+24	VOLTAGE PINS +5.2V	GND	-5.2V	-24V
CA 3046	BA, BB, BC, BD, BE, BF, BH, BK	-	-	-	-	-
LM 301	PA	7		4		
LM 301	TD			7		4
MC 10102	AA, AB, AC, AD, AE, AF, AH, AK, TB			1 AND 16	8	
MC 10109	TA			1 AND 16	8	
MC 10115	TE			1 AND 16	8	
NE 521	CA, CC, CE, CH		14	7	13	
SC 100	SA, SC, SE, SH		3	2		
SN 7400	SD, SE		14	7		
SN 7401	RA, RB, RC, SH		14	7		
SN 7402	SF, TF		14	7		
SN 7404	SL, TK		14	7		
SN 7410	TH		14	7		
SN 7430	SA		14	7		
SN 7442	SK		16	8		
SN 7473	SC		4	11		
SN 74154	SB		24	12		
9602	TC		16	8		



NOTES:
1). "T" DENOTES VALUE TO BE CHOSEN AT TEST.
2). ADDITIONAL .01 CAPACITORS PLACED ALONG VOLTAGE BUS.
3). UNUSED GATES:



4). ADDITIONAL 6.8μF CAPACITORS ON VOLTAGE BUSES.
5). IN914 DIODES MAY BE IN4448 OR IN4148.

LECROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN: A. AUGERES
CHECKED:
DATE: 2-19-74

TIME-TO-DIGITAL CONVERTER
MODEL 2228

DRAWING No. 2228-2

Technical Information

BASIC
CAMAC DATAWAY
OPERATING INFORMATION

Condensed from:

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Ispra Establishment -- Italy
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LeCroy Research Systems Corp.

INTRODUCTION

CAMAC is an international standard of modularized electronics as defined by the ESONE Committee of the JNRC, Ispra. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized multi-receptacle which, in turn, may be interfaced to a computer. In this way, additions to a data transfer and control system may be made by plugging-in additional modules and making suitable software changes. Thus, CAMAC allows information to be transfered into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC Crate which has 25 Stations, numbered 1 through 25. Station 25, the rightmost station, is reserved for a Crate Controller, whereas Stations 1 - 24 are Normal Stations used for CAMAC Modules. Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC Commands to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Data transfer, control functions, and module powering is affected via the Dataway. This is a series of bus and individual lines across the back of the crate. The dataway lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Page 18C for a pin allocation chart.

In a typical dataway operation, the crate controller issues a CAMAC Command which includes specifying a station number (N), a subaddress (A), and function code (F) (see Page 17C). In response, the subaddress of the module will generate valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a read command, the controller reads data contained within a module.

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USE OF THE DATAWAY LINES

Communication with plug-in units takes place through the Dataway. This passive multi-wire highway is incorporated in the crate and links the 86-pin sockets to all stations. The bus-lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified Dataway wiring but can be connected to individual points to which patch leads may be attached.

During a Dataway operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus-lines to specify a sub-section of the module or modules, and signals on the Function bus-lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus-line, which is available at all stations to indicate that a Dataway operation is in progress.

When a module recognizes a Read command, calling for a data transfer to the controller, it establishes data signals on the Read bus-lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus-line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus-lines. The strobes are used to transfer data from the Dataway into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that is requires attention. Three common controll signals are available at all stations, without requiring addressing by a command, in order to Initialize all units (typically after switch-on), to Clear data registers, and to Inhibit features such as data-taking.

DEFINITION OF COMMANDS

A command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a sub-section of the module or modules (by the four sub-address bus-lines), and the function to be performed (by the five function bus-lines). The command signals are maintained for the full duration of the operation on the Dataway. They are accompanied by a signal on the Busy bus-line which indicates to all units that a Dataway operation is in progress.

Station Number (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the left-hand end as viewed from the front, beginning with Station 1.

Sub-Address (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus-lines. These signals are decoded in the module to select one of up to sixteen sub-addresses, numbered in decimal from 0 to 15.

Function (F16, F8, F4, F2, F1)

The function to be performed at the specified sub-address in the selected module or modules is defined by the signals on the five F bus-lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the Dataway Command Operations section.

Strobe Signals (S1 and S2)

Two strobe signals S1 and S2 are generated in sequence on separate bus-lines. These signals are used to transfer information between plug-in units via the Dataway or to initiate operations within units. In either case the specific action is determined by the command present on the Dataway. Both strobes are generated during each Dataway command operation, and all plug-in units which accept information from the Dataway do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the Dataway lines. All units which accept data from the Dataway in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of Dataway signals, for example, clearing a register whose output is connected to the Dataway.

DATA

A common parallel highway is used for all transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24)

The controller or other common data source generates data signals on the W bus-lines at the beginning of any 'Write' operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

The Read Lines (R1-R24)

Data signals are set up on the R bus-lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the Dataway operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus-lines at the time of the Strobe S1.

STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), and Response (Q) lines.

Look-at-Me (L)

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the Dataway line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, Initialize, or by the performance of the specific action which generated the request.

Dataway Busy (B)

The Busy signal is used to interlock various aspects of a system which can compete for the use of the Dataway. Specifically, it is generated during Dataway command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the Dataway lines.

Response (Q)

The Q bus-line is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module.

On all Read and Write commands the signal on the Q bus-line remains static from the time the command is received until S2. For all other commands the signal on the Q bus-line may change at any time.

COMMON CONTROLS

Common control signals operate on all modules connected to them, without requiring to be addressed by a command. In order to provide protection against spurious signals the Initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

Initialize (Z)

The Initialize signal has obsolute priority over all other signals or controls. It sets all units to a basic state by resetting all resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

Inhibit (I)

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 ns.

Clear (C)

This common signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and 3 to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

PRIVATE WIRING

Patch Leads (P1-P7)

Five pins (P1 to P5) on the 86-way socket at normal stations are not prewired to Dataway lines but are freely available for local connections. At the control station seven pins (P1-P7) are available. Signals on the patch pins must either remain static when B is present or have rise and fall times not less than 20 ns.

DATAWAY COMMAND OPERATIONS

A command is composed of signals on the Station Number line or lines, the Sub-Address lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status information on the Q line. The two Strobes S1 and S2 must be generated in each Dataway command operation and control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 2. In this table the term 'register' is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the 4 sub-address lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command then the performance of that command should be reset the Look-at-Me source.

Read Commands (Function Codes 0-7)

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus-lines. Data signals are set up on the R bus-lines by the module as soon as the 'Read' command is recognized, and the appropriate status signal connected to the Q bus-line. The R and Q signals reach a steady state before S1, and are maintained for the full duration of the Dataway command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have cosecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Read command. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

Code 0, Read Group 1 Register

This command selects, by sub-address, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

Code 1, Read Group 2 Register

Same as Code 0, except command selects register from the second group.

Code 2, Read and Clear Group 1 Register

Same as Code 0, except the module register is cleared at time S2.

Code 3, Read Complement of Group 1 Register

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

Code 4 - 7

Unassigned at this time.

CONTROL COMMANDS (Function Codes 8 - 15)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed on the Q bus-line in any of these commands. The signal on the Q bus-line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by strobe 2.

Code 8, Test Look-at-Me

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus-line.

Code 9, Clear Group 1 Register

This command selects, by sub-address, a register from the first group in the module and clears the contents of this register.

Code 10, Clear Look-at-Me

Same as Code 8, except the Look-at-Me source is cleared at time S2.

Code 11, Clear Group 2 Register

Same as Code 9, except command selects register from the second group.

Code 12-15

Unassigned at this time.

WRITE COMMANDS (Function Codes 16-23)

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus-lines. The controller or other common data source generates data signals on the W bus-lines at the beginning of the "Write" operation. The module connects the appropriate status signal to the Q bus-line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the Dataway command operation unless the status of the signal source is changed at Strobe 2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Write function. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

Code 16, Overwrite Group 1 Register

This command selects, by sub-address, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus-lines by the controller.

Code 17, Overwrite Group 2 Register

Same as Code 16, except command selects register in the second group.

Code 18, Selective Overwrite Group 1 Register

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

Code 19, Selective Overwrite Group 2 Register

Same as Code 18, except command selects register in the second group.

Code 20 - 23

Unassigned at this time.

CONTROL COMMANDS (Function Codes 24 - 31)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed by the Q bus-line in any of these commands. The signal on the Q bus-line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by strobe S2. Precautions must be taken to ensure that information is not lost due to Q signals appearing between S1 and S2.

Code 24, Disable

This command selects, by sub-address, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

Code 25, Increment Preselected Registers

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the sub-address.

Code 26, Enable

This command enables the feature of the module selected by the sub-address, e.g., a Look-at-Me source or a data input.

Code 27, Test Status

This command selects, by sub-address, any feature of a module other than a source of a Look-at-Me request, and tests it by producing a response on the Q bus-line.

Code 28 - 31

Unassigned at this time.

DIGITAL SIGNAL STANDARDS ON THE DATAWAY

The potentials for the binary digital signals on the Dataway lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic '0' and the low state (near ground potential) corresponds to logic '1'. Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the '0' state.

It is an essential feature of the Dataway that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one controller-like unit in a crate. The Inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during Dataway operations.

Voltage standards for Dataway Signals

All Dataway Signals must conform to the voltage levels as follows:

Pull-up current sources for all Dataway bus-lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is one and only one current source per line. The minimum pull-up current when the Dataway line is at +3.5 V is defined in Table 4 as 2.5 mA but, if the controller generates Dataway signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals and for the L signals in the unit receiving the signals so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller) together. The Q and R lines will generally have many units generating the signals (say 20) with a few units (maximum 4) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

Timing of Dataway Signals

The sequence of events during a single Dataway operation is shown in Timing Diagram, Page 13C, by means of simplified signal waveforms. The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the '1' state. Other command and data lines may, of course, be in the '0' state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchroism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earlies time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t_0 - t_9, with the following significance:

Points t_0, t_3, t_6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal Dataway with no capacitative loading.

Points t_9, t_5, t_8 represent similarly the initiation of the positive-going edges of the same signals.

Points t_2, t_{11} are the latest times at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

Points t_1, t_3, t_4, t_7 represent the latest times at which the received signals are permitted to reach a maintained '1' state, and therefore refer to the last negative-going transition across the + 0.8 V threshold.

Points t_6, t_9, t_{10}, t_{12} represent the latest times at which the received signals are permitted to reach a maintained '0' state, and therefore refer to the last positive-going transition across the + 2.0 V threshold.

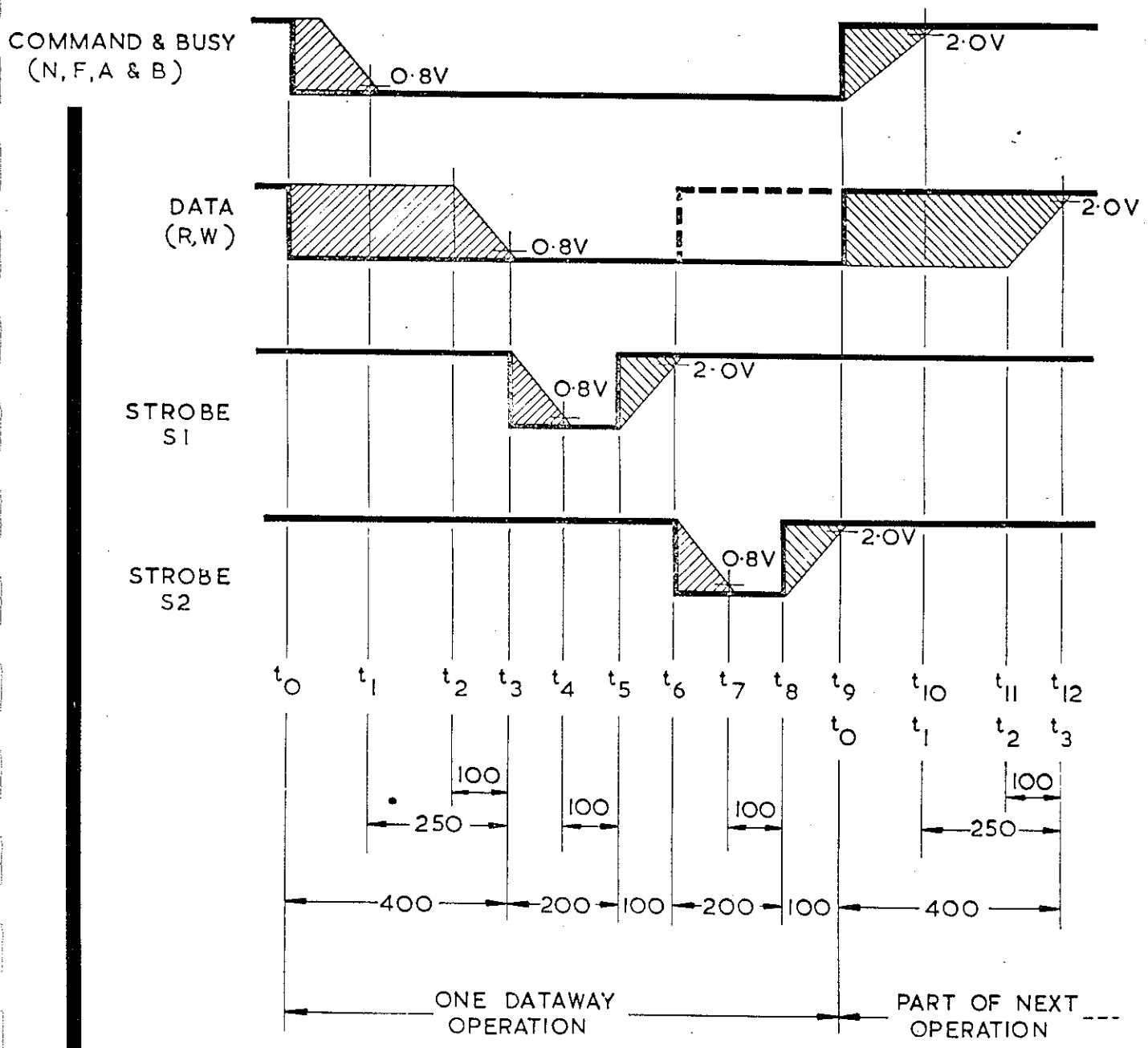
Controllers must initiate the negative and positive going edges of the command and strobe signals at intervals not less than those defined by t_3, t_5, t_6, t_8 and t_9. Modules respond to the command within the most adverse value of $(t_1 - t_2)$; i.e., 100 ns. The electrical characteristics of the Dataway and connections from it into units must allow signals to rise and fall within the minimum times for $(t_0 - t_1)$, $(t_2 - t_3)$ etc.

The next Dataway operation must not start before t_9.

The extreme case is shown in Timing Diagram, Page 15C, with the next operation starting at t_9, so that $t_9 - t_{12}$ of one operation coincide with $t_0 - t_3$ of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data there could be a complete absence of signal transitions between t_0 and t_3.

Technical Information

DATAWAY TIMING



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

TIMING OF A DATAWAY OPERATION.

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LeCroy Research Systems Corp.

Technical Information

POWER SUPPLIES

The voltage tolerances and current loadings are specified below. The specified tolerances in voltage refer to the voltage measured at the contacts of the Dataway sockets and must be maintained under the worst combination of factors such as a.c. mains voltages and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

Note that the maximum currents stated in the below table are subject to the over-all restrictions as follows:

1. The current carried by any contact of the Dataway socket must not exceed 3 A.
2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.
3. The power dissipation per single width station should not, therefore, normally exceed 8 W; however, under special circumstances this rating may be increased to a maximum of 25 W provided suitable precautions are taken to comply with total power dissipation and current loadings.

The resistance between any point on the Dataway OV power return bus-line and the point at which the power supply is joined to the crate wiring must not exceed 2 milliohms.

Technical Information

Supply Voltage	Voltage Tolerance	Maximum Current Loads	
		In the Plug-in (per unit width) See Notes (1) & (3) Above	In the crate See Note (2) Above
Mandatory			
+24V d.c.	± 0.5%	1A	6A
+ 6V d.c.	±2.5%	2A	25A
- 6V d.c	±2.5%	2A	25A
-24V d.c	±0.5%	1A	6A
OV			
Additional (as required)			
+200V d.c.	+60V, -20V		0.1A
+ 12V d.c.	± 0.5%		
- 12V d.c.	± 0.5%		
117V a.c.	+10%, -12%		0.5A

CAMAC FUNCTION CODES

Function No.	Function	Function Line Coding					
		F 16	F 8	F 4	F 2	F 1	No.
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look at Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look at Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Overwrite Group 1 Register	1	0	0	1	0	18
19	Selective Overwrite Group 2 Register	1	0	0	1	1	19
20	Non-standard	1	0	1	0	0	20
21	Reserved	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Reserved	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Increment Preselected Registers	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

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Technical Information

PIN ALLOCATION AT NORMAL STATION

VIEWED FROM FRONT OF CRATE

Free Bus Line	P1	B	Busy Bus Line
Free Bus Line	P2	F16	Function Bus Line
Individual Patch Point	P3	F8	Function Bus Line
Individual Patch Point	P4	F4	Function Bus Line
Individual Patch Point	P5	F2	Function Bus Line
Command Accepted	X	F1	Function Bus Line
Bus Line with Patch Point – Inhibit	I	A8	Sub–Address Bus Line
Bus Line with Patch Point – Clear	C	A4	Sub–Address Bus Line
Individual Lines with Patch Points – Station Number	N	A2	Sub–Address Bus Line
Individual Lines with Patch Points – Look-at-Me	L	A1	Sub–Address Bus Line
Bus Line – Strobe 1	S1	Z	Initialize Bus Line
Bus Line – Strobe 2	S2	Q	Response Bus Line
	W24	W23	
	W22	W21	
	W20	W19	
	W18	W17	
	W16	W15	
24 Write Bus Lines	W14	W13	
	W12	W11	
W1 = least significant bit	W10	W9	
W24 = most significant bit	W8	W7	
	W6	W5	
	W4	W3	
	W2	W1	
	R24	R23	
	R22	R21	
	R20	R19	
	R18	R17	
	R16	R15	
24 Read Bus Lines	R14	R13	
	R12	R11	
R1 = least significant bit	R10	R9	
R24 = most significant bit	R8	R7	
	R6	R5	
	R4	R3	
	R2	R1	
Reserved for –12 volts D.C.	–12	–24	–24 volts D.C.
Reserved for +200 volts D.C.	+200	–6	–6 volts D.C.
Reserved 117 volts A.C. Live	ACL	ACN	Reserved for 117 volts A.C. Neutral
Reserved	Y1	E	Reserved for Clean Ground
Reserved for +12 volts D.C.	+12	+24	+24 volts D.C.
Reserved	Y2	+6	+6 volts D.C.
0 volts (Power return)	0	0	0 volts (Power Return)

Control Station is identical except that:

(1) Even numbered R and W lines are used for L.
(2) Odd numbered R and W lines are used for N.
(3) Pins P1 and P2 are individual patch points.
(4) Pins N and L become P6 and P7.

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Technical Information

STANDARD DATAWAY USAGE

Title	Designation	Pins	Use at a Module
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8.	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16.	5	Defines the function to be performed in the module.
Timing			
Strobe 1.	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2.	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1 – W24	24	Bring information to the module.
Read	R1 – R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Response	Q	1	Indicates status of feature selected by command.
Busy	B	1	Indicates that a Dataway Operation is in progress.
Command Accepted	X	1	Indicates recognition of a valid command.
Common Controls			Operate on all features connected to them, no command required.
Initialize	Z	1	Sets module to a defined state. (Accompanied by S2 and B)
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears Registers. (Accompanied by S2 and B)
Private Wiring			
Free Bus Lines	P1 – P2	2	Free for unspecified common connections.
Patch Points	P3 – P5	3	Free for unspecified interconnections.
Mandatory Power Lines			The Crate is Wired for Mandatory and Additional Lines
+24V D.C.	+24	1	
+ 6V D.C.	+6	1	
– 6V D.C.	–6	1	
–24V D.C.	–24	1	
OV	0	2	Power return.
Additional Power Lines			Lines are Reserved for the Following Power Supplies
+200V D.C.	+200	1	Low current for indicators etc.
+ 12V D.C.	+12	1	
– 12V D.C.	–12	1	
117V A.C. (Live)	ACL	1	
117V A.C. (Neutral)	ACN	1	
Clean Ground	E	1	Reference for circuits requiring clean ground.
Reserved	Y1, Y2	2	Reserved for future allocation.
TOTAL		86	

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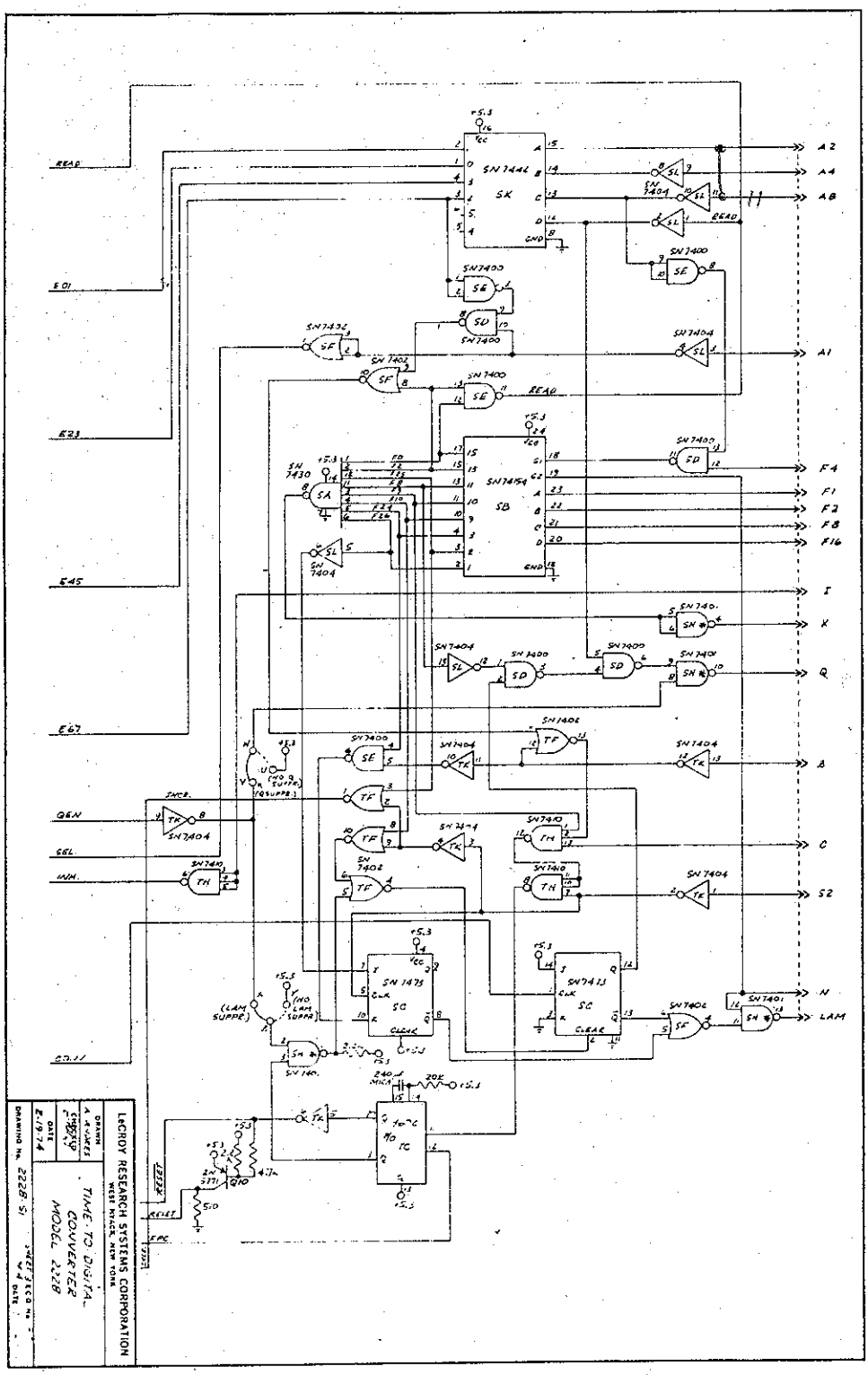

mod for Sauli
no Q for A(2)

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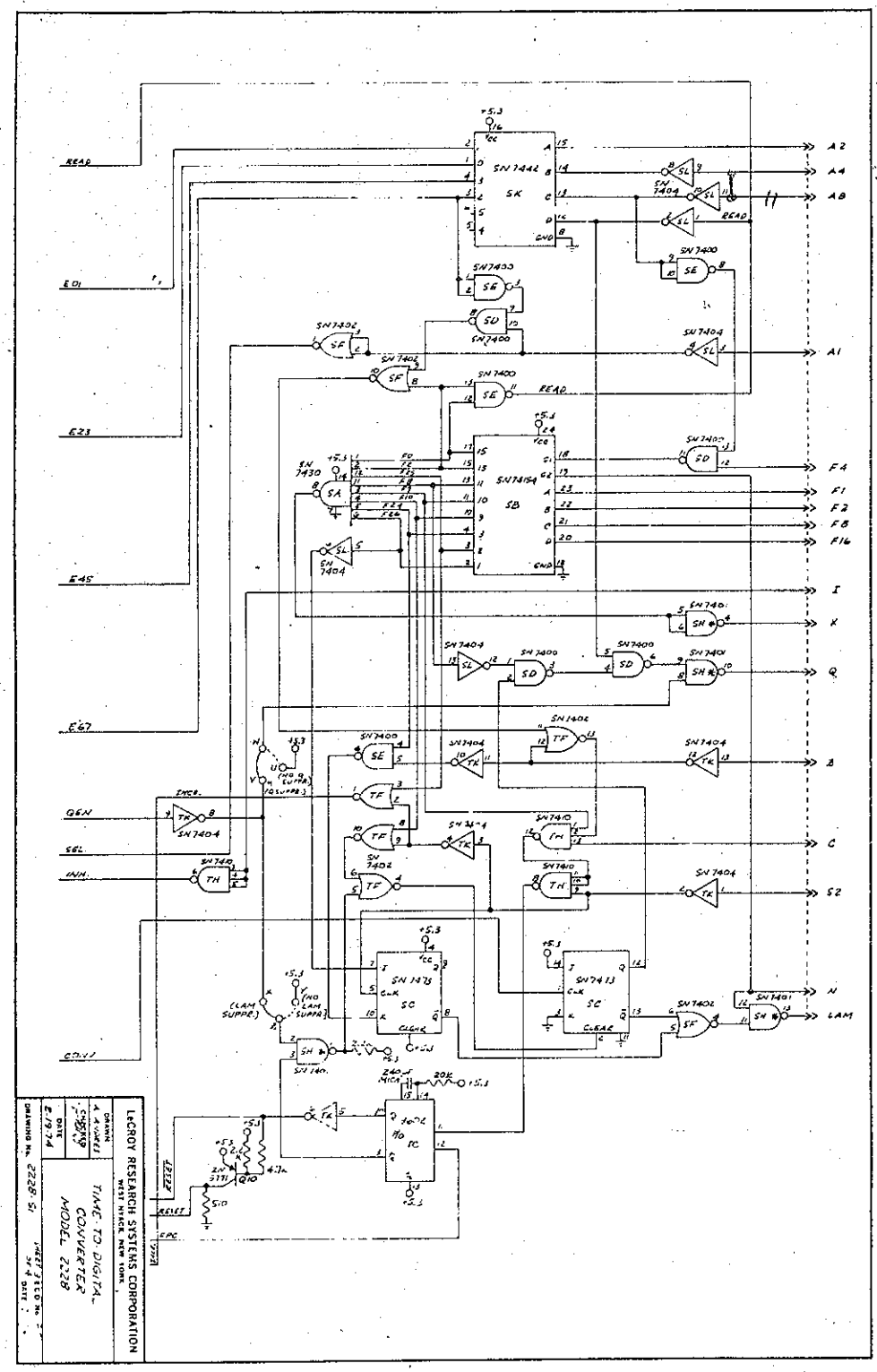

mod for Sauli
no Q for A(4)

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West Nyack, New York