MODEL 2228A/2229

OCTAL TIME-TO-DIGITAL CONVERTER

2229 VERSION

February, 1985

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CAMAC
Multiple Input Time Digitizers

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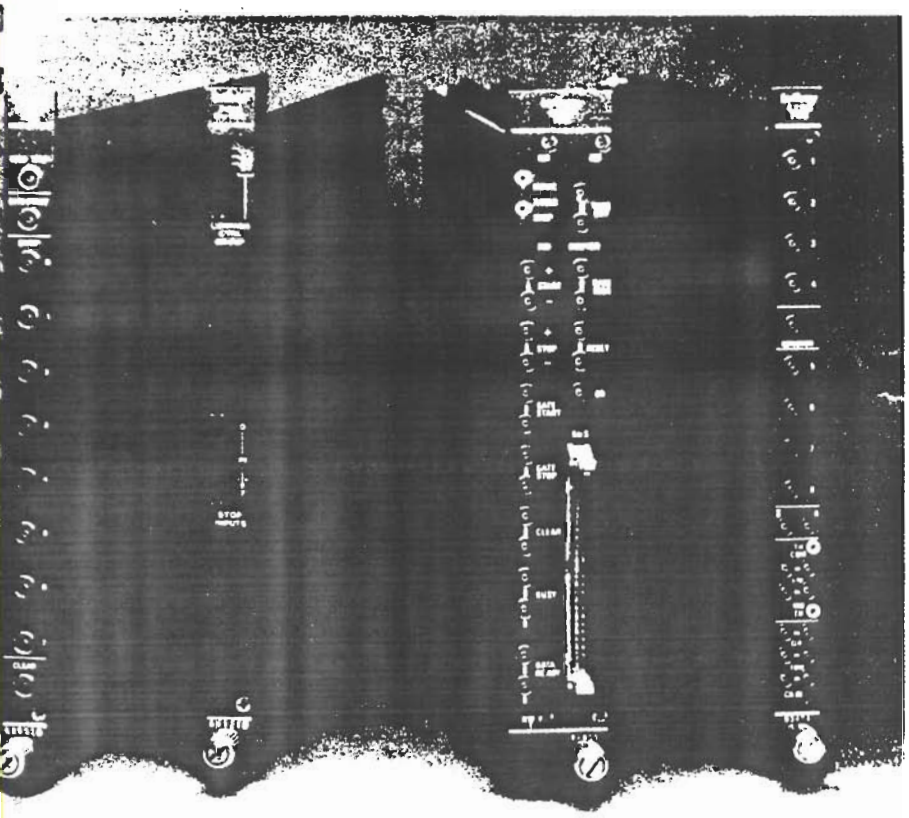


- **Full Scale Ranges from 100 nsec to 167 msec**
- **LSB Resolution from 30 psec to 2.56 μsec**
- **Single and Multiple Input Digitizers**
- **Single Hit, Multihit and Multisource Devices**
- **No (Real Time) or Very Low Conversion Time**
- **NIM, TTL and ECL Signal Level Compatibilty**

FLEXIBLE CONFIGURATIONS FOR PRECISE MEASUREMENTS

LeCroy time digitizers offer precise, fast measurements of time intervals in a large variety of industrial, government laboratory and university research environments.

These four modular CAMAC (IEEE-583) instruments permit flexible configurations tailored to the measurement problem. For example, a single instrument can simultaneously digitize eight time intervals from eight different detector elements to 50 psec LSB. Multiple signals from a single detector can have their absolute or relative time of arrival recorded in another device with 1 nsec LSB and no conversion time before readout. Another instrument can monitor up to 16 sources of signal and digitize the arrival of the first. Time interval data can be histogrammed without prior knowledge of the order of the START and STOP signals at a rate of 1 MHz and better than 160 psec accuracy.

Applications for LeCroy time digitzers include time-of-flight spectroscopy, particle beam accelerator monitoring, Muon Spin Rotation measurements, laser induced chemical studies and digital signal analysis.

FEATURES

Modular System: Can be customized to the particular time measurement application. Four time instruments to choose from with auxiliary modules.

High Density: Ideal for multi-input data acquisition.

Flexible Inputs: Several input signal standards to simplify input signal conditioning.

High Performance: Characteristics include high resolution, long range and fast throughput.

GENERAL

Electronic time interval measurement involves digitizing the time between two or more pulses. The first pulse is usually called START and the latter called STOP. For devices in which the order is reversed or unknown, a single COMMON input is used, against which INDIVIDUAL or STOP inputs are timed.

Two other configurations may also be employed. First a MULTIHIT digitizer accepts a COMMON or START input, then digitizes several INDIVIDUAL or STOP pulses which arrive on the same cable. A second variation is called MULTISOURCE, where many inputs are present but only the first to arrive is digitized. In the latter case the source of the input which is digitized is also identified.

Instrument Selection Chart

Model	Channels	Input Signal levels	Minimum Least Count	Dynamic Range	Minimum Full Scale	Conversion Time
2228A	8	NIM levels	50 psec	11-bit	100 nsec	100 μsec
2229	8	ECL levels	50 psec	11-bit	100 nsec	100 μsec
2229 Mod 400	8	ECL levels	30 psec	11-bit	60 nsec	100 μsec
4204	1 (16)*	High impedance ±1.5 V, ECL	156 psec	24-bit	2.4 msec	< 1 μsec
4208	8**	50 Ω±1.5V	1 nsec	24-bit	±8.3 msec	no conversion time

*Model 4204 Multisource input, first input for the 16 received is digitized

**Model 4208 may be configured as fewer channels of multihit.

All LeCroy Time Digitizers are modular instruments in the CAMAC IEEE-583 Standard (see LeCroy Application Note AN-33 "Introduction to CAMAC" for details). Several instrument housings are available with different capacity and power options. Interface from the CAMAC environment may be via the CAMAC Branch Highway directly into computer or via an IEEE-488 (GPIB) interface (LeCroy CAMAC Model 8901A) and others.

LeCroy Application Notes describe many applications for these high performance instruments.

FUNCTIONAL DESCRIPTION

Model 2228A, Model 2229 Octal Time Digitizer

The LeCroy Models 2228A and 2229 are octal time digitizers packaged in single-width CAMAC modules (see LeCroy Application Note AN-33 "Introduction to CAMAC"). They incorporate all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals. Internally, the 2228A and 2229 are identical. They differ only in that the 2228A accepts NIM level inputs while the 2229 requires complementary ECL (Emitter Coupled Logic) logic levels.

The Models 2228A and 2229 have eight independent channels, each of which measures the time from the leading edge of a common START pulse to the leading edge of its individual STOP pulse. Each channel disregards any STOP pulses received before a START signal and will accept only one STOP for every START.

Conversion begins upon receipt of the START signal and proceeds until one of the following: a STOP signal is received; the cycle is terminated by the application of a front-panel CLEAR signal; or the digitizer reaches full scale.

The 2228A or 2229 converts the measured time intervals into 11-bit digital numbers using a 20 MHz internal clock for a full-scale digitizing time of 100 μsec. Rear-panel control of full scale and conversion slope

permits digitization to fewer bits and correspondingly shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. A CAMAC LAM (Look-At-Me), if enabled, is generated at the end of the conversion interval to signal readout.

Three switch-selectable full-scale time ranges, 100, 200 and 500 nsec, are digitized to 95% of 11 bits (2048 counts) and provide 50, 100 and 250 psec resolutions respectively. Higher accuracy, 30 psec resolution (60 nsec range) is available with the Mod 400 option.

On-line testing is facilitated by either a front-panel COMMON STOP input or by a CAMAC command. A signal at the COMMON STOP input generates simultaneous stops for each channel, permitting accurate testing of the module.

Excessive system deadtime due to false starts may be eliminated through use of the FAST CLEAR input. Accepting NIM level signals, this input allows the digitizer to be cleared at any point in its conversion cycle without the necessity for CAMAC operations.

Model 4204 Multisource, Time Interval Meter

The Model 4204 Time Interval Meter is a general purpose time measurement instrument designed for research and industrial monitoring applications requiring fast encoding or conversion times, high precision, and long time ranges.

In less than a microsecond, the Model 4204 Time Interval Meter encodes the measured time interval into a 32-bit word. By selecting the required resolution (down to 156.2 psec), a specific subset of 24 bits of the dataword may be read. Several overflow options are included and both the designated overflow and an overall data offset can be set via CAMAC control.

An externally controlled fast routing system permits the acquisition of data in a time-resolved environment. The acquired data may be accumulated with a preprogrammed offset and then shifted by a fixed amount each time the externally triggered router is pulsed. A total of 256 time slices may be accumulated.

The Model 4204 may accept up to 16 different sources of STOP (or START) to make one time interval measurement. The 16 sources are OR'd together inside the module and an OR front-panel output is provided. This OR output may be used to STOP (or START) the digitizer. The pattern of the sources providing the STOP (or START) within a given time window is stored in the 4204 and is CAMAC readable. When more than one source is present within the time window, an overflow may be generated to reset the unit. Finally, the channel number of the active input may drive the router, permitting the acquisition of separate spectra for each input. This instrument is widely used in Muon Spin Rotation experiments.

The 1 MHz data throughput rate may be achieved even without a fast data acquisition system via a LeCroy Histogramming Memory Module. The LeCroy Histogramming Memory Module (Model 3588) can be connected via a front-panel auxiliary bus. The histogramming memories may then be read out at lower speeds via CAMAC or through the LeCroy Model 8901A, GPIB (IEEE 488) Interface. Data loaded into the histogramming memory units retain all the above features including programmable offset and router.

Model 4208 Wide Range, Octal Time Digitizer

The LeCroy Model 4208 Time Digitizer is designed to cover applications where time measurements must be performed in real time, and which require wide dynamic range with high resolution.

The Model 4208 has eight independent channels, each of which measures the time from the leading edge of a COMMON input to the leading edge of its INDIVIDUAL input pulse.

Due to the advanced design, common start input mode as well as common stop input mode can be used. The digitizer will encode input pulses preceding the COMMON input as negative times and input pulses arriving after the COMMON input as positive times.

The Model 4208 also may operate as a single input, 8-hit time digitizer. In this strap-selectable mode, all eight inputs are cascaded. As each input is hit, it enables the next one. The unit also may be configured as a dual input 4-hit time digitizer, a quad double-hit time digitizer, or several other combinations of multihit.

The 4208 converts the measured time intervals into a 23-bit digital word pulse a 24th sign bit. The sign bit indicates whether or not the COMMON input has preceded or followed the INDIVIDUAL input. This corresponds to a dynamic range of ±8.3 msec (which can be expanded with an external clock and appropriate logic circuits. See 4208 manual).

The module is equipped with a high stability crystal-controlled 125 MHz clock. The 1 nsec resolution is achieved by digital interpolation between two clock pulses. Deadtime after an event has occurred is negligible and data readout can occur immediately after the event. An external clock input is provided to permit synchronous operation of several modules with an external 125 MHz time base.

CAMAC COMMANDS AND FUNCTION CODES

Model 2228A, 2229 Octal Time Digitizers

CAMAC Commands:

Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2".

I: "Start" input is inhibited during CAMAC "inhibit" command.

Q: A Q = 1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression).

X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated.

L: A Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules.

CAMAC Function Codes:

F(0): Read registers; requires N and A; A(0) through A(7) are used for channel address.

F(2): Read registers and clear module; requires N, A and S2. Clears on A(7) only.

F(8): Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is generated if LAM is present and enabled.

F(9): Clear module (and LAM): requires N and any A from A(0) to A(7), and S2.

F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7).

F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(7).

F(25): Test module; requires N, S2 and any A from A(0) to A(7).

F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F(24) applied.

Caution: The state of the LAM mask will be arbitrary after power turn-on.

Q and LAM Suppression:

A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.

Model 4204 Multisource, Time Interval Meter

CAMAC Commands:

C: Clears last event (same as CLEAR Input)

Z: Initializes modules

I: Inhibits module (Inhibits START, STOP, and Multi-source ECL Input)

LAM: A Look-At-Me is generated as soon as the module has valid data to be read.

Q: A Q response is generated if the requested function can be executed.

CAMAC Function Codes:

F(0)•A(0-3): Reads time interval data, 24 bits

F(1)•A(0-3): Reads multi-source hit word; the multi-source hit word is never erased and may always be read. It is over-written by the next event.

Data format:

Bit 1 to 16: Hit pattern of multi-source input.

Bit 17 to 20: Channel number – 1 of the multi-source input used for the time interval measurement (first channel hit).

Bit 21: Set if a second pulse arrives on the same multi-source input channel that was first hit (double pulse resolution 50 nsec).

F(2)•A(0-3): Reads time interval data (24 bits) at S1, resets register and LAM at S2.

F(2)•A(8): Same as F(2)•A(0-3) plus starts test "0" at S2; a subsequent read function will read the result of the test.*

F(2)•A(9): Same as above, but for test "1".*

F(2)•A(10): Same as above, but for test "2".*

F(2)•A(11): Same as above, but for test "3".*

*NOTE: The tests defined above are mainly for calibration purposes and not for normal customer use.

F(8)•(0-3): Tests LAM, Q response if LAM on.

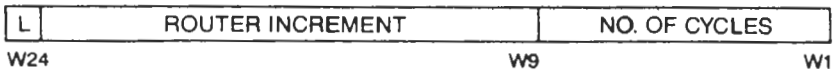
F(9)•A(0-3): Sets the router register to zero; in multi-source mode, clears the hit pattern word; clears only the last event being processed or already processed; clear time <500 nsec.

F(10)•A(0-3): Clears LAM and data register

F(16)•A(0-3): Writes offset register, 24 bits

F(17)•A(0-3): Selects multi-source mode and writes router command word

Data format:



Bit 1 to 8: Number of router cycles, = 0 for multi-source mode.

Bit 9 to 23: Number of router increment steps (step size 256 channels).

Bit 24: Multi-source mode: if = 1, generates overflow condition if number of hits at multi-source input >1.
Normal Mode: if = 1, external router will not loop.

F(18)•A(0-3): Writes command word on the following format:

Bit 1 to 4: Time Resolution Range.

Bit 5 to 24: Time Overflow Setting.

F(24)•A(0-3): Disables module (in this state, the offset plus router value can be read with F(0) or F(2)).

F(25)•A(0-3): Increments router counter by one. Must not be used in multi-source mode.

F(26)•A(0-3): Enables module

Model 4208 Wide Range, Octal Time Digitizer

CAMAC Commands:

Z,C: Initialize module; clears all channels and clears the LAM.

I: Inhibits all channel inputs during CAMAC inhibit command.

Q: Conditional response for F(0), F(2), F(8), F(10)

X: X = 1 response is generated for each valid function.

L: When enabled (jumper option), LAM is generated by the unit in response to either the "End of Time Window" input or the internal monostable pulse, whichever comes first.

CAMAC Function Codes:

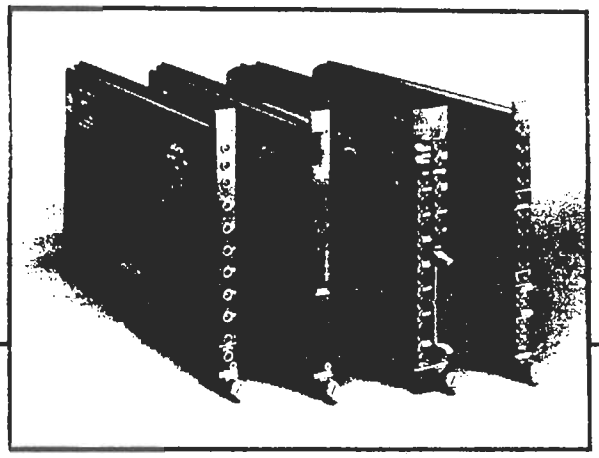
F(0)•A(0) to A(7): Addressed readout; read data on Read Lines (2's complement convention); Q = 0 if an empty channel is read; Q = 1 otherwise.

F(2)•A(0) to A(7): Addressed readout as for F(0); F(2)•A(7) clears the unit at S2; does not clear the LAM.

F(8)•A(0): Test Look-at-Me; Q = 1 if LAM is present.

F(9)•A(0): Clears unit; resets LAM and all channels.

F(10)•A(0): Test and clear Look-at-Me; Q = 1 if LAM is present.



SPECIFICATIONS

CAMAC Time Digitizers

(TIME-TO-DIGITAL CONVERTERS)

MODEL	2228A	2229	4204	4208
CHANNELS	8	8	1	8
INPUT LEVELS	NIM (logical 1 = – 0.8 V); (threshold ⩽ – 500 mV) 50 Ω input impedance	Differential ECL (– 0.8 V and – 1.6 V) (Common mode range, – 0.4 V to – 2.0 V; threshold ⩽250 mV	– 1.5 V to + 1.5 V; high impedance Multisource input is differential ECL (– 0.8 V to – 1.6 V)	– 1.5 V to + 1.5 V 50 Ω input impedance
DYNAMIC RANGE	11 bits	11 bits	24 bits	23 bits + sign
NUMBER OF RANGES	3	3	15	1
TIME RESOLUTION	50 psec 100 psec 250 psec**	50 psec (30 psec)* 100 psec 250 psec**	156.2 psec to 2.56 μsec	± 1 nsec
TIME RANGE	0-100 nsec 0-200 nsec 0-500 nsec**	0-100 nsec (0-60 nsec)* 0-200 nsec 0-500 nsec**	±167 msec	±8.3 msec
CONVERSION TIME	100 μsec (Rear-panel adjustment for fewer bits/ shorter time)	100 μsec (Rear-panel adjustment for fewer bits/ shorter time)	<1 μsec; typically 0.5 μsec for zero time measurement	none (real time technique)
TEST FEATURES	Yes	Yes	No	No
FAST CLEAR TIME	1.4 μsec	1.4 μsec	<500 nsec	50 nsec
INTEGRAL NON-LINEARITY	<±2 counts	<±2 counts	±3 counts for resolution ⩾625 psec, ⩽±5 counts otherwise	±1 count
COMMENTS	**Internally adjustable to 1 μsec full scale, 500 psec res.	*Specify Mod 400 when ordering **Internally adjustable to 1 μsec full scale, 500 psec res.	Programmable Offset Router may be driven by multisource input. Front-panel port is for Histogramming Memory (Model 3588).	May be set to multihit via jumpers. Multihit deadtime 3 nsec between stops.
POWER				
+ 6 V	600 mA	600 mA	3.1 A	1.5 A
– 6 V	550 mA	600 mA	2.7 mA	3.3 A
+24 V	25 mA	25 mA	30 mA	17 mA
–24 V	140 mA	140 mA	60 mA	17 mA
	10.9 W	11.2 W	36.9 W	29.6 W
PACKAGING	#1 CAMAC module	#1 CAMAC module	#2 CAMAC module	#1 CAMAC module

SECTION 1

SPECIFICATIONS

1.2 Introduction

The Model 2228A and 2229 TDC modules contain eight complete time-to-digital converters in a single-width CAMAC module. The time-to-digital conversion is accomplished in two steps. A capacitor is charged up by a constant current source initiated by the common start pulse and terminated by the stop pulse. The total charge delivered to the capacitor is an analog representation of the time interval to be measured. An analog-to-digital conversion is then performed by using the Wilkinson rundown method. In this technique, the charge is removed from the capacitor at a constant rate during which time pulses from an oscillator are gated into a scaler. The final count is thus proportional to the time interval measured.

1.3 Inputs

The eight Stop inputs of the 2228A require standard NIM levels supplied via coax, terminated at the individual 50 Ω Lemo-type connectors. The eight Stop inputs of the 2229 require differential ECL levels supplied via twisted-pair or flat ribbon cable that is terminated in 112 Ω at a dual eight pin connector. These cables (Model CST 34/16) may be ordered from the factory or built by the user (see Figure 1.2). Note that if the module driving the 34-pin end of this cable conforms to the ECLine standard, then a half twist in this cable will be necessary.

Pulses at these inputs define the end of the timing intervals for the eight channels. The Stop input pulses should be a minimum of 5 nsec Full Width at Half Maximum. Since an accidental Stop pulse overlapping the Start will cause the channel to ignore the real Start pulse a short Stop pulse width is recommend to minimize this possibility.

The Common Start, Common Stop and Common Clear of the 2228A each accept NIM pulses and are terminated in 50 Ω at Lemo-type connectors. In the 2229, these three common signals use three pairs of a five-pair ribbon cable that is optionally terminated in 112 Ω at a dual 8-pin connector. The SIP Termination resistor package can be removed via the side panel access (a storage location is provided for this SIP at the bottom of the module) allowing use of a multiconnector ribbon cable "daisy chaining" all Common inputs of several 2229 modules. This requires only one driver per 16 modules, but it is important that the last, and only the last connector be terminated. Total cable length should be minimized (i.e., > 2 meters) for minimum pulse distortion and module to module delay. However the user may find that a small amount of slack should be allowed in the daisy chain between each module to allow easy removal of one module from the chain. A cable (Model CST 34/10-L shown in Figure 1.3) suitable for driving the Common inputs to twenty-four 2229 modules is available from LeCroy.

A pulse applied to the Common Start input begins the timing measurement unless it is held in an inhibited condition by the CAMAC I (Inhibit) command.

A pulse applied to the Common Stop input will stop all inputs and is intended for calibration and test use (see Section 2.2).

1.4 Full Scale Count

The Full Scale Count can be adjusted by a rear panel potentiometer. The range is from 250 to 1950 counts (about 8 to 11 bits). A voltage proportional to the Full Scale is provided at a rear panel test point. To get a more accurate setting, test the TDC with a Start pulse and no Stop pulse. A graph of the Full Scale Count vs V_{BFS} (Test Point Voltage) is shown in Figure 1.1.

1.5 Conversion Gain

Three Conversion Gain ranges can be selected by a switch on the side panel. These are factory set for 50, 100 and 250 psec/count. These correspond to Full Scale Input times of 100, 200 and 500 nsec. The 250 psec/count range can be extended to 500 psec/count by the trim pot provided. (Temperature Drift is increased by up to a factor of 4 by this method. If a more stable method is desired, see Section 2.3 on Extended Time Ranges).

1.6 Offset

Although the devices are selected at the testing stage to get a close match on offsets, the TDC is not absolutely calibrated. This means the offsets will vary from channel-to-channel and board-to-board. The typical offset is 7 ±2 nsec, when measured from the Common Start to the individual stops at the front panel. Offsets measured with Individual Stops vs. Common Stop will also differ slightly.

On its most sensitive range the 2228A and 2229 will resolve 50 pS per count. The time required for an electrical signal to travel approximately 1/2 inch is 50 psec in 50 Ω cable or on a printed circuit board. Additionally, propagation times for the gating circuitry may vary by 3 nsec or more (60 counts) per device.

1.7 Conversion Time and Fast Clear

Conversion time for the 2228A and 2229 is approximately .05 µsec X Full Scale Count + 1 µsec. Maximum conversion time is, therefore, approximately 100 µsec. For an 8-bit conversion this time is reduced to about 14 µsec.

1.8 Clear

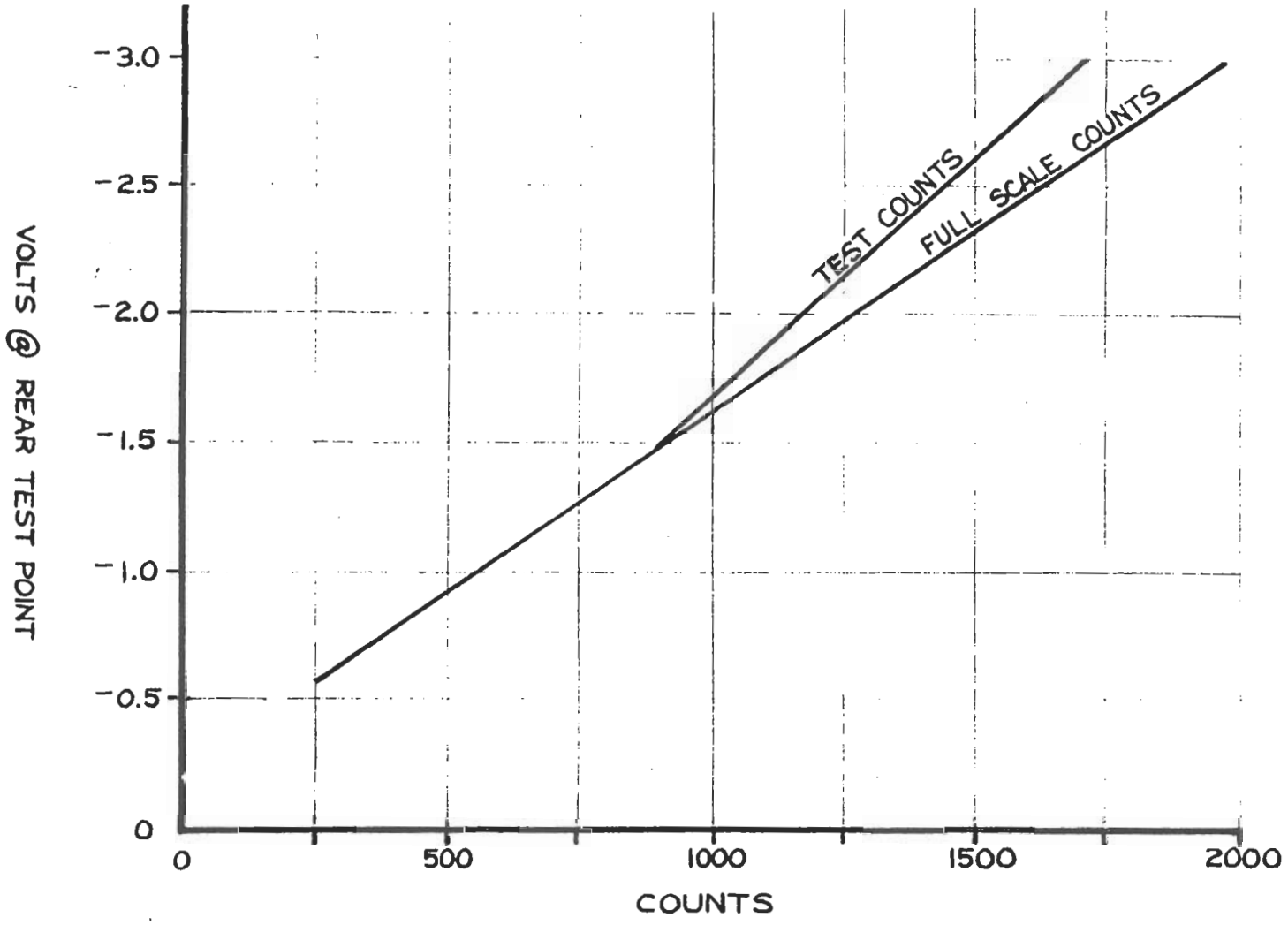
A Clear command, either CAMAC **F(9)** or front panel (50 nsec minimum), can be used to clear the 2228A or 2229 at any time. A waiting time of approximately 2 µsec is required to settle within 1 count of the

proper value.

The fast clear signal forces all 8 channels of the unit to cease their conversions and be cleared and ready to accept another start pulse after the wait time. The fast clear feature allows TDC conversion to be initiated by a fast trigger and completed only if the event satisfies a complete trigger requirement.

1.9 Packaging and Power Requirements

The 2228A and 2229 are packaged in standard #1 width CAMAC modules (conforming to ESONE Committee Report EUR4100). Each dissipates a total of 8.3 watts of power.



FULL SCALE vs. TEST POINT VOLTAGE

TEST VALUE (F25) vs. TEST POINT VOLTAGE

Figure 1.1

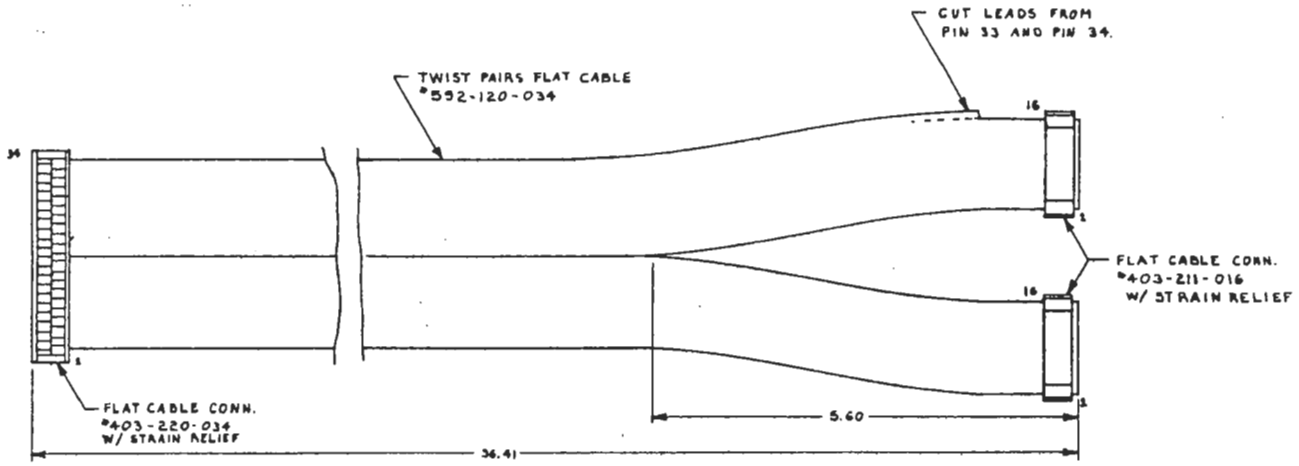
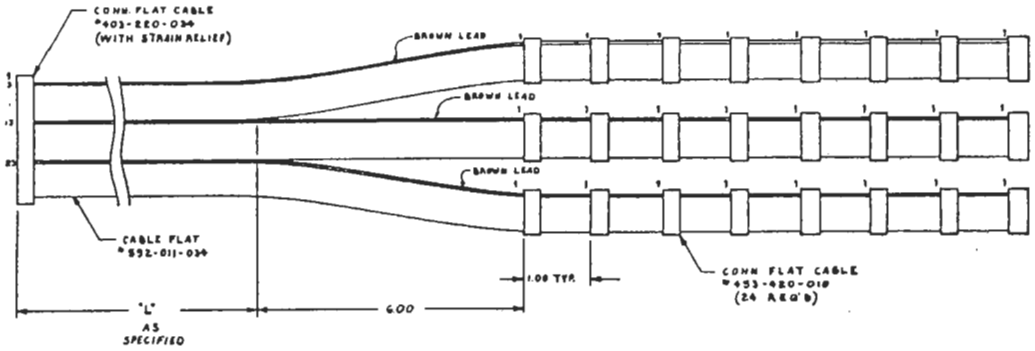


Figure 1.2



NOTES:
1) ON 10 PIN CONNS., BROWN LEADS GO TO PINS.
2) ON 34 PIN CONN. BROWN LEADS GO TO PIN 3, PIN 15 AND PIN 23.
PINS 1, 2, 33, 34 NOT USED.
3) NO STRAIN RELIEFS TO BE USED WITH 10 PIN CONNECTORS.

Figure 1.3

SECTION 2

A USER GUIDE TO OPERATION OF THE 2228A AND 2229

2.1 Data Readout Techniques

The data output is standard CAMAC-compatible (TTL negative logic) in 11-Bit binary format plus overflow. The digitized information is gated onto the R1 to R11 (2^0 to 2^{10}) and the overflow flag onto R12 of the Dataway bus by **F(0)·N·A**, where **F(0)** signifies the read function, N signifies the module to be read and A (from **A(0)** to **A(7)**) signifies which TDC channel in the module is to be read out. Generally, the unit is ready for readout when the LAM appears. The function **F(2)**, Read and Clear, may also be used to read information from selected TDC channels. This readout is destructive only when **A(7)** is addressed.

The **F(2)·N·A(7)** clears all channels at one time. The **F(2)** command on addresses **A(0)** through **A(6)** will cause the TDC contents to be read with no clear and the input gate will remain disabled.

There are three basic types of readout schemes that can be used: read all channels, read all channels in only those modules having a LAM and read only those channels that have a LAM.

The first method, read all channels, allows for use of direct memory access which is simple to use and allows for read cycle times at maximum CAMAC or CPU rates. It requires a large memory and also requires sorting the data later to throw out the channels that overflowed.

The second method allows skipping of empty modules by using the Q and LAM suppression if all channels in the module overflowed (i.e., no valid data). This method does not allow the use of DMA since some logical decisions must be made based on LAM. However, for low "hit" rates, the readout may be faster and the amount of data to sort later is reduced.

The third method allows reading only those individual channels with valid data. This is accomplished by having the LAM reflect the status of the channels selected by the subaddress lines ("A" lines). Typically the read-out proceeds as follows: The A lines are set to the selected subaddress (for example read A(X) in an empty slot). The LAM status word is then read and checked to see if any modules have data. If data is available, a read cycle is started for the same A and the appropriate N's. When this is complete the computer advances to the next subaddress. This also requires logical decisions on LAM so DMA cannot be used but only valid data is put into memory. No further data compacting is needed.

The graph in Figure 2.1 shows example readout times per crate for the various readout schemes. It is based on 16 TDC's per crate, 3 μsec per DMA cycle and a software controlled read cycle of 20 μsec. Since the Read and DMA cycle times may be much different from those used in this example, it is recommended that the user investigate the available readout techniques to find the one best suited to his application.

2.2 Test Function

The Model 2228A/2229 offers two choices of on-line testing. The first method involves the use of the Common Stop input. A pulse applied to this input will simultaneously stop all channels. It is important to note that this Common Stop pulse will terminate the timing interval 4.5 ±0.5 nsec later than if the same pulse were applied to the separate Stop inputs.

During the precision on-line testing using this Common Stop input, it is still possible for the individual Stop inputs to independently stop their respective channels earlier. It is, therefore, recommended that the normal Stop pulse sources be vetoed (inhibited) during the testing time.

A second method of performing on-line testing is via the CAMAC function **F(25)**. Upon application of **F(25)·N·A** (any A from A0 to A7) at S2 time, an internal Start and Stop is generated, defining a time increment of approximately 75% of full scale for all 8 channels. Once again, a Stop input at any of the 8 channels will also terminate the time interval for that channel. For this reason, the sources of the stop pulses (logic units or discriminators) should be inhibited during testing, or multiple tests should be made to assure that no spurious pulses stopped any channel short of the full testing interval.

2.3 Using the TDC at <500 nsec Full Scale Settings

The Model TDC begins charging its integrating capacitor upon receipt of the Common Start pulse. A constant current source rundown also begins immediately. On the standard unit, an automatic stop is generated at about 1.2 times the full scale time range setting after the Common Start pulse (for channels which received no Stop input) and the oscillator is automatically started. Since the rundown began when the Start pulse was received, a number of 50 nsec-spaced clock pulses (20 MHz clock) will not be counted. This introduces a small constant time offset into the result (See Figure 2.2) which can be calibrated out by using different cable lengths for Start and Stop inputs (this also should be done to compensate for the minimum internal offset of approximately 7.0 nsec).

For users desiring a 500 psec/count range (achieved simply by readjusting the 250 psec/count range potentiometer) such as might be needed for drift chamber applications, this effect would total 24 counts or approximately 2.4%. Compensation for this would necessitate an additional 12 nsec of delay cable. To eliminate this

necessity, it is possible, by moving one jumper, *for the TDC to trigger the oscillator with the leading edge of the start input. Turning on the oscillator within the timing interval causes some oscillatory noise which affects the integrating capacitor. Although this noise would affect the linearity of measurements using a 100 nsec full scale range, it is integrated out in the 1 µsec range and in the end contributes quite negligibly to integral non-linearities. Using this jumper option will also adversely affect the differential linearity of the TDC. For example the user may see more even than odd numbered TDC readings because even numbered "bin" widths may become slightly larger than odd bins. The integral linearity remains good because the average bin width is unaffected.

The effect described above is especially noticeable in units modified for extended time ranges as described in the next section.

2.3.1 Optional: Extended Time Ranges

The Model 2228A and 2229 are available at extra cost with a factory installed option providing .5, 1 and 2.5 nsec/count time ranges (order Mod 200 version).

2.4 Start-Stop Input Time Jitter and Drift

Each Start and Stop input has a "threshold" level which is affected by several factors (e.g., the base-emitter drop of an input emitter follower in the 2228A, etc.). If these factors were to change with temperature, voltage, or time variations this would cause triggering at a different amplitude level. Since the rise time of the input pulses is not equal to zero the result is a small time jitter and/or drift. The effect is worse for input pulses of longer risetimes. However, in the 2228A and 2229, the circuitry accepting the stop pulses and start pulses is identical (i.e., in the example above, although the base emitter drop does change by some small amount (=2 mV/°C), it changes nearly equally for both start and stop inputs). Therefore, if care is taken to use identical pulses (i.e., same risetime) for the start and stop inputs, the relative time difference between them will remain nearly constant, regardless of how far the "threshold" drifted. It is worthwhile to note that reasonable voltage variations and aging do not cause "threshold" drift of the inputs. The triggering level for both Start and Stop inputs is between -350 mV and -450 mV for the 2228A and at 0 V differentially (-1.2 V nominal for symmetrical pulses) for the 2229.

*Move jumper from G4-G4 to G3-G3. See Schematic Sheet 2 of 5.

2.5 Overflow Detection

The 2228A and 2229 have a continuously adjustable Full Scale (from approximately 8 to 11 Bits). This requires detection of Full Scale by some means other than using the next most significant bit as an indicator unless the Full Scale is set to approximately 5% beyond the desired count (e.g., 1024 + 5% = 1075). In addition, the state of the Analog-to-Time Converter is detected when the clock stops. This information is stored and presented on the R12 line independent of the Full Scale setting. This information is also used to determine LAM and Q response.

2.6 LAM and Q Response

The 2228A/2229 was designed to permit the elimination of readout of empty modules to achieve fast readout rate. A module in which no channel has received a stop pulse (i.e., all scalers overflowed) will produce no Q-response or LAM and appears as an empty CAMAC slot during readout, reducing readout time. An X-response is still generated.

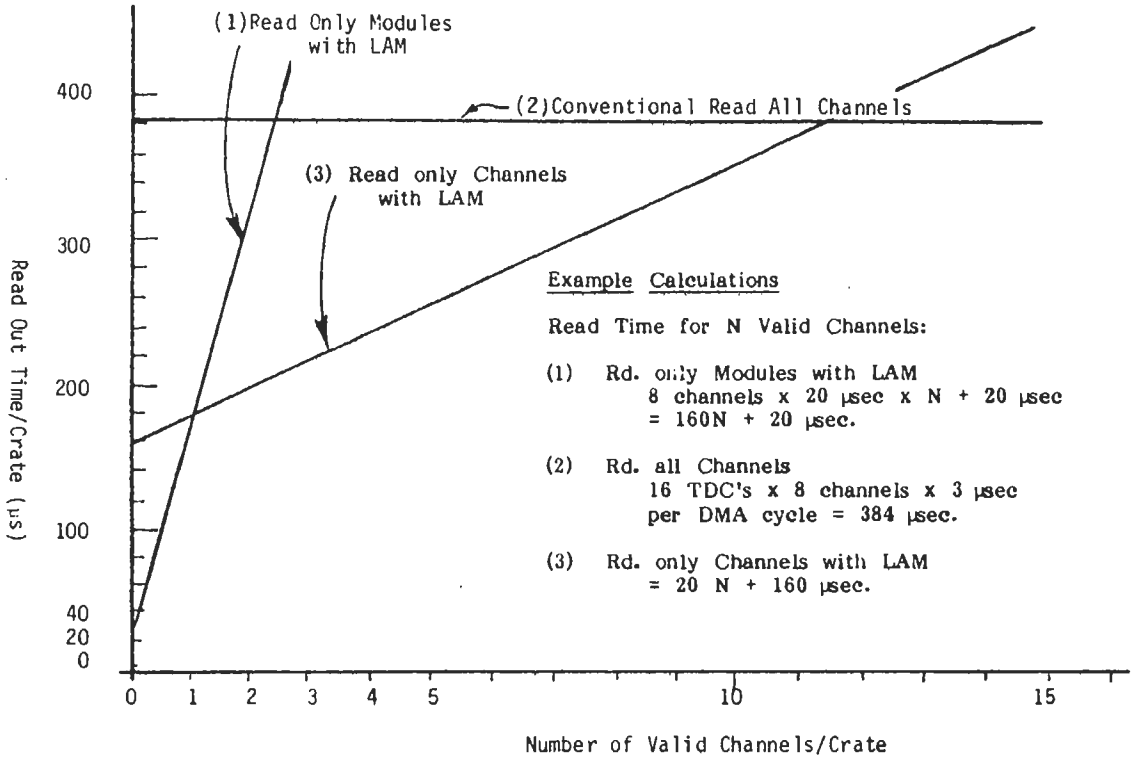
Some branch drivers (interfaces between computers and CAMAC crates) or readout schemes require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations the Q Select Side Panel Switch should be turned to the "End of Conversion" position.

A LAM (Look-At-Me) signal is generated from end of conversion until a Module Clear or Clear LAM (**Z, C, F(2)·A(7), F(9)** or **F(10)**). LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable **F(26)** or Disable **F(24)** function command, and can be tested by Test LAM **F(8)**. LAM is suppressed for empty modules as indicated above.

The test function **F(8)** allows the LAM to be tested. In response to application of **F(8)·N·A** (where A is any A from A(0) to A(7)) independent of Disable LAM, a Q response will be generated if LAM is set and not masked. Although the LAM is disabled while the 2228A in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an **F(8)·N·A** is applied. An **F(10)** will clear the LAM independent of the state of the LAM mask but this will also end Q response and disable readout until after the next conversion. A safer way to eliminate the L signal is to use **F(24)** (Disable Look-At-Me) to mask the L signal. This will allow normal readout to continue.

Also see the section on 2228A Read Schemes.

IMPORTANT: The unit should always be initialized with an **F(24)** (Disable LAM) or an **F(26)** (Enable LAM) and an F(10) (Clear LAM) whenever the crate power is turned on.



READ OUT TIME vs. VALID CHANNELS/CRATE

Figure 2.1

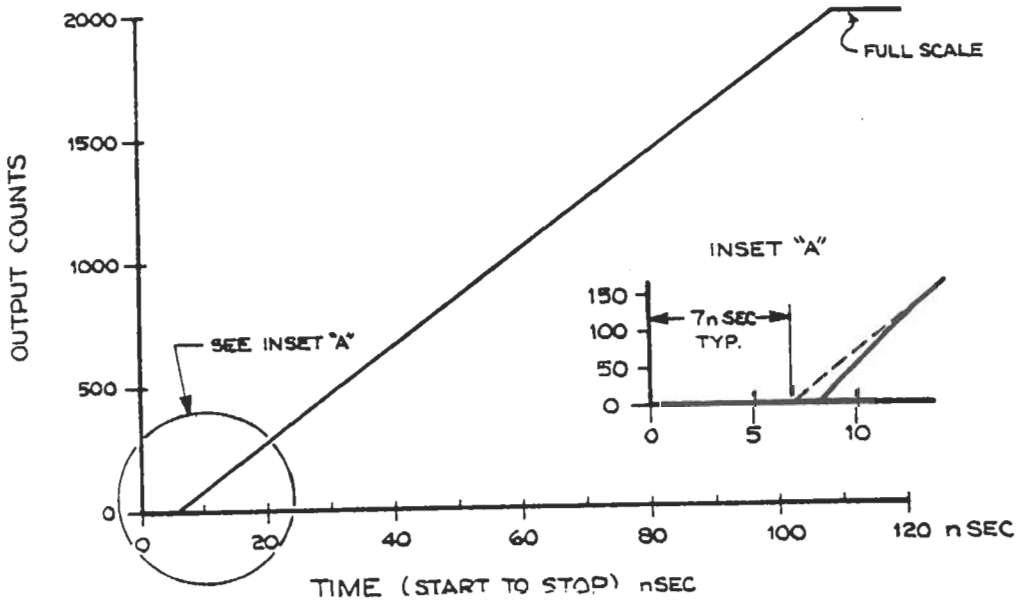

2000
1500
1000
500
0
OUTPUT COUNTS
FULL SCALE
SEE INSET "A"
INSET "A"
150
100
50
0
7n SEC
TYP.
0
5
10
0
20
40
60
80
100
120 n SEC
TIME (START TO STOP) nSEC

Figure 2.2

SECTION 3

FUNCTIONAL DESCRIPTION

3.1 General

The Model 2228A and 2229 consist of 8 independent identical TDC's and associated circuitry. Referring to the block diagram (Figure 3.1), the TDC circuitry is divided into seven basic sections:

a. A Common Start, Delayed Start and Common Stop circuit for distributing the start signal to the start-stop gates.

b. Eight Stop Input circuits.

c. Eight Time-To-Analog converters.

d. Eight Analog-To-Time converters.

e. Eight scalers.

f. A Gated oscillator

g. A CAMAC control section.

3.2 Start, Delayed Start and Common Stop

The Model 2228A requires NIM-level inputs for the Start and Stop, but uses ECL integrated circuits for gating and latching (see Figure 3.2). This requires a -800 mV shift in logic levels which is provided by using NPN emitter followers on all inputs. Timing stability is accomplished by providing both the start channel and the stop channels with approximately the same number and type of components assembled so that delay changes (caused by temperature and voltage changes) will cancel each other.

A pulse applied to the Common Start input, after receiving a voltage offset and level inversion, will set a latch (Schematic 2/5) formed from two ECL negative NAND gates. The latch output couples to two 3 input gates each driving the center point of 100 Ω strip line busses via 50 Ω coax. Each of the two busses provides four Stop channels with a Start Enable signal which is available until a Common Stop is received, until the delayed Start occurs, or until a clear pulse is received (see next three paragraphs for explanation of three Start-Disable functions).

Once the Start latch is set, it will remain set until a clear pulse resets the entire module. If the common Stop latch is set, or when the delayed Start occurs (either one disabling the Start latch output), they will remain in that condition until the Start latch is cleared. Thus, once one Start pulse is received, the entire section is made immune to any further Start pulses until the entire module is properly cleared. A CAMAC Inhibit will disable the Start input emitter follower for the duration of the Inhibit.

The Common Stop Latch, when set, will disable the two 3-input gates, ending the Start Enable signal. The Common Stop input passes through the same level shifting and inverting stages and uses the same type latch as the Start channel. The only differences are that the latch complement level is used to disable the 3 input coax drive gate and the latch is only enabled when the Start latch is set and is, therefore, cleared when the Start latch is cleared.

The delayed Start is a level which occurs approximately 1.2 times the full scale time range setting. It results from a level-sensing amplifier monitoring a capacitor which is being charged via a constant current source, which was unclamped when the Start latch set. Because the current source is controlled by the I-select line, it is always proportional to the current sources in the time-to-analog circuits (see next section).

A common module clear pulse, 1.0 to 1.2 μsec long, is used to clear the Start latch and keep it clamped (therefore disabled) for the duration of the clear.

The internal test capability is provided by generating a Common Start and a Common Stop upon receiving an **F(25)**. These two pulses are generated by two voltage comparators that monitor a ramp generated by I_{SEL}. The delay is thus proportional to the psec/Count Range. The other side of the start comparator is tied to ground and the other side of the Stop comparator is tied to V_{BFS} which tracks the full scale range. The count obtained is thus about 75% of the full scale range for most psec/Count and full scale range settings.

3.3 Stop Input Circuits

The individual Stop circuits operate identically to the Common Stop (see previous section). When a Start enable signal occurs, it enables the linear gate of the Time-To-Analog Converter (TAC) stage via an ECL differential output gate. It also enables the Stop latch to be set which, until the Start enable signal appeared, was held clamped in a reset condition, preventing it from being set by a possible premature pulse at the Stop input.

Once the Stop latch is enabled, it will be set by the next Stop input pulse. (The input pulse uses the same level shifting, inverting, and latching techniques as the Start and Common Stop inputs.) When the Stop latch is set, it disables the ECL gate, thereby disabling the linear gate in the TAC.

3.4 Time-To-Analog Converters

Each Time-To-Analog Converter (TAC) utilizes a constant current generator where the actual value of current is determined by the difference between the voltage on the I-Select bus and the -24 V bus. This current is gated into an integrating capacitor for the duration of time between common Start and a Stop, therefore, the voltage on the capacitor is proportional to that time. This capacitor is then

discharged by the Analog-To-Time Converter Stage.

As can be seen from sheet 3 of the schematic, the I-Select bus voltage is varied grossly to select ranges by switch selection of voltage levels of a compensated, tracking divider chain. Each range position has a fine control potentiometer which has been factory adjusted to provide the ranges shown on the side panel (and on the schematic). The 250 psec/Count range can be set as high as 500 psec/Count and used reliably.

Temperature drift is increased by up to a factor of 4 by this method. If a more stable method is desired, see Section 2.3 (converting the TDC to longer time ranges).

3.5 Analog-To-Time Converter

The Analog-To-Time Converter (ATC) stage is functionally the inverse of the previous TAC stage, except that the capacitor discharge rate is much slower than the charge rate.

The charge which was delivered to the integrating capacitor through the linear gate of the TAC stage is subsequently removed by means of a stable current source (see Figure 3.2). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. (This rate is proportional to the difference between the +24 and V_{REF} inputs.) The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is more negative than a reference level (which is set by the voltage divider between +3 V and ground). The output time duration (T_2) is, therefore, proportional to the input time (T_1) of the TAC where time T_2 is approximately 1,000 times T_1 when used in the most sensitive 50 psec/Count range (i.e., $T_2 = 1000\ T_1$).

Stable operation of the QTC is assured by the on-board stabilized V_{REF} (approximately +12 V current source reference) to be independent of external supply variations. Whenever necessary elsewhere in the analog circuits, tracking dividers and temperature-compensating diodes or transistors are used to remove first order drift errors.

3.6 Scaler

The output of each Analog-To-Time Converter in the TDC is used to gate a clock into one half of a LeCroy hybrid SC100 Dual Eleven-Bit Scaler. The oscillator is synchronously started with respect to the leading edge of the Start input pulse (see Section 3.7). This insures no fractional pulses during the beginning of the run-down cycle.

When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). The 11-Bit data word will be gated out in parallel to the CAMAC dataway when an N, either an **F(0)** or an **F(2)** command and the appropriate A are received.

3.7 Gated Oscillator

The clock circuit is a modified Colpitts oscillator employing a highly temperature-stable clock and a mica capacitor as its resonant elements. Its frequency is 20 MHz. The oscillator is gated on at approximately 1.2 times the full scale range setting after the leading edge of the Start pulse. (In the optional long time range units it is gated on with the leading edge of the Start, as the clock noise becomes insignificant.) Synchronously, gating the oscillator on in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates clock noise caused by not delaying the turn-on. The conversion time is approximately 1 μsec + (.05 μsec times the full scale count setting).

3.8 Full Scale Adjustment

The Model 2228A and 2229 allow for an adjustable full scale from about 8 bits to 11 bits of data. The adjustment is made via a rear panel pot. There is a test point provided at the rear panel to allow monitoring the full scale setting (see the conversion chart Figure 1.1). This feature reduces the conversion time in proportion to the full scale range.

3.9 Overflow Detection

Because the full scale is adjustable it is necessary to detect overflow (no stop within time range) by some means other than using the next bit as an overflow condition. (This method can still be used if desired on all but the 11 bit range by setting the full scale pot to about 5% beyond the desired count.) The method used in the 2228A and 2229 is to sample the state of the clock gate for each channel following the last clock pulse. If there was a valid stop, the gate should be closed. The information acquired is stored in latches and used to determine the Q and Look-At-Me status.

3.10 LAM and Q Response Circuits

As stated previously, the overflow information is used in the Q and LAM decisions. There are three switch selectable options for Q status:

a. All channels have Q=1 if conversion is complete.

b. All channels have Q=1 if conversion is complete and at least one channel has valid date (i.e., did not overflow).

c. Each channel has a Q=1 if at the end of conversion it had not overflowed.

The LAM status has 4 switch selectable options. These are:

a. LAM status = 1 if conversion is complete.

b. LAM status = 1 if conversion is complete and at least one channel has valid data (i.e., did not overflow).

c. LAM status = 1 if conversion is complete and the channel addressed by the "A" lines has not overflowed. (This is not according to CAMAC convention. (See description of the Fast Read Mode in Section 2.1.)

d. LAM = 0 always. This allows the user to turn off the LAM in cases where it is not desired without needing to send an **F(24)** to the unit each time it is turned on.

3.11 CAMAC Control

The decoding of CAMAC "F" lines F1, F2, F8 and F16 is done in an excess three gray code to decimal converter (7444). The useful outputs are OR'd together and then AND'd with F4 and A8 (valid channel). This signal is in turn AND'd with N to produce the "Valid Command" signal that is used as CAMAC X. This signal also provides the read gate to output data onto the dataway and a gate (along with Z and C) for S2.

The CAMAC "A" lines A2 and A4 are decoded and gated with end of conversion and an OR'd signal of **F(0)** and **F(2)** in a BCD to decimal decoder (7442). The output of this decoder provides the enable signal to the four SC100 scalers. The A1 line provides the select line to the scalers (selects which half of the SC100 is gating data out if it is enabled).

The A1, A2 and A4 lines also go to an 8 line to 1 line data selector (multiplexer) to examine the individual overflow signals. These signals are stored in the two quad latches (74175) and are OR'd together by a 7430 8 input gate. These latches are clocked by the end of conversion signal (delayed through Q-26).