technical information manual

SERIES 2249(A, SG, W)

12 CHANNEL ADC

11-79.

WARRANTY

All LRS instruments are guaranteed to operate within their specifications for one year from the date of purchase. Under this warranty, any unit which fails to perform within specifications, as a result of defects in workmanship or materials, will be restored to specified operating condition free of charge except for shipping costs involved in the return of the unit to the factory.

In order that this warranty be considered valid, it is necessary that the LRS Warranty Card which accompanies the unit on delivery be completed and returned to the factory within 30 days of receipt of equipment.

All questions concerning repairs or replacement parts should be addressed directly to factory's Quality Control Manager. This procedure will insure the fastest possible service. Please include the Model Type, Serial Number, and ECN (Engineering Change Number) with all requests for parts or service.

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

NOTE TO THE USER

LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, and in response to information received from the users of our equipment, the Engineering Department at LeCroy is continually seeking to refine and improve the performance of our products.

While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

If you have any questions about the performance or operation of this unit, rapid assistance may be obtained from our Engineering Services Department in Spring Valley, NY, telephone 914-425-2000, or from your local distributor in countries other than the U.S.A.

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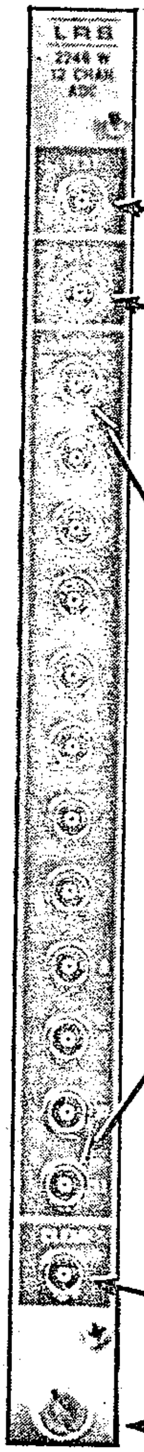
CAMAC Model 2249W

12-Channel A-to-D Converter



TEST Input: Accepts DC level; unit injects a charge of -20 pC/volt into all inputs simultaneously upon application of F(25) at S2 time.

Common GATE: 50 Ω; >-600 mV enables; recommended range of gate width, 30 nsec - 10 µsec; effective opening and closing times, approximately 5 nsec.

Analog Inputs: Charge-sensitive; AC-coupled; 50 Ω; linear range, 0 - -2.0 volts; -500 pC full scale.

Fast CLEAR: ≤ 2 µsec; requires >-600 mV, >50 nsec FWHM signal into 50 Ω.

#1 CAMAC Module, utilizing ±6, ±24 volts.

April, 1977

ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

TECHNICAL DATA

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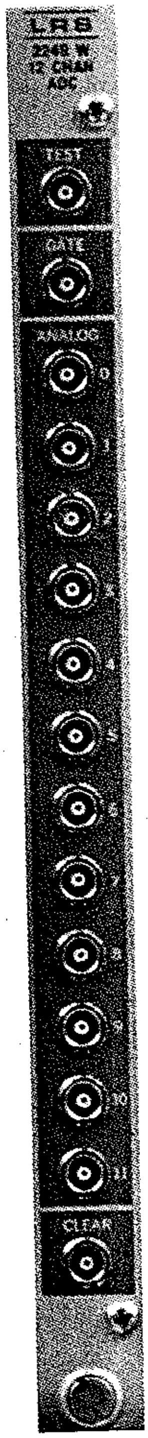

CAMAC Model 2249W

12-Channel A-to-D Converter

The LeCroy Model 2249W is a twelve-channel, eleven-bit integrating-type analog-to-digital converter. It features excellent linearity and unprecedented stability, thus allowing operation at wide gates of up to 10 μsec. Thus, the 2249W is compatible with CsI and NaI crystal detectors. Its minimum gate of 30 nsec makes its use with organic scintillators and Čerenkov detectors possible in all but the highest rate conditions.

The 2249W has been optimized for dynamic range and linearity. By AC-coupling the input, 11 bit (1980 counts) operation has been achieved with ± 1 count integral linearity. This excellent linearity is maintained from the smallest signal size to signals as large as −2 V.

The test feature allows all twelve ADC's to simultaneously digitize a charge proportional to a DC-level provided to a front-panel connector or patched into the CAMAC Dataway connector. In addition, the pedestals alone can be checked on-line by the same test feature by removing the CAMAC inhibit (I) during the test.

The Model 2249W offers an excellent event rate capability through the incorporation of a 2 μsec fast clear, which permits the ADC's to begin digitizing and then be cleared upon receipt of later trigger information rather than delaying the analog signals with long cables while the trigger decision is being made. In addition, rapid readout is made possible by a convenient Q and LAM suppress feature, side-panel adjustable between 0 and 100 counts. This feature permits an empty 2249W to be overlooked in a CAMAC readout cycle.

March, 1977

Innovators in Instrumentation

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LeCroy Research Systems Corp.
Spring Valley, New York

4. OPERATIONAL DESCRIPTION

4a. General

The LeCroy Model 2249 Series 12-Channel ADC contains 12 complete analog-to-digital converters in a single-width CAMAC module. The 2249A and SG offer 10 bits, and the W version offers 11 bits. The analog-to-digital conversion is accomplished by the Wilkinson-rundown method, which ultimately yields a digital output (in TTL negative logic binary format) which is proportional to the integral of the i·dt of the input pulse. By the Wilkinson technique, the input charge is delivered to an integrating capacitor from a linear gate, and then discharged at a constant rate. During the time this rundown is taking place, pulses from an oscillator are gated into a scaler resulting in the final count proportional to the charge originally stored in the capacitor.

4b. Analog Inputs

The 12 analog inputs of the 2249 Series are of 50 Ω impedance and accept negative-going pulses or levels only during an externally applied gating interval. To assure performance within the linear range of the 2249A and SG, input signals should not exceed -1 volt or 2 volts for the W version. The actual amount of input charge that yields a full scale digital output (1024 counts) is 256 picocoulombs (or 12.8 volt-nsec) for the 2249A and SG (512 pC, 25.6 volt-nsec, for the W version). The full scales of the 12 channels of each 2249 are set up to match within 5% of each other. Quiescent DC level of the anlog inputs of the 2249A and SG are set at approximately +4 mV to assure that it does not go negative should any drift occur. The 2249W is AC coupled and does not require this critical biasing.

4c. Gate

The built-in linear gate is common to all 12 analog inputs of the A and W, necessitating that analog-to-digital conversion for all channels is done in parallel. The 50 Ω impedance gate accepts pulses ≥-600 mV in amplitude. The duration may be between 10 nsec and 200 nsec (see next paragraph). Because of the finite risetime and falltime of the internal gate pulse, the effective gating interval is not adequately defined to allow input gate pulses shorter than 10 nsec. The actual gate opening and closing times are approximately 2 nsec, and the gate should precede the analog inputs by at least 4 nsec (A & SG versions) or 7 nsec (W version). Except when photomultiplier noise is a prime consideration, it is good practice to apply a gate pulse which is wider than the expected duration of the longest analog input. IMPORTANT NOTE! The duration of the effective gate will exceed that of the gate pulse by 4 nsec for the A and SG versions and 5 nsec for the W version.

For the 2249A and SG, gate widths exceeding 200 nsec create excessive residual pedestal (1 + 0.03t/pC, where t = gate duration in nanoseconds) and reduce the overall accuracy of the ADC by magnifying the effects of the instability manifest in the temperature coefficient, which is directly dependent upon the gate width, (i.e., maximum of ± (.03% of reading (in pC) + .002 t)pC/^{o}C). In addition, longer gates will imply an increased susceptability to any DC offset of the analog input. The actual limit of the gate duration is 2 μsec provided the resultant decrease in accuracy can be tolerated. Actually, with a gate duration of >200 nsec, it is recommended that the inputs be AC-coupled if possible.

The excellent stability and linearity of the Model 2249W allows it to be used with gate widths up to 10 μsec. In order to maintain this linearity with wide gates, however, it is necessary for the input pulse to occur within 500 nsec of the gate opening. During this 500 nsec period, a fixed amount of charge is automatically injected onto the integrarating capacitor to assure linear operation even for very small input charges which would otherwise deviate from the linearity maintained by the circuit for larger input charges. This injection lasts approximately 500 nsec, but the appearance of charge from the analog input will cause it to be extended. Without input charge appearing, the q inject will cease after 500 nsec (i.e., charge added will settle out), and subsequent input charge would be subject to a conversion graph which goes non-linear at the bottom (i.e., for small input charges).

Similarly, if it is necessary to use wide gates (>200 nsec) and the 2249W is not available, the 2249A must be used with reduced accuracy, then the analog input should occur within 500 nsec after the gate opening. During this 500 nsec period, a fixed amount of charge is automatically injected into the integrating capacitor to assure linear operation in a region representing very small input charge which would otherwise deviate from the linearity maintained by the circuit for larger input charges. This charge injection lasts only 500 nsec, but the appearance of charge from the analog input will cause it to be extended. Without input charge appearing, the q inject will cease after 500 nsec (i.e., charge added will settle out), and subsequent input charge would be subject to a conversion graph which goes nonlinear at the bottom (i.e., for small input charges).

The 2249 Series gate is inhibited from shortly (≈100 nsec) after the trailing edge of the gate until any CAMAC clear (C, Z, F(9) or F(2)·A(11)) or a front panel clear is applied. This effectively locks out spurious analog signals and noise from the ADC while the desired signal is being processed. The ADC's internal oscillator is synchronized with the leading edge of the gate pulse (although it occurs somewhat later), eliminating inaccuracies caused by the utilization of free-running oscillators in previous designs.

The 2249SG gate inputs require -1.4 V to be enabled. Deviations from this amplitude will result in pedestal variations as the charge injection is controlled by the gate pulse. The gate inputs are terminated in 50 Ω allowing one half of the 32 mA current source output of a NIM module (such as the LeCroy Model 821) to be employed. The second half of the bridged pair should not be terminated in 50 Ω.

4d. <u>Start Input</u> (2249SG Only)

Because the gate inputs of the 2249SG are considered asynchronous, a separate signal is required to start the internal oscillator. This pulse should be a NIM level applied either simultaneously with the earliest gate pulse or should follow it by ≤100 nsec. The pedestal of a given channel will decrease by 1 count per 50 nsec start delay,with respect to the Gate time.

4e. <u>Fast Clear</u>

A front panel fast clear input accepting fast NIM-level signals (≥600 mV into 50 Ω of minimum duration, ≥50 nsec) forces all 12 channels to cease their conversions, be cleared and ready to accept another gate pulse after 1.2 to 1.5 μsec. In worst-case conditions, the 2249A and SG will clear to within 1 count after 1.2 μsec. An internal monostable makes the 1.2 μsec period mandatory, although this can be changed by special request at a sacrifice in the extent of the clearing. The fast clear feature allows ADC conversion to begin by a fast trigger and completed only if the event satisfies a complete trigger requirement.

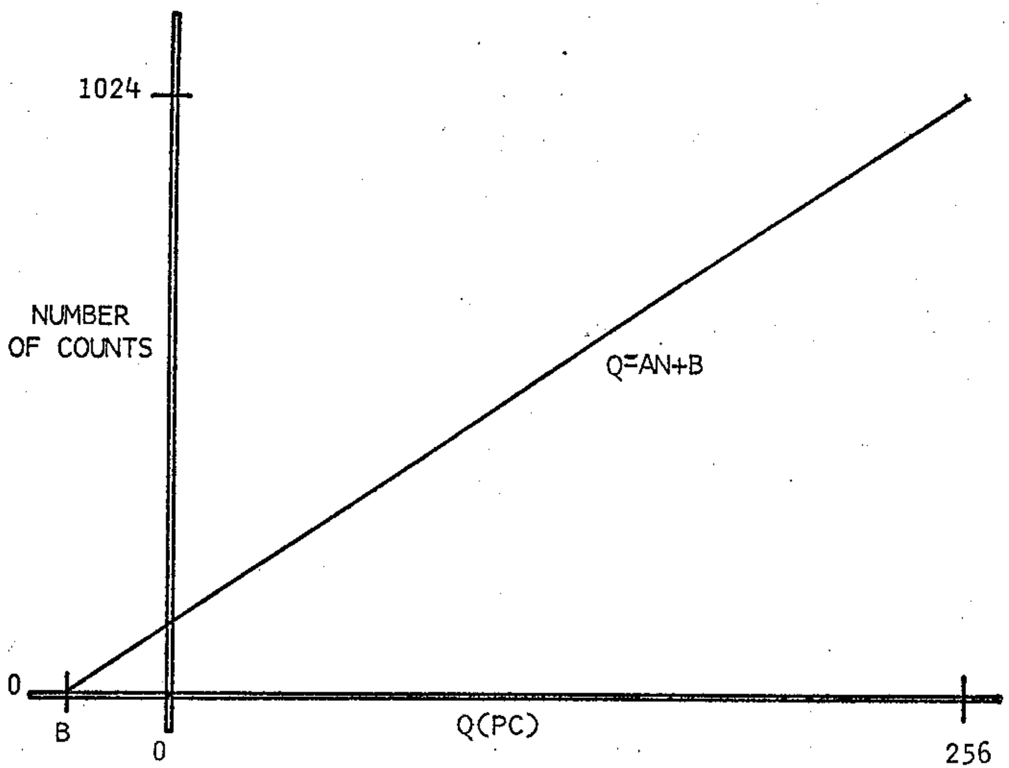
4f. Test Feature

A built-in test feature checks all channels simultaneously with an F(25) command. If the CAMAC Inhibit (I) is present and a positive DC level is applied either to a front panel "Test" input (with internal high Z (≥10KΩ) connection to a +12 volts) or optionally to rear connector patch points P1, P2, or P5, then F(25)·S2 will inject charge with a proportionality constant of -12.5 pC/volt into all inputs (23.5 pC for the W version). The internal gate generated by F(25)·S2 is approximately 80 nsec. If the user desires a measure of residual pedestal only, the CAMAC "I" should be removed; F(25)·S2 will then generate the 80 nsec gate only with no charge being injected into the analog inputs. This test feature permits the pedestal itself to be periodically checked for drifts. If two measurements are made, one with charge input and one without (i.e., with and without "I"), the total conversion characteristics could be checked. In this case, the "no charge" result gives the intercept and the "with charge" counts minus the "without charge" counts divided by the charge applied, gives the slope of the conversion plot. (See Graph on next page.)

The test feature may be connected to the rear of the 2249 as mentioned previously. The rear of the 2249 printed circuit board contains 3 drilled holes labeled P1, P2 and P5. Soldering a feedthrough through any one of these holes electrically connects the front panel "Test" input to the CAMAC connector pins P1, P2, or P5. In this way, many units can be grouped for simultaneous calibration.

It should be noted that the standard 2249SG does not respond to F(25) and has not "Test" feature. It is possible, however, to do on-line testing of the 2249SG if necessary. The price of this feature is the elimination of the inhibit feature. With the standard 2249A, the CAMAC "Inhibit" enabled the test circuit while disabling the gate circuit. Since the 2249SG has no internally generated "Test" function, the "Start" circuit must be used. To permanently enable this "Start" circuit to permit a test function to be performed, Q7, or the inhibit transistor, must be removed.

With Q7 removed, the leading edge of a pulse applied to the "Start" input will cause a fixed charge to be injected into the 2249SG analog inputs. Coincident with the "Start", the 12 gate pulses must be applied, which should have a duration between 80 nsec and 100 nsec. An exact 80 nsec gate will yield a proportionality constant of -12.5 pC/volt of DC signal



B IS AMOUNT OF PEDESTAL

Q IS CHARGE APPLIED TO ADC ANALOG INPUTS

N IS TOTAL NUMBER OF COUNTS

A IS CONVERSION SLOPE
I.E. A=(Q+B)/N

applied to whichever rear patch point (P1, P2, or P5) you choose to use for the test input. For shorter gate widths, a smaller net amount of charge is injected into each input, i.e., on the order of 90% ±1% for a 40 nsec gate.

If a test function is to be used, care must be taken to be sure the "gates" precede the "Start" by 10 nsec.

CAUTION: Since the "test" is not a designated feature of the 2249SG, its utilization is not factory tested.

4g. Linearity

The integral linearity of the 2249 Series is typically < ±2 counts (see specifications). This is defined by LeCroy as the maximum deviation from the best straight line fit to measured points. Every ADC is computer tested before being shipped to make certain it meets linearity and functional operation specifications. Each channel is tested for linearity at 50 points across its range by a 16 bit digital to charge converter.

4h. Pedestal

The residual pedestal is the number of counts obtained when a gate pulse is applied with a no analog input (i.e., input merely terminated in 50 Ω). Pedestal is a result of several factors, the largest of which is the charge injection (also contributing to the A and SG versions is a factory-set positive DC offset) the purpose of which is to assure proper operation of the front end in case the quiescent DC level of the input should drift. It is this DC offset contribution which largely comprises the gate-dependent portion of the residual pedestal specification. The fixed amount of pedestal indicated on the spec results largely from the q injection.

Due to DC coupling of the A and SG inputs, the gate-dependent portion of the pedestal has a temperature coefficient associated with it. This effect is magnified by a factor of 2 if the input is DC shorted to ground as it would be when driven from a pulse transformer, for example, used to cater photomultiplier dynode signals to the negative input requirements of the 2249A. For short gate widths, the resultatn potential temperature drift is small. However, it is nevertheless recommended that AC-coupling be used wherever rate conditions can permit it. This will nearly eliminate all but the fixed pedestal and its associated temperature coefficient.

The pedestal of the 2249A is factory adjusted to 8 counts for a gate duration of 50 nsec and to 50 counts for the SG version. The adjustment is made with a 50 Ω termination of each analog input. The pedestal of each channel of the 2249A is separately screwdriver adjustable through the side panel. Each adjustment screw is accessed through a hole adjacent to the input for the channel. (NOTE: When making adjustments, use a non-conducting screwdriver.)

The pedestal of the 2249W is factory adjusted to 16 counts for a gate duration of 400 nsec. The adjustment is made with a 50 Ω termination of each analog input. The pedestal of each channel of the Model 2249W is also screwdriver adjustable through the side panel. Each adjustment screw is accessed through a hole in the input for the channel.

NOTE: When making adjustments, use a non-conducting screwdriver.

The pedestal dependence on gate width (t) is approximated as follows for the Model 2249W:

$$\text{PED Counts} = A_0(1-e^{-A_1 t/to}) + A_2 t + A_3$$

The first term is the exponential decay of the charge injected by the leading edge of the gate to bring the QTC into linear operation. A_0 and A_1 are proportional to the capacitance selected on the pedestal adjust trim cap in each channel. This trim accounts for only a few counts at 250 nsec and is less than one count from A_0 by 500 nsec. The effect of this trim can be reduced by reducing the setting of the pedestal adjust.

The second term, A_2t, shows the linear relationship of pedestal to gate width above gate widths of 250 nsec. The factor A_2 is approximately 25 counts per microsecond. This small number reduces the need for stable gate widths.

The last term, A_3, is negative and represents the amount of charge that needs to be injected to put the QTC into linear operation and to compensate for gate width stretching (5 nsec) and the charge drained off before the clock starts. All of these terms vary slightly with different channels.

4i. Conversion Time

Since the full scales of the 12 channels of each 2249 may differ from each other by up to ±5%, the time for each channel to achieve a full scale conversion may also differ from that of the other channels. Total conversion time is roughly 50 μsec for the A and SG versions and 100 μsec for the W version. Manufacturing variances in clock frequency, ramp currents, and the necessity to allow for overflow as well as a wait interval incorporated in the design, require that a 20% margin in conversion time be allowed for. As a result, the 2249A clock is internally held on for a maximum time of 60 μsec, the SG for 55 μsec, and the W for 100 μsec (for any size conversion). Due to the fast clear feature of the 2249, however, this conversion time need be awaited only for valid events.

A factory option for the 2249A allows 8-bit operation with 66 pC full scale (0.25 pC/count) and a conversion time of 16.5 ±5% μsec.

IMPORTANT: Care should be taken to ensure that all gates come within 2 μsec of the "Start" pulse. If this will not be true, the duration of active clock may be increased by changing the 20K Ω resistor on IC "TD" (9602) to a larger value. Then the maximum allowable time between any two gates should be the new value of the monostable delay minus approximately 53.5 μsec.

4j. Q and LAM Suppression

The 2249 Series was designed to permit one to eliminate the readout of empty modules if maximum readout rate is desired. An adjustable potentiometer (accessed from side of module) permits the user to define an "empty" module by setting a count level from 0 to 100 that must be accessed before data is considered useful. A module in which all channels contain less than the set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated.

Some branch drivers (interfaces between computer and CAMAC crate) require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations, the L suppress feature may be defeated by removing the jumper XZ and replacing it with jumper YZ. (See Schematic sheet 3 or the circuit board section on next page.) In this situation a LAM condition is obtained after any Read command. The Q-response suppress can be defeated by removing jumper VW and replacing it with jumper UW. To defeat both Q and L Suppress, it is only necessary to set the count level to 0. (NOTE: 2249's and older 2249A's do not have all the jumper options available on the P.C. board. These units will require the bus be cut and a jumper added on the solder side of the board.)

4k. Data and Readout

The output data of the 2249 Series is standard CAMAC compatible (TTL negative logic) in binary format, plus overflow. The digitized information plus overflow bit are gated onto the Dataway bus lines by F(0)•N•A, where F(0) signifies the read function, N signifies the 2249 to be read, and A (from A(0) to A(11)) signifies which ADC channel in the 2249 is to be read out. Generally the unit is ready for readout when LAM appears. The function F(2) (Read and Clear) may also be used to read information from chosen ADC channels. However, this readout is destructive only when A(11) is addressed, the F(2)•N•A(11) clearing all channels at one time. The F2 command on addresses A(0) through A(10) will cause the ADC contents to be read with no clear and the input gate will remain disabled.

4l. LAM

A LAM (Look-At-Me) signal is generated from end of conversion until a module Clear or Clear LAM (Z, C, F(2), F(9) or F(10)). LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable F(26) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM may be suppressed for empty modules as indicated in "Q and LAM Suppression" section above.

The test function F(8) allows the LAM to be tested. In response to application of F(8)•N•A (where A is any A from A(0) to A(11)) independent of Disable LAM, a Q response will be generated if LAM is set. Although the LAM is disabled while the 2249 in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an F(8)•N•A is applied.

IMPORTANT! When current is applied to the 2249 (such as would occur when plugging a module in and turning the crate power supplies on), the states of the LAM latch and LAM enable are arbitrary. The unit must always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM), and an F(10) (Clear LAM).

4m. Packaging and Current Requirements

The 2249 is packaged in a standard #1 width CAMAC module (conforming to ESONE Committee Report EUR4100). The A and SG versions dissipate a total of 7.5 watts and the W, 10.6 watts.

CAUTION! Because of the adjacency of the various voltage bus connector contacts, plugging in any CAMAC unit may cause mementary misalignment of the unit and short the power pins to each other. This can cause severe damage to the module inserted, especially since the 24 volt pins are adjacent to the 6 volt pins. THUS, THE CRATE POWER SHOULD BE OFF WHEN A MODULE IS INSERTED OR REMOVED.

4n. Inhibit Circuit

The standard 2249A and W have an automatic inhibit that prevents subsequent gate pulses from allowing more charge to enter the QTC after a first gate pulse is applied. This "self inhibiting" feature is not offered on the 2249SG. Therefore, extreme caution must be taken to permit only one gate pulse per channel per event.

The Inhibit line of the 2249SG only affects the "Start" input, not the individual gates. Thus, gate pulses received during an inhibit period will cause charging of the integrating capacitor of the QT100C but no counts will be observed at the digital output.

Caution! Be sure that your gate pulse source is externally inhibited whenever a CAMAC inhibit is applied. This function is easily performed if LeCroy Model 821 Quad Discriminator with Veto is chosen to drive the ADC gates.

5. FUNCTIONAL DESCRIPTION

5a. General

The Model 2249 consists of 12 independent identical ADC's and associated circuitry. Referring to the 2249 Block Diagram following, the 2249 circuitry is divided into 6 basic parts:

- Twelve QTC (charge-to-time converter) channels
- A gate, test, and pedestal circuit for distributing the gate signal to the eight separate linear gates of the QTC's
- Twelve clock synchronizers and scalers
- A controller oscillator
- A Q response and L suppress circuit
- A CAMAC control section

Separate descriptions of each of these circuit blocks follow.

5b. Charge-To-Time Converter

Each of the 12 inputs employs a hybrid charge-to-time converter (QTC). Specifications, block diagrams and waveforms for the QT100C are enclosed with this manual after the Functional Description section. The QTC consists of a virtual ground input amplifier, a linear gate driving a stable integrating capacitor, a current source, and an output differential amplifier.

The analog input of the 2249A and SG is a virtual ground with approximately 5 to 6 Ω impedance. It can be driven either from the front panel analog input via a 44 Ω resistor or from the common test input bus (which supplies each channel with an amount of charge proportional to the test input level supplied at the front panel or rear patch pin. (Without any TEST input, a high impedance connection to +12 volts generates an approximate 60% of full scale reading.)

*The QT100C and QT100B are identical and interchangeable. The letter change indicates only a change in method of manufacturing. These are used in the 2249A and SG. The QT102 is used in the 2249W and may not be interchanged with the QT100 series.

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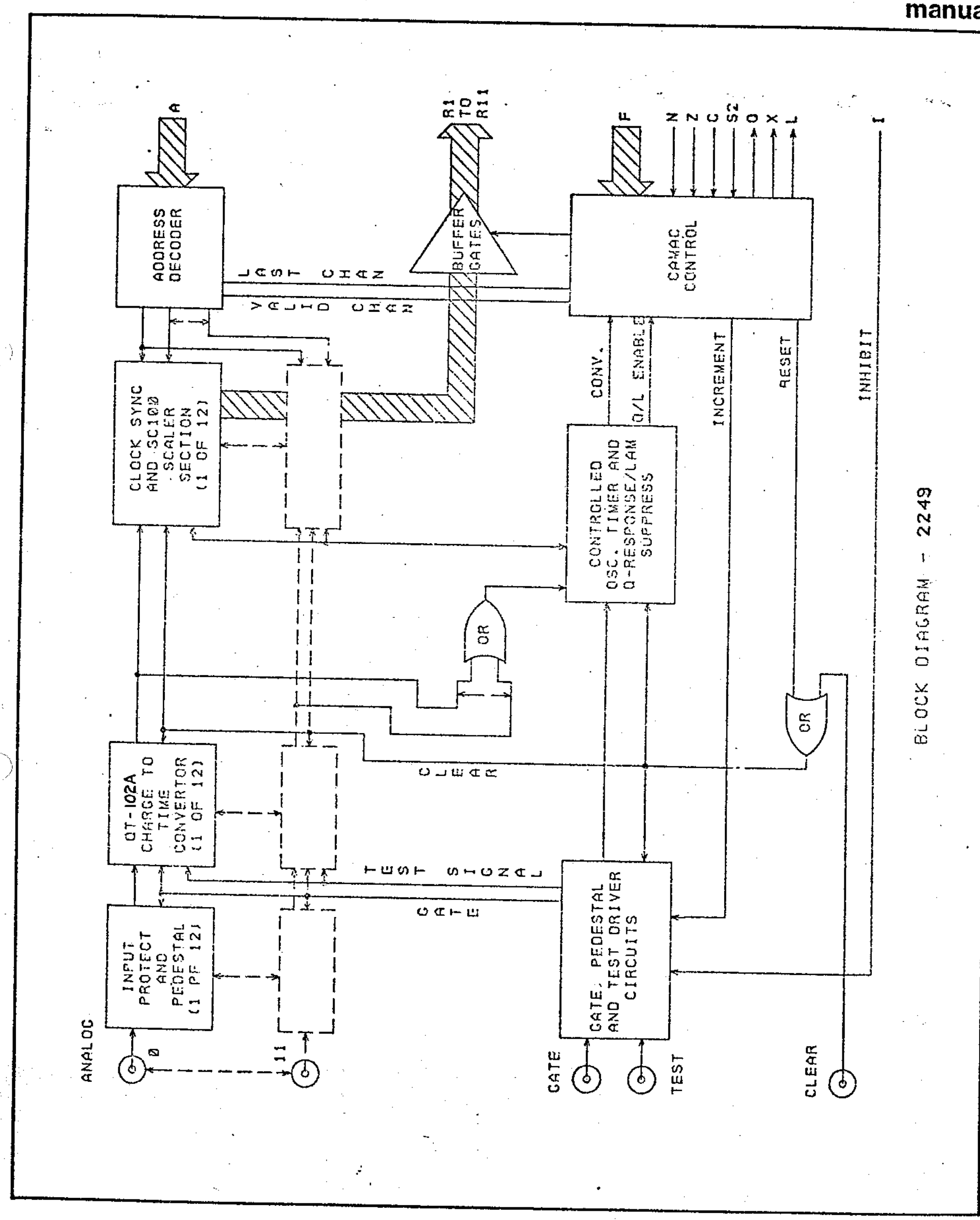


BLOCK DIAGRAM - 2249

The front panel input has 44 Ω of resistance divided into two parts with input clamp diodes at their junctions to provide input protection and reduce crosstalk on large overloads. These resistors, in series with the low input resistance of the linear gate, terminate the input cable to 50 Ω. The stored charge is therefore $Q = {}_0\int^{Tg}(V_{in}/50)dt = {}_0\int^{Tg}I_{in}dt$, where V_{in} is the time dependent voltage on the analog input and Tg is the duration of the gate pulse. The current handling capability of the gate limits the linear range of the analog input to -20 mA (or -1.0 volts across the 50 Ω input).

The required gate input signal is a standard NIM logic level, with recommended duration of 10 nsec minimum to 200 nsec maximum. The analog input is enabled for the duration of the gate.

The QT102 used in the 2249W employs a similar circuit, also with a 50 Ω input impedance. The input is, however, AC coupled via a 6.8 μF capacitor on the circuit board.

The charge delivered to the integrating capacitor through the linear gate is subsequently removed by means of a stable current source (see QTC Block and Waveform diagram). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. This rate is proportional to the difference between the +24 and V_{REF} inputs (Gain Adjust and +12 respectively, on block diagram). The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is greater than a reference level (which is set by the 30 mV bias voltage). The output time duration (T) is therefore proportional to the input charge Q,where time T in microseconds is approximately 0.4 times the charge Q in picocoulombs (i.e., T = 0.4 Q μsec/pC). Operation of the QTC is assured by on-board stabilized ±5 V supplies, keeping a perfect balance in the QTC. The V_{REF} (approximately +12 VDC) tracks the +24 VDC supply, causing the difference (used as the current source reference) to be independent of external supply variations. A small fixed amount of charge is always put into the analog input when a gate pulse is generated. Each ADC channel has been factory calibrated to read between 1 and 2 pC (for gate pulse widths of 50 nsec) when all the inputs are externally loaded with 50 Ω terminations. If the inputs are not terminated, a slightly lower reading will be observed.

A Clear command can be used if desired to clear the 2249 during a conversion cycle. It not only initializes all the digital control and scaler stages, but also, via a leading edge R-C differentiator, clears the analog ramp of the QTC to its quiescent level. The analog clear pulse width is about 300 nsec, leaving the 0.9 µsec remainder of the digital clear for settling in the QTC.

5c. Gate, Test and Pedestal Circuit

The gate generator is operated by either a front panel fast NIM input signal or by an increment signal supplied by the CAMAC controller. The internal gate pulse will actually enable the analog inputs of the A and SG versions about 4 nsec after application and the W version, 7 nsec after. It should, therefore, precede any input by at least that amount. The actual duration will be equal to the input plus about 4 nsec for the A and SG versions, 5 nsec for the W. The increment pulse supplied by the CAMAC control section generates a 100 nsec wide gate pulse (see schematic, sheet 3, and block diagram) upon application of an F(25). Its action is to enable the gate and generate a test pulse.

The test input of the 2249A and W is connected through a precision resistor to a common capacitor C Test in the test circuit. The charge which is stored in this capacitor is equally shared by all channels. The CAMAC Inhibit must be used when testing the unit with F(25). On an INRC command (F(25)·S2), the CAMAC control generates a pulse width 100 nsec which is OR'd into the gate circuit. In addition, if an inhibit condition exists, INCR discharges the test capacitor equally into the 12 QTC's during the 100 nsec gating interval. The test input accepts a positive DC level of 0 to 20 volts to produce a zero to full scale digital output of each ADC.

The trailing edge of the output of the gate generator also produces an initiate pulse which is used to set the busy latch and generates the delayed pulse which starts the conversion cycle. The busy latch feeds back to inhibit the gate within 100 nsec of the trailing edge and is cleared by the reset pulse.

The pedestal is adjusted by injecting charge via a trimmer capacitor (C_{PED}) into the virtual ground of the QTC from the leading edge of the gate pulse where the amount of charge is proportional to the C_{PED} in pFd times the voltage swing of the gate pulse. The trailing edge of the gate is not coupled in because the gate closes and blocks the charge. Because of the charge injection time constant, gate widths narrower than 50 nsec (500 nsec) will not allow all of the injected pedestal charge to be accumulated by the 2249A (2249W). This causes a reduction of the pedestal reading somewhat faster than indicated by the gate dependent term in the specifications.

5d. Clock Synchronizer and Scaler

The output of each QTC hybrid in the 2249 Series is used to gate an oscillator into one half of a LeCroy hybrid SC100 Dual Eleven-Bit Scaler. The Oscillator is synchronously started with respect to the leading edge of the gate (see Controlled Oscillator section). This ensures no fractional pulses during the beginning of the rundown cycle, but care must be taken at the end of the rundown. This is done by the synchronizing stage. Each gate circuit (see schematic sheet 2, and block diagram) supplies an integral number of clock pulses even if the QTC output returns to its quiescent state in the middle of a clock pulse as shown in the previous diagram.

When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4, and A8 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). Along with F(0) or F(2) and N, the 11-bit data will be gated out in parallel to the CAMAC dataway.

5e. Controlled Oscillator

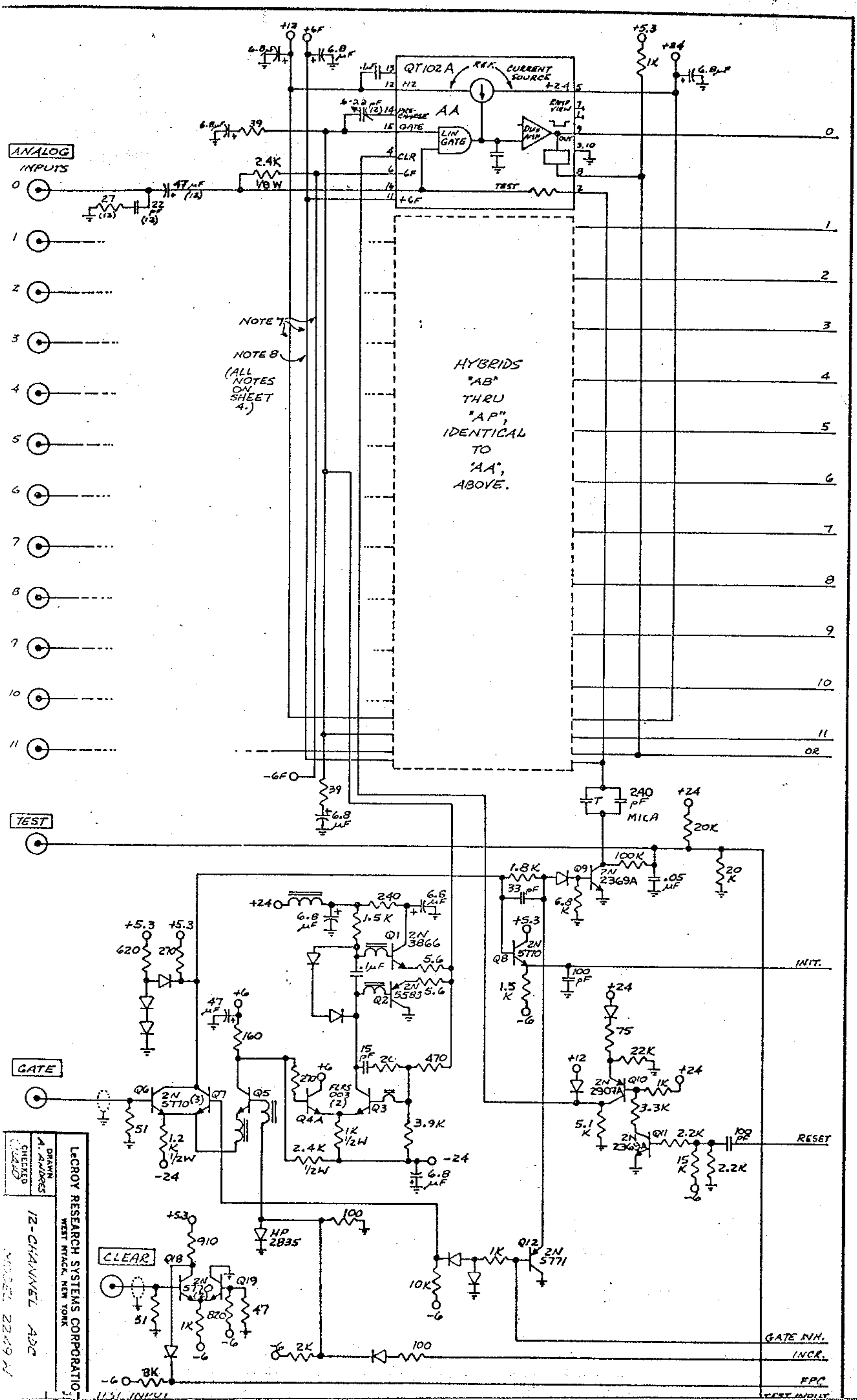
The clock circuit is a modified Colpitts oscillator employing a highly temperature stable choke and a mica capacitor as its resonant elements. Its frequency is 20MHz. The oscillator is gated on 2.2 μsec after the leading edge of the gate pulse. Gating the oscillator in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates noise and nonlinearities caused by not delaying the turn-on (see block diagram). The conversion time is set to 60 or 105 μsec allowing more than enough time for the nominal 50 μsec or 100 μsec full scale conversion to occur for the 2249A and SG or W, respectively. This allows for the ±5% differences from channel to channel, slight temperature drifts, module to module variations, etc., and still ensuring that an overflow can occur for oversized input pulses.

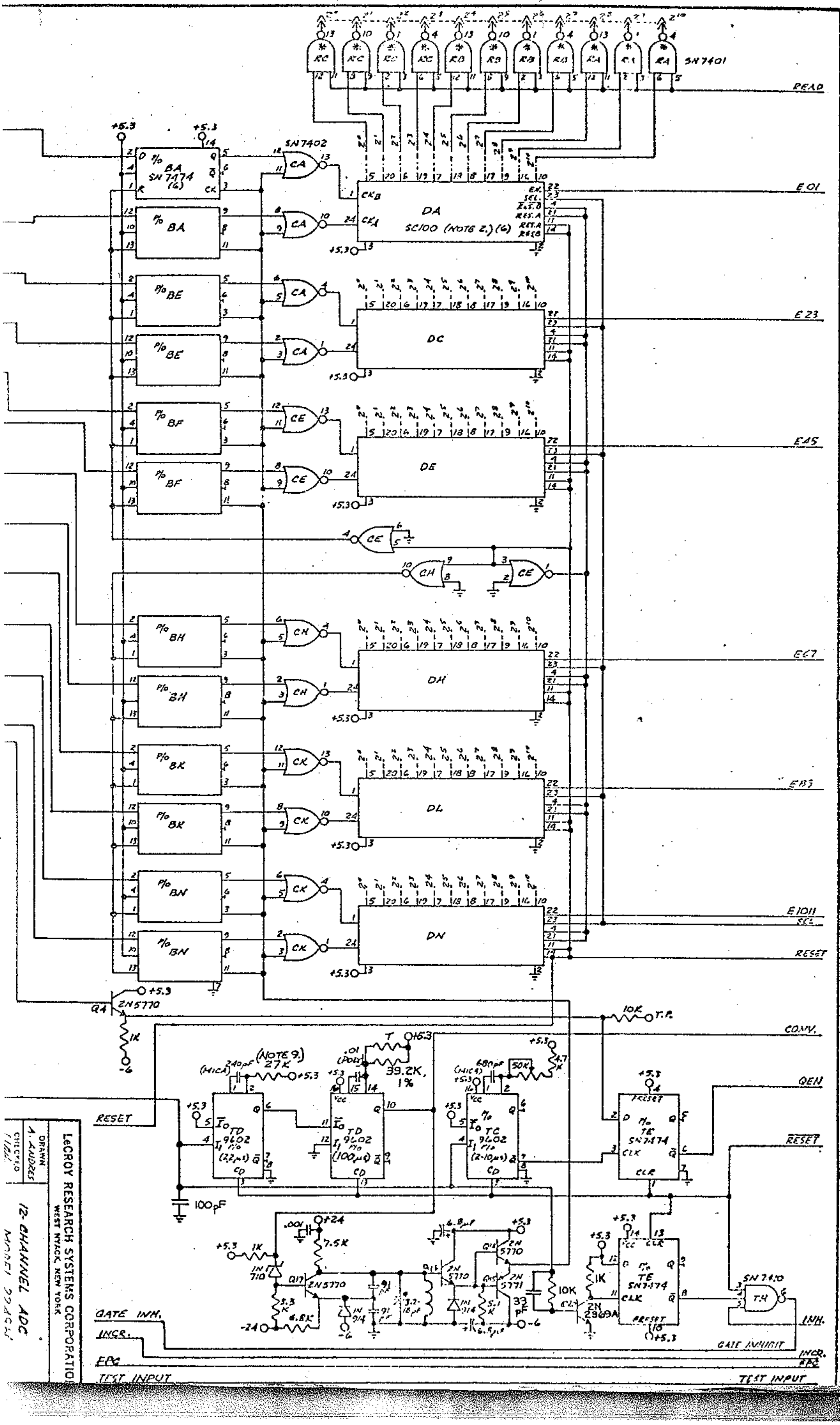
5f. LAM and Q-Response Suppress Circuit

At the beginning of the gate pulse, a monostable is set (see block diagram). The RC time constant of this monostable is adjustable by a side panel potentiometer labeled Q and L SUPPRESS LEVEL ADJUST. When the monostable resets, a latch is reset if one or more of the QTC outputs is still on. If set, this latch disables the Q-response circuit (that normally indicates valid data on an F(0) or F(2) Read Command) and clears the LAM latch. Disabling of the suppress function can be done for either Q-response or L. See the Operational section for more information.

5g. The CAMAC Control

The decoding of the CAMAC "F" functions and N is performed by a 4 line to 16 line decoder (an SN74154). A DC level is generated at the appropriate pin for each valid CAMAC command. Scaler addressing is accomplished using a 4 line to 10 line decoder (an SN7442) on A2, A4, and A8, to enable the appropriate SC100 20 channel scaler hybrid and the A1 bit is used to select the appropriate half of the SC100. X-response is generated for all valid commands, and Q-response and LAM are generated as described in the Q and L Suppress Circuit section.


ANALOG INPUTS
0
1
2
3
4
5
6
7
8
9
10
11
TEST
GATE
CLEAR
QT102A
AA
REF. CURRENT SOURCE
LIN GATE
DUAL AMP
RAMP VIEW
TEST
HYBRIDS "AB" THRU "AP", IDENTICAL TO "AA", ABOVE.
NOTE 7
NOTE 8
(ALL NOTES ON SHEET 4.)
OR
INIT.
RESET
GATE INH.
INCR.
FPC
TEST INPUT
240 pF MICA
LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK
DRAWN A. ANDRES
CHECKED
12-CHANNEL ADC
MODEL 2249 W



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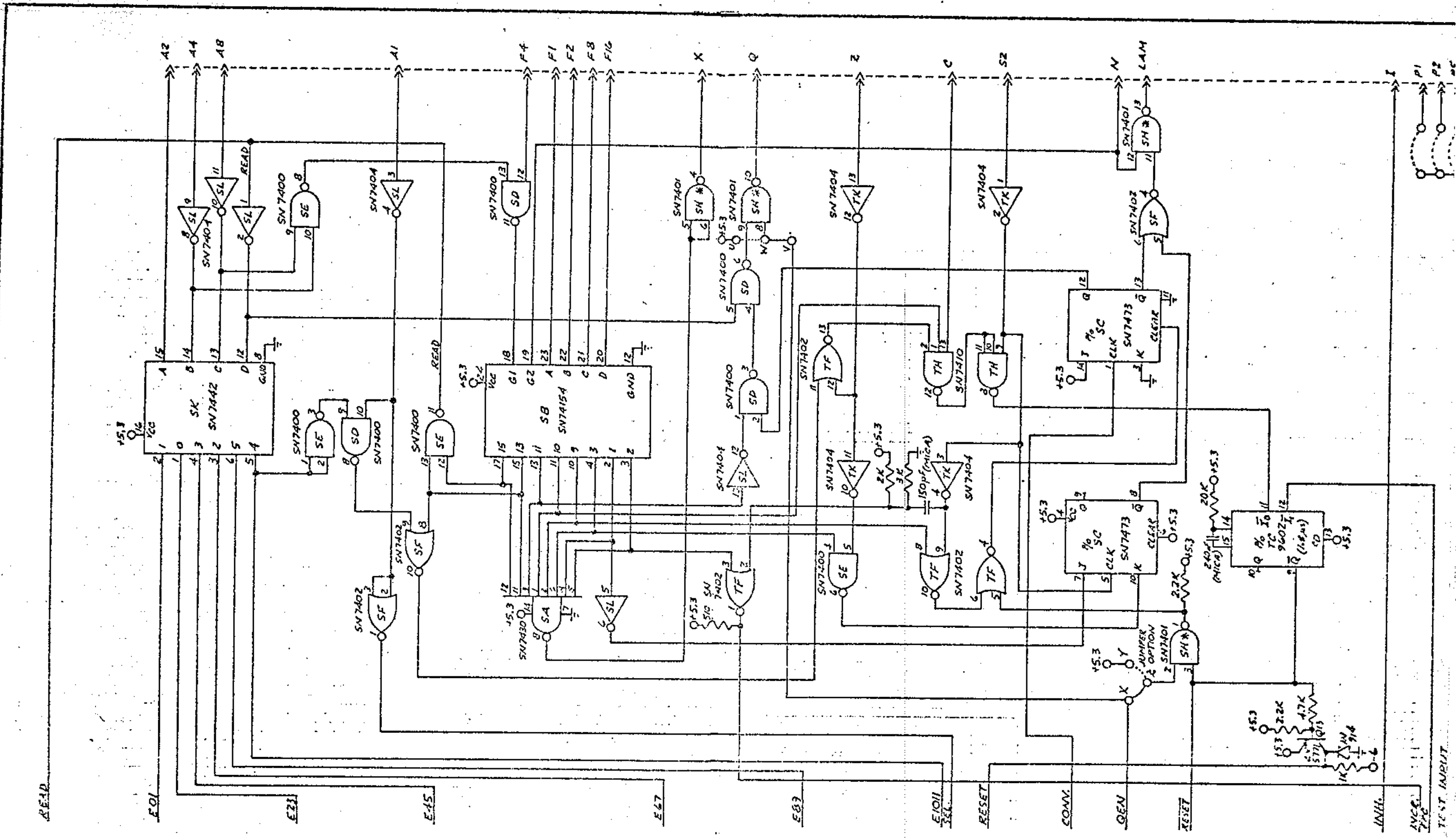
WEST NYACK, NEW YORK

12-CHANNEL ADC

DRAWN A. ANDRES



ALL NOTES ON SHEET 4.

LeCROY RESEARCH SYSTEMS CORPORATIO[N]
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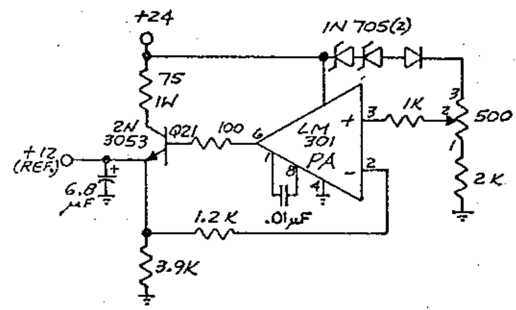
DRAWN A. MIDZES

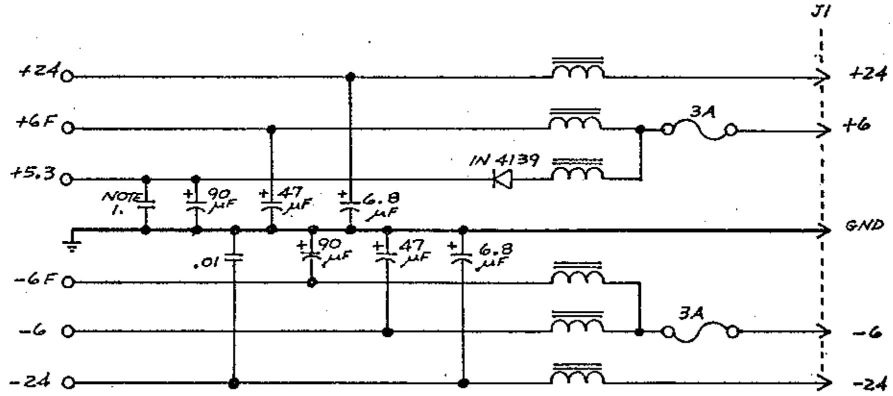
CHECKED

12-CHANNEL ADC

VOLTAGE PINS:

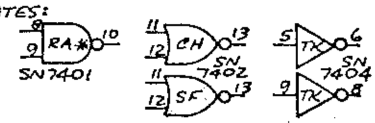
I.C.	REFERENCE	+24V	+12V	+6V	+5.3V	-6V	GND	-24V
LM 301	PA	7					4	
QT102	AA, AB, AC, AD, AE, AF, AH, AK, AL, AM, AN, AP	6	12	11		6	8, 10	
SC100	DA, DC, DE, DH, DL, DN				3		2	
SN 7400	SD, SE,				14		7	
7401	RA, RB, RC, SH				14		7	
7402	CA, CE, CH, CK, SF, TF				14		7	
7404	SL, TK				14		7	
7410	TH				14		7	
7430	SA				14		7	
7442	SK				16		8	
7473	SC				4		11	
7474	BA, BE, BF, BH, BK, BN, TE				14		7	
74154	SB				24		12	
9602	TC, TD				16		8	





NOTES:

1). ADDITIONAL CAPACITORS ON VOLTAGE BUSES, NOT SHOWN
2). ALL SC100-5 ARE WIRE OR-ED.
3). "T" DESIGNATES VALUE TO BE CHOSEN AT TEST.
4). * DENOTES OPEN COLLECTOR.
5). UNUSED GATES:



6). ALL UNIDENTIFIED DIODES ARE IN4448 OR IN914.
7). NOT SHOWN: 2.2 µF CAPACITORS ON +6V, -6V AND +12 BUSES TO GROUND.
8). 6.8µF CAPACITORS ON +6V BUS, NOT SHOWN.
9). THIS RESISTOR VALUE MAY VARY, IF HYBRIDS OTHER THAN QT 102A-5 ARE USED.

LeCROY RESEARCH SYSTEMS CORPORATIO
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12-CHANNEL ADC
MODEL 2249W

DRAWN A. ANDRES
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DATE

MODEL NO 2249W 12-CHANNEL ADC PRINTED 15-Mar-79
LAST REVISION NO 1009 REVISION DATE 13-Mar-79

101 246 **2	PC STOCK DBL SIDED	1 OZ	119	M
102 145 104	CAP CERA DISC 12V	.1 UF	1	
102 245 103	CAP CERA DISC 25V	.01 UF	12	
102 245 503	CAP CERA DISC 25V	.05 UF	1	
102 444 101	CAP CERA DISC 100V	100 PF	4	
102 444 220	CAP CERA DISC 100V	22 PF	12	
102 444 330	CAP CERA DISC 100V	33 PF	2	
102 745 102	CAP CERA DISC 500	.001 UF	1	
102 944 150	CAP CERA DISC 1KV	15 PF	1	
103 437 104	CAP CERA MONO 100V	.1 UF	12	
116 **0 910	CAP DIP MICA SPEC	91 PF	2	
116 515 151	CAP DIP MICA DM10	150 PF	1	
116 515 241	CAP DIP MICA DM10	240 PF	3	
116 525 681	CAP DIP MICA DM15	680 PF	1	
125 535 103	CAP POLYCARB FILM	.01 UF	1	
141 494 225	CAP TANT (MINI)	2.2 UF	7	
142 124 476	CAP TANT DIP CASE	47 UF	18	
142 824 685	CAP TANT DIP CASE	6.8 UF	16	
147 147 *90	CAP ALUM METAL CAN	90 UF	2	
158 639 **1	CAP VARI CERA	6-22 PF	12	
158 819 **1	CAP VARI CERA	3.2-18 PF	2	
161 *30 **0	RES COMP	ZERO OHMS	11	
161 225 242	RES COMP 1/8W 5%	2.4 K	12	
161 335 *47	RES COMP 1/4W 5%	4.7 OHMS	1	
161 335 *56	RES COMP 1/4W 5%	5.6 OHMS	2	
161 335 101	RES COMP 1/4W 5%	100 OHMS	3	
161 335 102	RES COMP 1/4W 5%	1 K	8	
161 335 103	RES COMP 1/4W 5%	10 K	4	
161 335 104	RES COMP 1/4W 5%	100 K	1	
161 335 121	RES COMP 1/4W 5%	120 OHMS	1	
161 335 122	RES COMP 1/4W 5%	1.2 K	1	
161 335 152	RES COMP 1/4W 5%	1.5 K	2	
161 335 153	RES COMP 1/4W 5%	15 K	1	
161 335 161	RES COMP 1/4W 5%	160 OHMS	1	
161 335 182	RES COMP 1/4W 5%	1.8 K	1	
161 335 200	RES COMP 1/4W 5%	20 OHMS	1	
161 335 202	RES COMP 1/4W 5%	2 K	3	
161 335 203	RES COMP 1/4W 5%	20 K	3	
161 335 222	RES COMP 1/4W 5%	2.2 K	4	
161 335 223	RES COMP 1/4W 5%	22 K	1	
161 335 241	RES COMP 1/4W 5%	240 OHMS	1	
161 335 243	RES COMP 1/4W 5%	24 K	1	
161 335 270	RES COMP 1/4W 5%	27 OHMS	12	
161 335 271	RES COMP 1/4W 5%	270 OHMS	2	
161 335 273	RES COMP 1/4W 5%	27 K	1	
161 335 302	RES COMP 1/4W 5%	3 K	2	
161 335 332	RES COMP 1/4W 5%	3.3 K	2	
161 335 333	RES COMP 1/4W 5%	33 K	1	
161 335 390	RES COMP 1/4W 5%	39 OHMS	2	
161 335 392	RES COMP 1/4W 5%	3.9 K	2	
161 335 393	RES COMP 1/4W 5%	39 K	1	
161 335 470	RES COMP 1/4W 5%	47 OHMS	1	
161 335 471	RES COMP 1/4W 5%	470 OHMS	1	

ECO NO.	DATE	DESCRIPTION
231 and 240	9-14-76 9-24-76	DOCUMENTATION FINALIZED. PARTS LIST PUT THRU AS ECO 231 AND ADDITIONAL CHANGES AS ECO 240, TO DISTINGUISH BETWEEN LEVELS OF CHANGE, TEN DAYS APART.
302	12-23-76	CHANGES TO ADAPT UNIT TO QT102A .
303	12-30-76	NEAR Q9: .1 uF CHANGE TO .05 uF IC "TD": AT PIN 14 "T" RESISTOR ADDED. ALSO TIMING CHANGE FROM 60 usec TO 100 usec ON SHEET 4: NOTE 9 ADDED
379	4-28-77	CHANGED ½W 1K RESISTOR TO 1.5K ½W WITH 3K ¼W RESISTOR IN PARALLEL. ASSEMBLY ONLY.
431	7-29-77	PARTS LIST CORRECTION ONLY.
442	8-16-77	CORRECTED ASSEMBLY DRAWING ONLY.
470	9-21-77	CORRECT ASSEMBLY DRAWING ONLY.
1001	3-29-78	PARTS LIST CORRECTION ONLY.
1002	6-13-78	VOIDED. SEE ECO #1006
1003	7-27-78	PARTS LIST CORRECTION.
1004	8-1-78	CHANGED Q9 AND Q11 FROM 2N5770 TO 2N2369A; CHANGED Q10 FROM 2N5771 TO 2N2907A (SHEET 1 OF SCHEMATIC AFFECTED).
1005	8-9-78	PARTS LIST UPDATE ONLY.
1006	8-31-78	REDUCED RATE EFFECT BY CHANGING 6.8 uF AT INPUT TO 47 uF.
1007	12-15-79	100 USEC OUTPUT OF MONOSTABLE 'TD' IS TEMPERATURE STABLIIZED BY SUBSTITUTING 39K CARBON RESISTOR WITH A 39.2K PRECISION RESISTOR (SHEET 2 OF SCHEMATIC AFFECTED).
1008	2-22-79	CORRECTED ASSEMBLY DRAWING.
1009	3-13-79	PARTS LIST CORRECTION ONLY.

REMARKS

LeCROY RESEARCH SYSTEMS CORPORATION
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ENGINEERING CHANGE ORDERS

MODEL 2249W

MODEL NO 2249W   12-CHANNEL ADC   PRINTED 15-Mar-79
LAST REVISION NO 1009   REVISION DATE 13-Mar-79

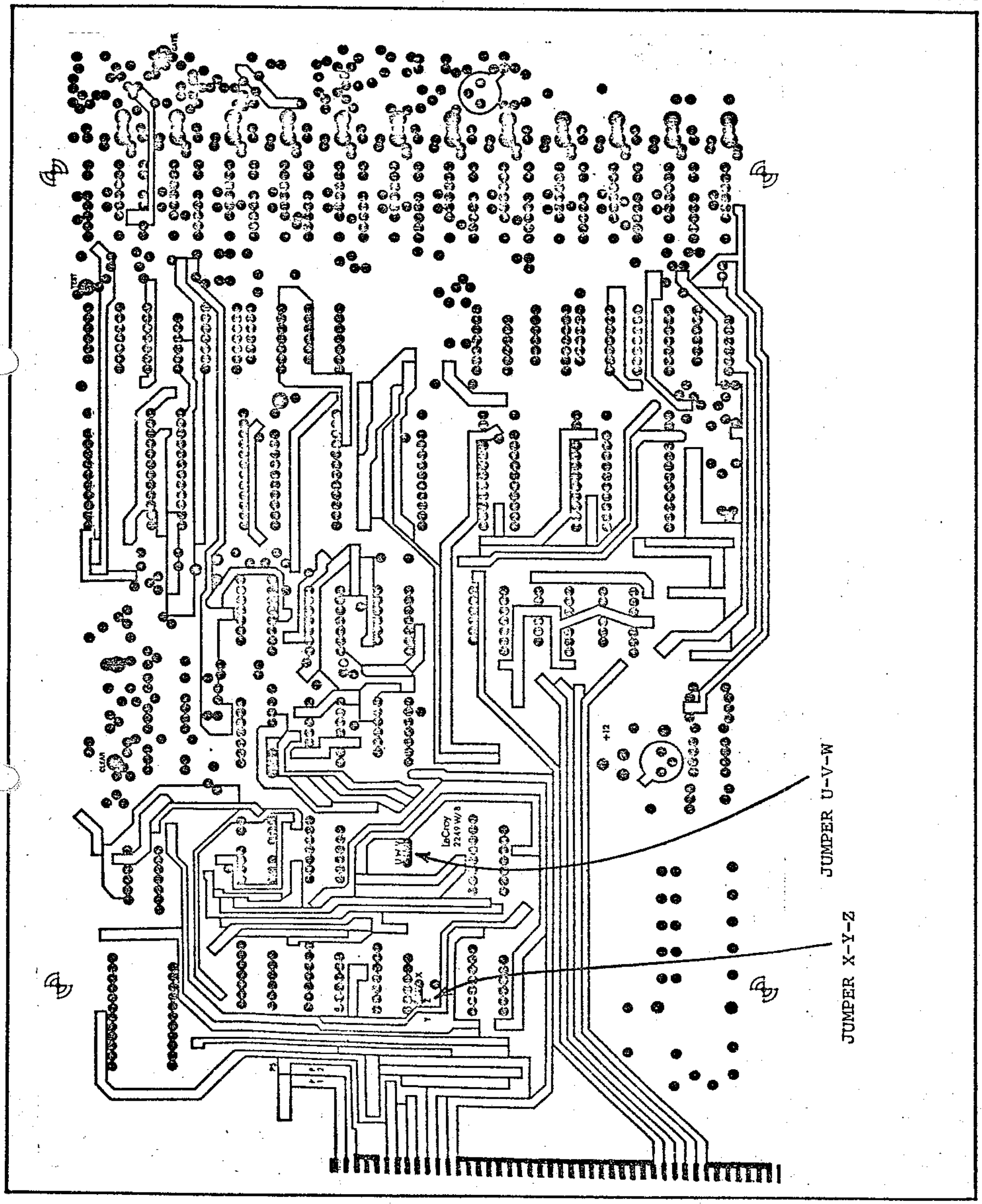
402	*30	**3	GROUND LUG NONLOCK	LEMO	A/R	
402	*30	**4	GROUND STRAP "H"	LEMO	A/R	
433	220	**2	FUSE SUB-MINI	3 AMP	2	
540	202	**1	FRONT PANEL CAMAC SIZE #1		1	M
540	203	**1	SIDE COVER CAMAC STD(LIP)		2	M
540	206	**1	RAIL CAMAC STANDARD		2	
540	209	**1	REAR PANEL CAMAC SIZE #1		1	
555	430	**3	CAPTIVE SCREW ASSEMBLY		1	
712	249	*33	PC PRE	2249W REV-C	1	
722	249	*33	FRONT PNL PREASS'Y	2249W	1	
732	249	*33	SIDE CAMAC LEFT	2249W	1	

NOTE 1   270 170 003 MATCHED SEE SCHEM
NOTE 2
NOTE 3
NOTE 4
NOTE 5
NOTE 6
NOTE 7
NOTE 8
NOTE 9
NOTE 10
NOTE 11
NOTE 12
NOTE 13
NOTE 14
NOTE 15

MODEL NO 2249W   12-CHANNEL ADC   PRINTED 15-Mar-79
LAST REVISION NO 1009   REVISION DATE 13-Mar-79

161	335	472	RES COMP 1/4W 5% 4.7 K	1
161	335	510	RES COMP 1/4W 5% 51 OHMS	2
161	335	511	RES COMP 1/4W 5% 510 OHMS	1
161	335	512	RES COMP 1/4W 5% 5.1 K	2
161	335	621	RES COMP 1/4W 5% 620 OHMS	1
161	335	682	RES COMP 1/4W 5% 6.8 K	2
161	335	750	RES COMP 1/4W 5% 75 OHMS	1
161	335	752	RES COMP 1/4W 5% 7.5 K	1
161	335	821	RES COMP 1/4W 5% 820 OHMS	1
161	335	911	RES COMP 1/4W 5% 910 OHMS	1
161	445	122	RES COMP 1/2W 5% 1.2 K	1
161	445	152	RES COMP 1/2W 5% 1.5 K	1
161	445	242	RES COMP 1/2W 5% 2.4 K	1
161	555	750	RES COMP 1W 5% 75 OHMS	1
168	531	546	RES PREC RN55D 39.2 K	1
181	457	501	RES VARI CERMET 500 OHMS	1
181	457	503	RES VARI CERMET 50 K	1
200	*31	**1	IC 2-IN NAND GATE SN7400N	2
200	*31	**2	IC 2-IN NAND GATE SN7401N	4
200	*31	**3	IC 2-IN NOR GATE SN7402N	6
200	*31	**4	IC HEX INVERTER SN7404N	2
200	*31	**7	IC 3-IN NAND GATE SN7410N	1
200	*31	**9	IC 8-IN NAND GATE SN7430N	1
200	*31	*11	IC J-K M-S FL-FL SN7473N	1
200	*31	*30	IC FLIP-FLOP SN7474N	7
200	*41	**1	IC DECODER SN7442N	1
200	*42	**2	IC MULTIVIBRATOR 9602PC	[illegible]
200	*81	**1	IC DECODER/DEMUL SN74154N	[illegible]
210	*40	*20	IC CHG-TO-TIME CON QT101A	12
210	*90	**1	IC 11-BIT SCALER [illegible]	[illegible]
230	110	**5	DIODE SWITCHING 1N4448	15
235	*50	**1	DIODE RECTIFIER 1N4132	1
240	[illegible]	705	DIODE ZENER 4.85V [illegible]	2
240	225	710	DIODE ZENER 6.8V 1N710A	1
253	*10	835	DIODE HOT CARRIER [illegible]	[illegible]
270	110	**1	TRANSISTOR NPN 2N2369A	[illegible]
270	140	**1	TRANSISTOR NPN 2N3866	[illegible]
270	150	**1	TRANSISTOR NPN 2N3053	[illegible]
270	170	**1	TRANSISTOR NPN 2N5770	10
270	170	**3	TRANSISTOR NPN FMT1190	2
275	110	**1	TRANSISTOR PNP 2N2907A	1
275	140	**2	TRANSISTOR PNP 2N5583	1
275	170	**2	TRANSISTOR PNP [illegible]	2
300	*10	**1	BEAD SHIELDING FERRITE	4
300	*20	**1	BEAD SHIELDING "1/2" SIZE	1
300	*50	**1	CHOKE FERRITE SINGLE LEAD	7
302	[illegible]	**1	INDUCTOR SPECIAL 1.00 UH	1
400	*10	**8	SOCKET IC ST DIP-8	3
400	*20	*14	SOCKET IC ST DIP-14	[illegible]
400	*30	*16	SOCKET IC ST DIP-16	15
400	*40	*24	SOCKET IC ST DIP-24	7
402	*30	**0	CONNECTOR CO-AXIAL LEMO	15
402	*30	**2	SPANNER NUT SMALL OD LEMO	15

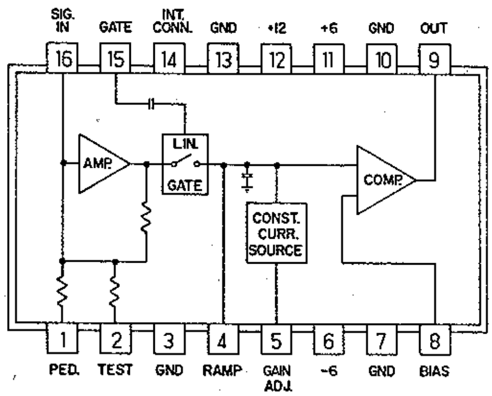
technical information manual



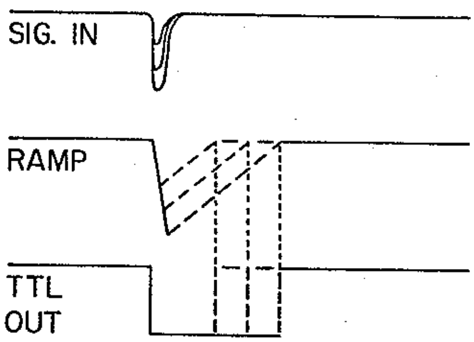
ENGINEERING DEPARTMENT
LeCroy Research Systems Corp.
Spring Valley, New York

technical information

LOGIC DIAGRAM (Top View)



INPUT-TO-OUTPUT WAVEFORMS



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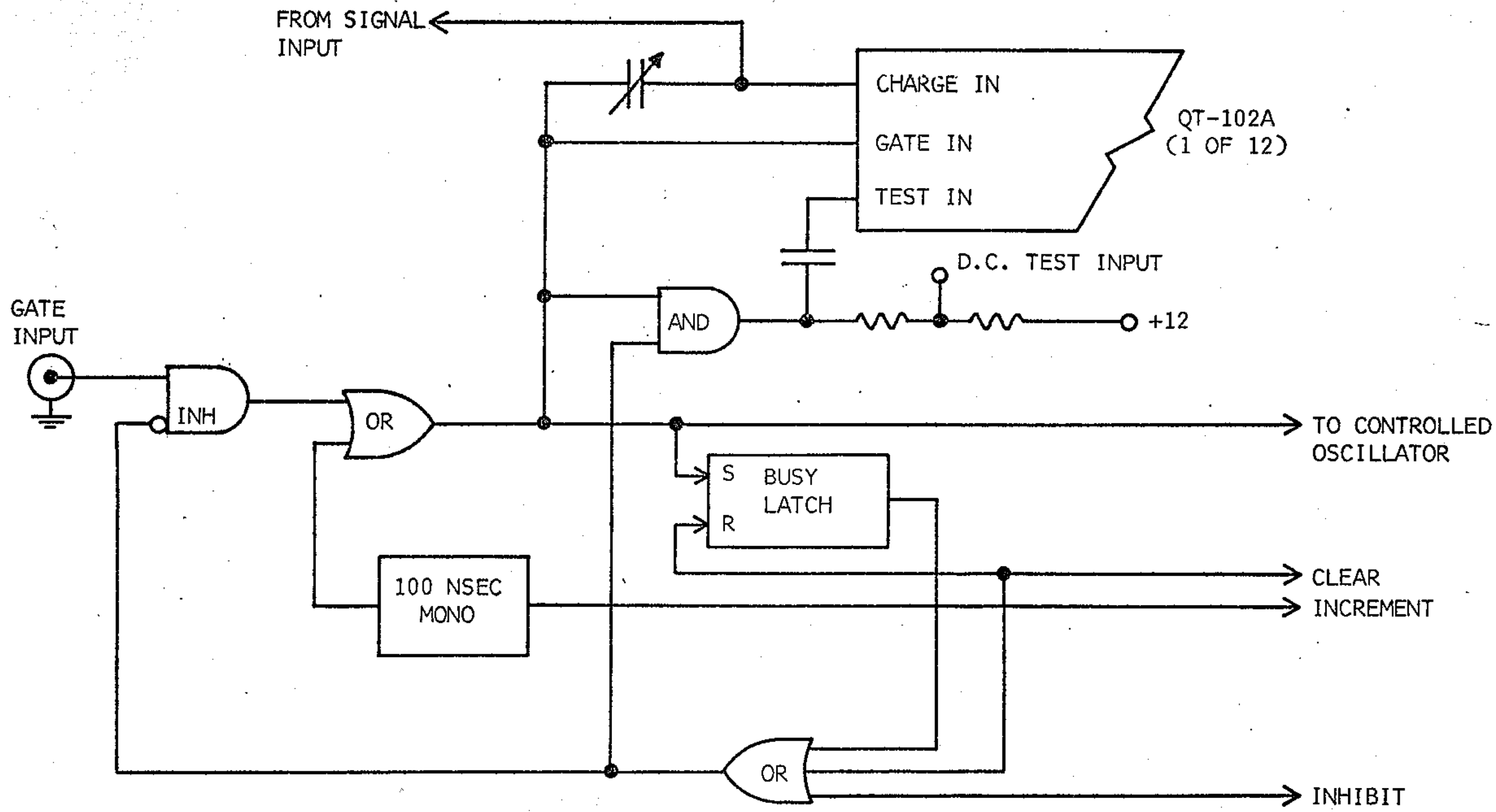
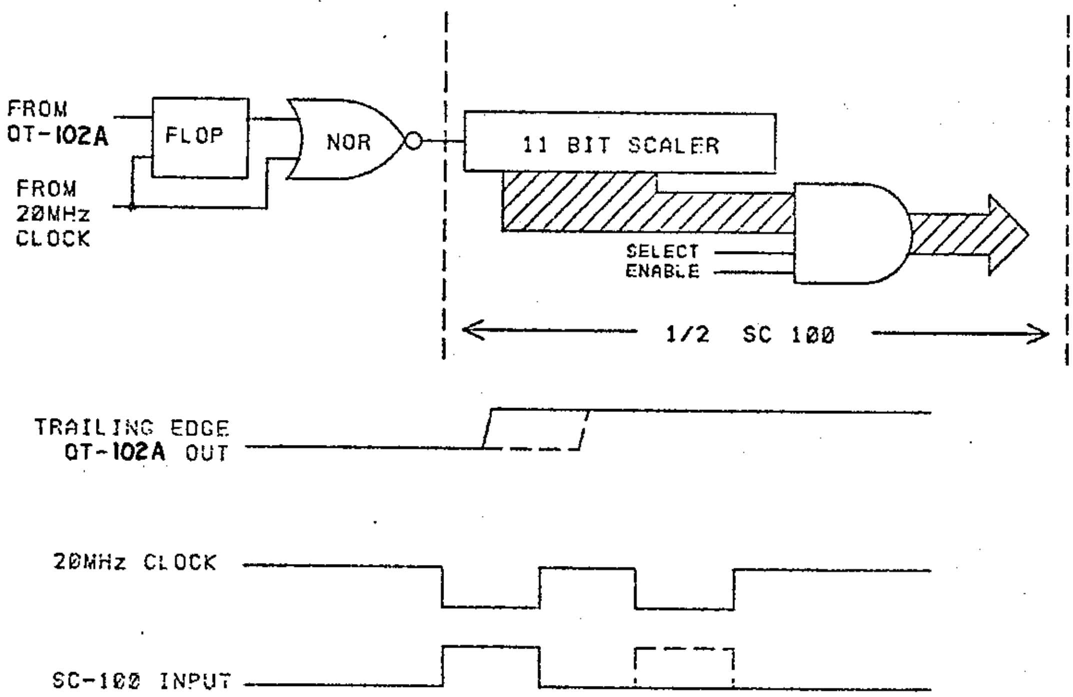


BLOCK DIAGRAM - GATE, PEDESTAL, TEST CIRCUIT

technical
information
manual



BLOCK DIAGRAM - CLOCK SYNC AND SCALER

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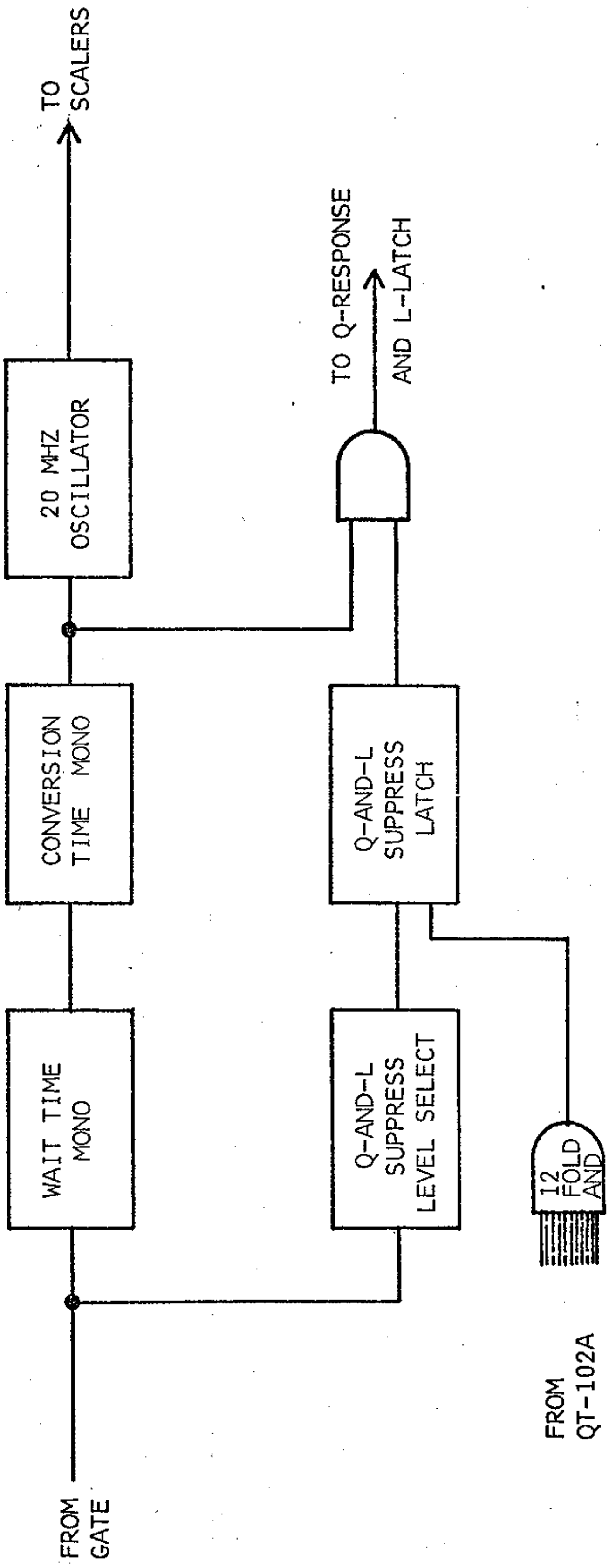

BLOCK DIAGRAM - CONTROLLED OSCILLATOR AND Q-RESPONSE AND L SUPPRESS