S. Rauchfuß

LRS Model 2249
Analog-to-Digital Converter

Technical Information

Model
2249

CAMAC ANALOG TO DIGITAL CONVERTER

Analog Inputs:	Twelve; Lemo-type connectors; charge sensitive (current integrating); direct-coupled, quiescently at approximately + 3 mV; 50 Ω impedance; linear range normally 0 to -1 V; protected to ± 50 volts against 1 usec transients.
Full-Scale Range:	256 pC.
Full-Scale Uniformity:	± 5%.
Integral Non-linearity:	± .25% of reading ± 0.5 pC.
ADC Resolution:	10 bits actual, (0.1%).
Long Term Stability:	Better than 0.25% of reading ± 0.5 pC/week (at constant temperature).
Temperature Coefficient:	- 0.05%/°C typical.
ADC Isolation:	A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC.
Gate Input:	One gate common to all ADC's; LEMO-type connectors; 50 Ω impedance; -600 mV or greater enables; minimum duration, 10 ns; maximum recommended duration, 200 ns (Actual limit approximately 3 microseconds with reduced accuracy; partial analog input must occur within 0.5 usec after opening gate to preserve accuracy), effective opening and closing times; 2 ns.
Fast Clear:	One front-panel input common to all ADC's; LEMO-type connector; 50 Ω impedance; -600 mV or greater clears, minimum duration, 0.5 us; (requires additional 1.5 us settling time after clear).
Residual Pedestal:	Typically 1 + 0.03t picocoulombs (where t=gate duration in nanoseconds) with 50 Ω reverse termination.

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Test:	DC level on front panel " Test" input or optional rear connector P1, P2, or P5 patch points (with externally supplied 75 to 200 usec gate pulse) will inject charge with a proportionality constant of 25 pC/volt into all inputs.
Digitizing Time:	50 us maximum.
Readout Time:	Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete.
Readout Control:	Ready for readout when LAM signal appears. Refer to ESONE Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards.
Data:	The proper CAMAC function and address command normally gates the 10 binary bits plus overflow bit of the selected channel onto the R1 to R11 (2^0 to 2^{11}) Dataway bus lines.
CAMAC Commands:	Z or C: ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. I: Gate input is inhibited during CAMAC "Inhibit" commands. Q: A Q=1 response is generated in recognition of an F(0) or F(3) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q=0) under any other condition. The Q response for empty modules can be suppressed.(See Q and LAM suppression). X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command in generated. L: A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for a duration of B, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules.
CAMAC Function Codes:	F(0): Read registers; requires "N" and "A", A(0) through A(11) are used for channel addresses. F(2): Read registers and Clear module and LAM; requires "N" and "A"; (Clears on A(11) only.

clears everywhere

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F(8): Test Look-At-Me; requires LAM, "N", and any "A" from A(0) to A(11) independent of Disable Look-At-Me.
F(9): Clear module and LAM; requires "N", "S2", and any "A" from A0 to A(11).
F(10): Clear Look-At-Me; requires "N","S2", and any "A" from A(0) to A(11).
F(24): Disable Look-At-Me; requires "N", "S2", and any "A" from A(0) to A(11).
F(26): Enable Look-At-Me; requires "N", "S2", and any "A" from A(0) to A(11).

Q and LAM Suppression: Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered useful. A module containing less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option.

Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module.

Power Requirements: ± 6V, ± 24V: within CAMAC power limits.

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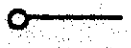
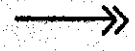
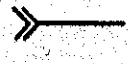
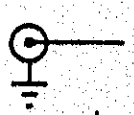
STANDARD DRAFTING SYMBOLS, ELECTRONIC

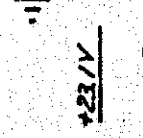

CONNECTION TO ANY GIVEN VOLTAGE.


LINE ENDING AT THE EDGE OF THE SHEET INDICATES CONTINUANCE ON ANOTHER SHEET.


MALE PIN OR CARD EDGE CONTACT.

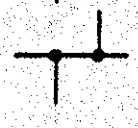

FEMALE PIN, SOCKET OR CARD EDGE CONNECTOR.


COAXIAL CONNECTOR.



QUIESCENT VOLTAGE (EXAMPLE). USUALLY WRITTEN SIDEWAYS.


NO CONNECTION.

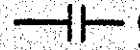

CONNECTION.


RESISTOR, ¼W, ±5%, VALUE IN OHMS (UNLESS SPECIFIED OTHERWISE).


RESISTOR, ¼W, ±1%, VALUE IN OHMS (UNLESS SPECIFIED OTHERWISE).


RESISTOR, VARIABLE, ANY TYPE.


RESISTOR, VARIABLE, ANY TYPE.


CAPACITOR, CERAMIC DISC, 1KV. VALUE IN MICROFARADS (UNLESS SPECIFIED OTHERWISE).

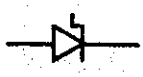

CAPACITOR, COMPOSITION AND VOLTAGE GIVEN. VALUES IN MICROFARADS (UNLESS SPECIFIED OTHERWISE).


CAPACITOR, POLARIZED, VALUES IN MICROFARADS/VOLTS (UNLESS SPECIFIED OTHERWISE).

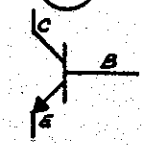

DIODE, 1N914 (UNLESS OTHERWISE INDICATED).


DIODE, ZENER, TYPE GIVEN.

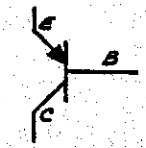

DIODE, TUNNEL, TYPE GIVEN.


DIODE, SNAP, TYPE GIVEN.


LIGHT EMITTING DIODE (LED).

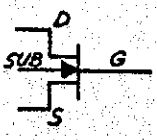


NPN TRANSISTOR, TYPE GIVEN

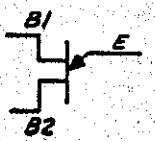


PNP TRANSISTOR, TYPE GIVEN

NOTE: SOME TRANSISTORS MAY BE COLOR CODED AS FOLLOWS:
WHT - 2N4275
YEL - 2N3563
BLU - 2N3565
RED - 2N4258
TAN - SE 3005
GRN - 2N 4250



FIELD EFFECT TRANSISTOR, TYPE GIVEN



TRANSISTOR, UNIJUNCTION


AIR CHOKE (1½" WIRE).


FERRITE BEAD


FERRITE CORE CHOKE, 3 μH, UNLESS OTHERWISE INDICATED.


FERRITE CORE CHOKE, 40 μH, UNLESS OTHERWISE INDICATED.

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LeCroy Research Systems Corp.

Technical Information

BASIC
CAMAC DATAWAY
OPERATING INFORMATION

Condensed from:

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Technical Information

USE OF THE DATAWAY LINES

Communication between plug-in units takes place through the Dataway. This passive multi-wire highway is incorporated in the crate and links the 86-way sockets at all stations. The bus-lines link corresponding pins at all normal stations and, in some cases, the control station. Each individual line links one pin at a normal station to one pin at the control station. The patch pins have no specified Dataway wiring but can be connected to individual points to which patch leads may be attached.

During a Dataway operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Sub-address bus-lines to specify a sub-section of the module or modules, and signals on the Function bus-lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy buy-line, which is available at all stations to indicate that a Dataway operation is in progress.

When a module recognizes a Read command, calling for a data transfer to the controller, it establishes data signals on the Read bus-lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, irrespective of whether or not there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus-line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus-lines. The strobes are used to transfer data from the Dataway into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that it requires attention. Three common control signals are available at all stations, without requiring addressing by a command, in order to Initialize all units (typically after switch-on), to Clear data registers, and to Inhibit features such as data-taking.

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DEFINITION OF COMMANDS

A command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a sub-section of the module or modules (by the four sub-address bus-lines), and the function to be performed (by the five function bus-lines). The command signals are maintained for the full duration of the operation on the Dataway. They are accompanied by a signal on the Busy bus-line which indicates to all units that a Dataway operation is in progress.

Station Number (N)

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the left-hand end as viewed from the front, beginning with Station 1.

Sub-Address (A8, A4, A2, A1)

Different sections of a module are addressed by signals on the four A bus-lines. These signals are decoded in the module to select one of up to sixteen sub-addresses, numbered in decimal from 0 to 15.

Function (F16, F8, F4, F2, F1)

The function to be performed at the specified sub-address in the selected module or modules is defined by the signals on the five F bus-lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 0 to 31. The definitions of the 32 function codes are summarized in the Dataway Command Operations section.

Strobe Signals (S1 and S2)

Two strobe signals S1 and S2 are generated in sequence on separate bus-lines. These signals are used to transfer information between plug-in units via the Dataway or to initiate operations within units. In either case the specific action is determined by the command present on the Dataway. Both strobes are generated during each Dataway command operation, and all plug-in units which accept information from the Dataway do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the Dataway lines. All units which accept data from the Dataway in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of Dataway signals, for example, clearing a register whose output is connected to the Dataway.

DATA

A common parallel highway is used for all transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines (W1-W24)

The controller or other common data source generates data signals on the W bus-lines at the beginning of any 'Write' operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

The Read Lines (R1-R24)

Data signals are set up on the R bus-lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the Dataway operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus-lines at the time of the Strobe S1.

STATUS INFORMATION

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), and Response (Q) lines.

Look-at-Me (L)

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the Dataway line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, Initialize, or by the performance of the specific action which generated the request.

Dataway Busy (B)

The Busy signal is used to interlock various aspects of a system which can compete for the use of the Dataway. Specifically, it is generated during Dataway command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the Dataway lines.

Response (Q)

The Q bus-line is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module.

On all Read and Write commands the signal on the Q bus-line remains static from before S1 until S2. For all other commands the signal on the Q bus-line may change at any time.

Command Accepted (X)

Whenever a module is addressed, it must generate X=1 if it recognizes the command as one it is equipped to perform. The signal on the X bus-line remains static from before X1 until S2.

COMMON CONTROLS

Common control signals operate on all modules connected to them, without requiring to be addressed by a command. In order to provide protection against spurious signals the Initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

Initialize (Z)

The Initialize signal has obsolute priority over all other signals or controls. It sets all units to a basic state by resetting all resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

Inhibit (I)

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 ns.

Clear (C)

This common signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and 3 to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

PRIVATE WIRING

Free Bus-Lines (P1, P2)

Contact P1 and P2 at all mormal stations are linked by two free bus lines. No standard uses are defined for these buses. (Crates manufactured by the older EUR4100e(1969) standards may not have these pins bussed.)

Patch Contacts (P3-P7)

Contacts P3-P5 at each normal station, and P1-P7 at the control station, are not wired to Dataway lines. They are available for special-purpose patch connections.

DATAWAY COMMAND OPERATIONS

A command is composed of signals on the Station Number line or lines, the Sub-Address lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status information on the Q line. The two Strobes S1 and S2 must be generated in each Dataway command operation and control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 2. In this table the term 'register' is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the 4 sub-address lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command then the performance of that command should be reset the Look-at-Me source.

Read Commands (Function Codes 0-7)

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus-lines. Data signals are set up on the R bus-lines by the module as soon as the 'Read' command is recognized, and the appropriate status signal connected to the Q bus-line. The R and Q signals reach a steady state before S1, and are maintained for the full duration of the Dataway command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have cosecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Read command. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

Code 0, Read Group 1 Register

This command selects, by sub-address, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

Code 1, Read Group 2 Register

Same as Code 0, except command selects register from the second group.

Code 2, Read and Clear Group 1 Register

Same as Code 0, except the module register is cleared at time S2.

Code 3, Read Complement of Group 1 Register

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

Code 4 - 7

Unassigned at this time.

CONTROL COMMANDS (Function Codes 8 - 15)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed on the Q bus-line in any of these commands. The signal on the Q bus-line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by strobe 2.

Code 8, Test Look-at-Me

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus-line.

Code 9, Clear Group 1 Register

This command selects, by sub-address, a register from the first group in the module and clears the contents of this register.

Code 10, Clear Look-at-Me

Same as Code 8, except the Look-at-Me source is cleared at time S2.

Code 11, Clear Group 2 Register

Same as Code 9, except command selects register from the second group.

Code 12-15

Unassigned at this time.

WRITE COMMANDS (Function Codes 16-23)

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus-lines. The controller or other common data source generates data signals on the W bus-lines at the beginning of the "Write" operation. The module connects the appropriate status signal to the Q bus-line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the Dataway command operation unless the status of the signal source is changed at Strobe 2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive sub-addresses starting at sub-address 0. At each of these sub-addresses the module generates Q = 1 in response to the appropriate Write function. At the next sub-address in sequence (where there is not a data register) the response is Q = 0. At all remaining sub-addresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

Code 16, Overwrite Group 1 Register

This command selects, by sub-address, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus-lines by the controller.

Code 17, Overwrite Group 2 Register

Same as Code 16, except command selects register in the second group.

Code 18, Selective Overwrite Group 1 Register

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

Code 19, Selective Overwrite Group 2 Register

Same as Code 18, except command selects register in the second group.

Code 20 - 23

Unassigned at this time.

CONTROL COMMANDS (Function Codes 24 - 31)

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus-lines. However, information may be conveyed by the Q bus-line in any of these commands. The signal on the Q bus-line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by strobe S2. Precautions must be taken to ensure that information is not lost due to Q signals appearing between S1 and S2.

Code 24, Disable

This command selects, by sub-address, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

Code 25, Increment Preselected Registers

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the sub-address.

Code 26, Enable

This command enables the feature of the module selected by the sub-address, e.g., a Look-at-Me source or a data input.

Code 27, Test Status

This command selects, by sub-address, any feature of a module other than a source of a Look-at-Me request, and tests it by producing a response on the Q bus-line.

Code 28 - 31

Unassigned at this time.

Technical Information

DIGITAL SIGNAL STANDARDS ON THE DATAWAY

The potentials for the binary digital signals on the Dataway lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic '0' and the low state (near ground potential) corresponds to logic '1'. Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the '0' state.

It is an essential feature of the Dataway that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one controller-like unit in a crate. The Inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during Dataway operations.

Voltage standards for Dataway Signals

All Dataway Signals must conform to the voltage levels as follows:

Pull-up current sources for all Dataway bus-lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is one and only one current source per line. The minimum pull-up current when the Dataway line is at +3.5 V is defined in Table 4 as 2.5 mA but, if the controller generates Dataway signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals and for the L signals in the unit receiving the signals so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller) together. The Q and R lines will generally have many units generating the signals (say 20) with a few units (maximum 4) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

Technical Information

Timing of Dataway Signals

The sequence of events during a single Dataway operation is shown in Timing Diagram, Page 13C, by means of simplified signal waveforms. The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the '1' state. Other command and data lines may, of course, be in the '0' state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchroism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earlies time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t_0 - t_9, with the following significance:

Points t_0, t_3, t_6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal Dataway with no capacitative loading.

Points t_9, t_5, t_8 represent similarly the initiation of the positive-going edges of the same signals.

Points t_2, t_{11} are the latest times at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

Points t_1, t_3, t_4, t_7 represent the latest times at which the received signals are permitted to reach a maintained '1' state, and therefore refer to the last negative-going transition across the + 0.8 V threshold.

Points t_6, t_9, t_{10}, t_{12} represent the latest times at which the received signals are permitted to reach a maintained '0' state, and therefore refer to the last positive-going transition across the + 2.0 V threshold.

Technical Information

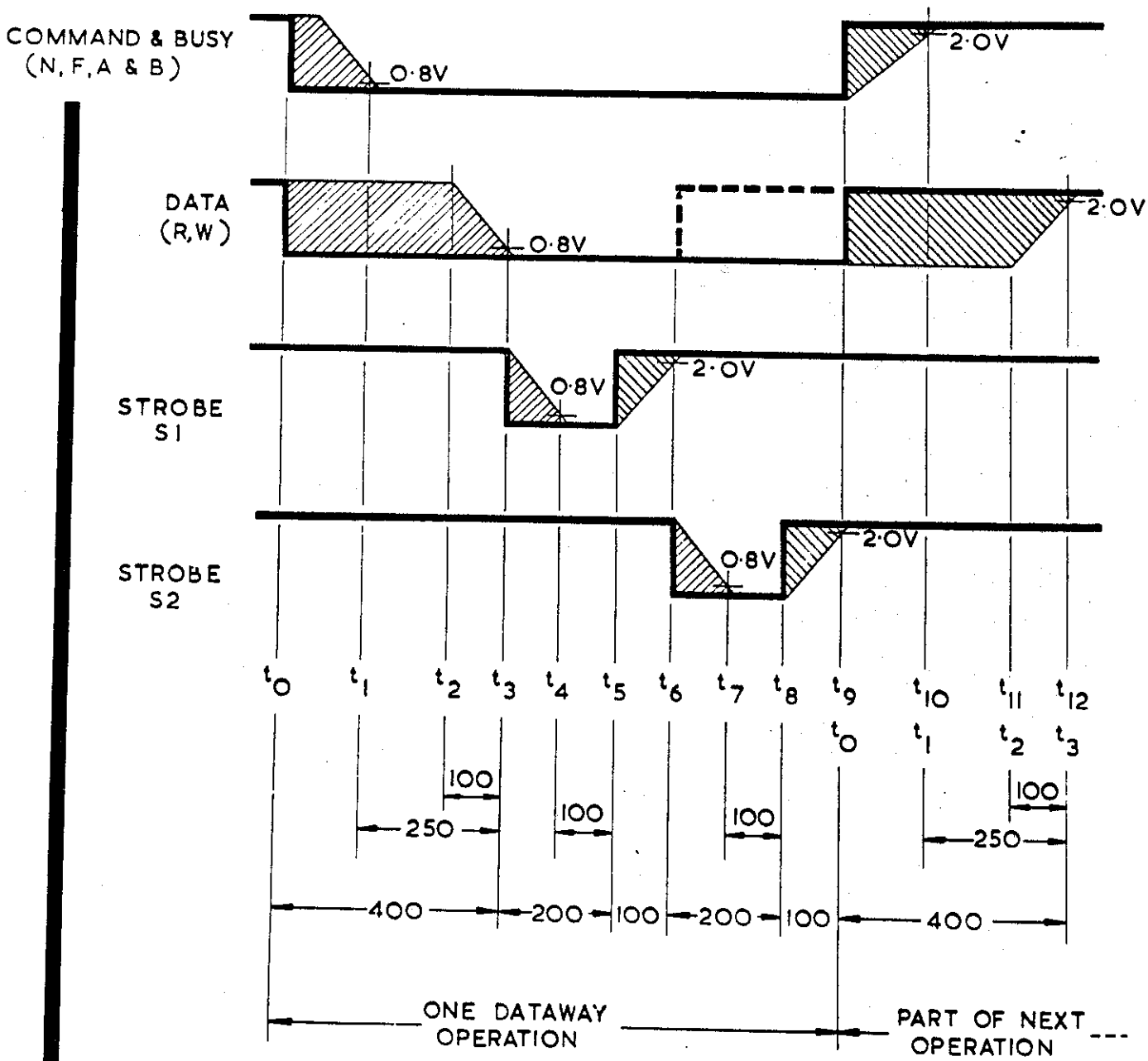
Controllers must initiate the negative and positive going edges of the command and strobe signals at intervals not less than those defined by t_3, t_5, t_6, t_8 and t_9. Modules respond to the command within the most adverse value of $(t_1 - t_2)$; i.e., 100 ns. The electrical characteristics of the Dataway and connections from it into units must allow signals to rise and fall within the minimum times for $(t_0 - t_1)$, $(t_2 - t_3)$ etc.

The next Dataway operation must not start before t_9.

The extreme case is shown in Timing Diagram, Page 15C, with the next operation starting at t_9, so that $t_9 - t_{12}$ of one operation coincide with $t_0 - t_3$ of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive Dataway operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data there could be a complete absence of signal transitions between t_0 and t_3.

Technical Information

DATAWAY TIMING



TIMES GIVEN ARE MINIMUM VALUES IN NANOSECONDS

TIMING OF A DATAWAY OPERATION.

ENGINEERING DEPARTMENT
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Technical Information

POWER SUPPLIES

The voltage tolerances and current loadings are specified below. The specified tolerances in voltage refer to the voltage measured at the contacts of the Dataway sockets and must be maintained under the worst combination of factors such as a.c. mains voltages and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

Note that the maximum currents stated in the below table are subject to the over-all restrictions as follows:

1. The current carried by any contact of the Dataway socket must not exceed 3 A.
2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.
3. The power dissipation per single width station should not, therefore, normally exceed 8 W; however, under special circumstances this rating may be increased to a maximum of 25 W provided suitable precautions are taken to comply with total power dissipation and current loadings.

The resistance between any point on the Dataway OV power return bus-line and the point at which the power supply is joined to the crate wiring must not exceed 2 milliohms.

Technical Information

Supply Voltage	Voltage Tolerance	Maximum Current Loads	
		In the Plug-in (per unit width) See Notes (1) & (3) Above	In the crate See Note (2) Above
Mandatory			
+24V d.c.	± 0.5%	1A	6A
+ 6V d.c.	±2.5%	2A	25A
- 6V d.c	±2.5%	2A	25A
-24V d.c	±0.5%	1A	6A
OV			
Additional (as required)			
+200V d.c.	+60V, -20V		0.1A
+ 12V d.c.	± 0.5%		
- 12V d.c.	± 0.5%		
117V a.c.	+10%, -12%		0.5A

Technical Information

CAMAC FUNCTION CODES

Function No.	Function	Function Line Coding					
		F 16	F 8	F 4	F 2	F 1	No.
0	Read Group 1 Register	0	0	0	0	0	0
1	Read Group 2 Register	0	0	0	0	1	1
2	Read and Clear Group 1 Register	0	0	0	1	0	2
3	Read Complement of Group 1 Register	0	0	0	1	1	3
4	Non-standard	0	0	1	0	0	4
5	Reserved	0	0	1	0	1	5
6	Non-standard	0	0	1	1	0	6
7	Reserved	0	0	1	1	1	7
8	Test Look at Me	0	1	0	0	0	8
9	Clear Group 1 Register	0	1	0	0	1	9
10	Clear Look at Me	0	1	0	1	0	10
11	Clear Group 2 Register	0	1	0	1	1	11
12	Non-standard	0	1	1	0	0	12
13	Reserved	0	1	1	0	1	13
14	Non-standard	0	1	1	1	0	14
15	Reserved	0	1	1	1	1	15
16	Overwrite Group 1 Register	1	0	0	0	0	16
17	Overwrite Group 2 Register	1	0	0	0	1	17
18	Selective Overwrite Group 1 Register	1	0	0	1	0	18
19	Selective Overwrite Group 2 Register	1	0	0	1	1	19
20	Non-standard	1	0	1	0	0	20
21	Reserved	1	0	1	0	1	21
22	Non-standard	1	0	1	1	0	22
23	Reserved	1	0	1	1	1	23
24	Disable	1	1	0	0	0	24
25	Increment Preselected Registers	1	1	0	0	1	25
26	Enable	1	1	0	1	0	26
27	Test Status	1	1	0	1	1	27
28	Non-standard	1	1	1	0	0	28
29	Reserved	1	1	1	0	1	29
30	Non-standard	1	1	1	1	0	30
31	Reserved	1	1	1	1	1	31

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Technical Information

PIN ALLOCATION AT NORMAL STATION

VIEWED FROM FRONT OF CRATE

Free Bus Line	P1	B	Busy Bus Line
Free Bus Line	P2	F16	Function Bus Line
Individual Patch Point	P3	F8	Function Bus Line
Individual Patch Point	P4	F4	Function Bus Line
Individual Patch Point	P5	F2	Function Bus Line
Command Accepted	X	F1	Function Bus Line
Bus Line with Patch Point – Inhibit	I	A8	Sub–Address Bus Line
Bus Line with Patch Point – Clear	C	A4	Sub–Address Bus Line
Individual Lines with Patch Points – Station Number	N	A2	Sub–Address Bus Line
Individual Lines with Patch Points – Look-at-Me	L	A1	Sub–Address Bus Line
Bus Line – Strobe 1	S1	Z	Initialize Bus Line
Bus Line – Strobe 2	S2	Q	Response Bus Line
	W24	W23	
	W22	W21	
	W20	W19	
	W18	W17	
	W16	W15	
	W14	W13	
	W12	W11	
	W10	W9	
	W8	W7	
	W6	W5	
	W4	W3	
	W2	W1	
	R24	R23	
	R22	R21	
	R20	R19	
	R18	R17	
	R16	R15	
	R14	R13	
	R12	R11	
	R10	R9	
	R8	R7	
	R6	R5	
	R4	R3	
	R2	R1	
Reserved for –12 volts D.C.	–12	–24	–24 volts D.C.
Reserved for +200 volts D.C.	+200	–6	–6 volts D.C.
Reserved 117 volts A.C. Live	ACL	ACN	Reserved for 117 volts A.C. Neutral
Reserved	Y1	E	Reserved for Clean Ground
Reserved for +12 volts D.C.	+12	+24	+24 volts D.C.
Reserved	Y2	+6	+6 volts D.C.
0 volts (Power return)	0	0	0 volts (Power Return)

24 Write Bus Lines

W1 = least significant bit
W24 = most significant bit

24 Read Bus Lines

R1 = least significant bit
R24 = most significant bit

Control Station is identical except that:

(1) Even numbered R and W lines are used for L.
(2) Odd numbered R and W lines are used for N.
(3) Pins P1 and P2 are individual patch points.
(4) Pins N and L become P6 and P7.

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Technical Information

STANDARD DATAWAY USAGE

Title	Designation	Pins	Use at a Module
Command			
Station Number	N	1	Selects the module (Individual line from control station).
Sub-Address	A1, 2, 4, 8.	4	Selects a section of the module.
Function	F1, 2, 4, 8, 16.	5	Defines the function to be performed in the module.
Timing			
Strobe 1.	S1	1	Controls first phase of operation (Dataway signals must not change).
Strobe 2.	S2	1	Controls second phase (Dataway signals may change).
Data			
Write	W1 – W24	24	Bring information to the module.
Read	R1 – R24	24	Take information from the module.
Status			
Look-at-Me	L	1	Indicates request for service (Individual line to control station).
Response	Q	1	Indicates status of feature selected by command.
Busy	B	1	Indicates that a Dataway Operation is in progress.
Command Accepted	X	1	Indicates recognition of a valid command.
Common Controls			Operate on all features connected to them, no command required.
Initialize	Z	1	Sets module to a defined state. (Accompanied by S2 and B)
Inhibit	I	1	Disables features for duration of signal.
Clear	C	1	Clears Registers. (Accompanied by S2 and B)
Private Wiring			
Free Bus Lines	P1 – P2	2	Free for unspecified common connections.
Patch Points	P3 – P5	3	Free for unspecified interconnections.
Mandatory Power Lines			The Crate is Wired for Mandatory and Additional Lines
+24V D.C.	+24	1	
+ 6V D.C.	+6	1	
– 6V D.C.	–6	1	
-24V D.C.	–24	1	
OV	0	2	Power return.
Additional Power Lines			Lines are Reserved for the Following Power Supplies
+200V D.C.	+200	1	Low current for indicators etc.
+ 12V D.C.	+12	1	
– 12V D.C.	–12	1	
117V A.C. (Live)	ACL	1	
117V A.C. (Neutral)	ACN	1	
Clean Ground	E	1	Reference for circuits requiring clean ground.
Reserved	Y1, Y2	2	Reserved for future allocation.
TOTAL		86	