OPERATOR'S MANUAL

CAMAC MODEL 2323A
DUAL GATE AND DELAY
GENERATOR

May 1987

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1 GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation, packaged separately, should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

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DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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2 PRODUCT DESCRIPTION

GENERAL DESCRIPTION

The CAMAC Model 2323A is a fully programmable dual gate and delay generator. The gate pulse output width is programmable via CAMAC or manual control over the range of 100 nsec (50 nsec at reduced accuracy) to 10 seconds.

The delay signal starts at the trailing edge of the Gate pulse. Its width also is programmable via CAMAC or manual control to values of 10 nsec, 30 nsec, 100 nsec, or 300 nsec. Settings of both gate and delay signals are overwritten under CAMAC control, whereas they are incremented under manual control. Values may be read back via CAMAC.

The Model 2323A is triggerable by either an external START pulse or by a CAMAC command. In the Latched mode, the output pulse width is determined by the time between the START and STOP inputs or CAMAC commands.

The Model 2323A provides NIM outputs of the Gate and Delay and a complementary NIM output of the gate signal. Also, jumper options allow selection of either an ECL gate or delay output and selection of either a TTL gate or delay output of either positive or negative polarity.

FRONT-PANEL DESCRIPTION

Displays

LED's are used to indicate:

1. The channel currently or last selected (A or B)
2. The Gate duration setting (3-1/2 Digit Display)
3. The Gate range setting (μsec, msec, sec, L (latched mode))
4. The Delay width (10, 30, 100, 300 nsec)
5. Channels currently triggered (CHAN A or CHAN B)

Controls

The 3-position (A-OFF-B) CHAN switch is used to select either CHAN A or CHAN B. Settings can be changed manually only while the CHAN switch is depressed.

The pushbutton UP (DOWN) switch is used to increment (decrement) the display setting. The display increments (decrements) at about 2 Hz for the first eight counts and then changes to a faster rate.

The pushbutton RANGE switch selects the order of magnitude of the gate setting and advances the decimal point and the range setting indicators accordingly. The indicator advances from μsec to sec and then the display goes blank for two increments as the L indicator comes on. This is the Latched mode.

The pushbutton DELAY WIDTH switch selects the width of the Delay pulse and advances the Delay width indicators accordingly.

The 2-position, locking TRIGGER switches (one for each channel) select either the positive-going (+) or the negative-going (-) edge of the START pulse as the trigger.

The front-panel multi-turn potentiometers and test points (one for each channel) are used to set the threshold above which the START pulse will trigger the unit. The range of adjustment is -3 V to +3 V and is operated in conjunction with the polarity selecting trigger control described above.

The 2-position, locking CAMAC switch selects either manual control (OFF) or CAMAC control (ON) as long as they are not overwritten by a CAMAC write command.

Inputs

START is a bridged, high impedance pair of inputs via two Lemo-type connectors, allowing for the possibility of daisy chaining START signals. The input threshold level is factory adjusted to -400 $\pm$ 50 mV to accept NIM inputs and is adjustable over a range of $\pm$3 V via the front-panel potentiometer. The positive or negative-going edge (selected by the TRIGGER switch) of the START signal initiates the timing cycle. A 50 Ω terminator should be employed in the unused START input. Alternatively, there is space available on the board for an optional 1/8 W, 50 Ω terminating resistor.

STOP is a standard NIM input via a Lemo connector, with an impedance of 50 Ω. In the latched or the preset mode, the STOP signals terminates the timing cycle.

OR is a standard NIM input via a Lemo connector, with an impedance of 50 Ω. The OR signal produces a gate output for as long as it is asserted.

BLANK is a standard NIM input via a Lemo connector with an impedance of 50 Ω. The BLANK signal cancels the Gate outputs (including an OR signal) for as long as it is asserted.

Outputs

NIM is a NIM-standard output via a Lemo connector. This signal goes low (-16 mA) for the Gate duration. The risetime is $\leq$2.5 nsec and falltime is $\leq$2.5 nsec.

Complementary NIM is a NIM-standard output via a Lemo connector. This signal goes high (0 mA) for the Gate duration. The risetime is $\leq$2 nsec and falltime is $\leq$2.5 nsec.

DLY is a NIM-standard output via a Lemo connector. This signal goes low (-16 mA) at the trailing edge of the gate signal

for the delay duration (10, 30, 100, or 300 nsec). It will be reset high if the leading edge of a new gate occurs during the delay pulse. The risetime is $\leq$2 nsec and the falltime is $\leq$2.5 nsec.

TTL is an open-drain FET output connected to the front-panel Lemo connector. This signal has the option of being normally off (+ polarity) and going high for the gate or delay duration, or normally on (-polarity) and going low for the gate or delay duration. Polarity and gate or delay options are selectable with shorting plugs*. Factory set for negative polarity. There is a factory installed 51 Ω 1/2 W pullup resistor to +5 V. If parallel operation of several 2323A's is desired, this resistor should be removed from all but one output to prevent excessive current. *Note: The 51 Ω pullup (to match 50 Ω cable) will enable operation with output pulse durations greater than 30 nsec. For 10 nsec operation use the NIM output discussed above.*

+E- is an ECL differential pair output via a 2-pin connector. The + (-) signal goes high (low) (-0.8 V (-1.7 V)) for either the gate or delay duration. These options are selectable with shorting plugs*, factory set for Gate output.

OPTIONS

The following options are made available to the user (see Figure 1). They are located at the front-panel end of the main pc board. Note that there are two identical sections, each taking up half of the board space. Channel A(B) is located at the top (bottom).

* Connections made at factory (see Figure 1).

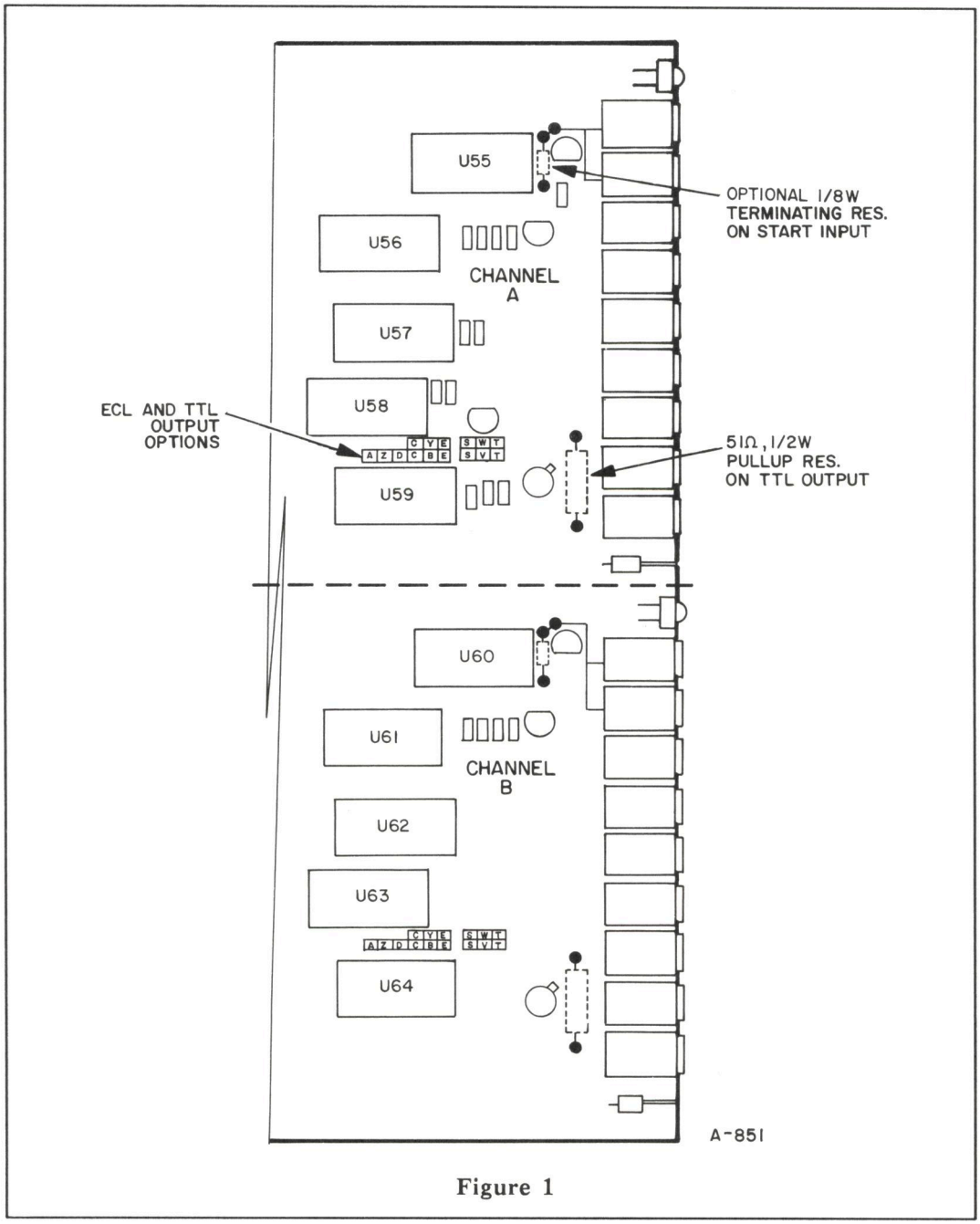

U55
OPTIONAL 1/8W
TERMINATING RES.
ON START INPUT
U56
CHANNEL
A
U57
U58
ECL AND TTL
OUTPUT
OPTIONS
C Y E
A Z D C B E
S W T
S V T
51Ω, 1/2W
PULLUP RES.
ON TTL OUTPUT
U59
U60
U61
CHANNEL
B
U62
U63
U64
A-851

Figure 1

Should the user wish to terminate the START input with a resistor to ground (typically 50 Ω), space is available at the front-panel side of U55 (U60), the AM865's, for an 1/8 W resistor.

The TTL and ECL outputs are factory set for the Gate output and the TTL polarity is negative (normally on). However, should the user wish to set either or both of these outputs for the delay output or change the TTL polarity, it can be done by moving the shorting plugs according to the table below. The wire wrap pins and shorting plugs are located between and in the vicinity of U58 (U63) and U59 (U64).

LOGIC	OUTPUT	CONNECTIONS
ECL	GATE	B-C *
ECL	DELAY	B-E
-TTL	GATE	Z-A, Y-C, S-W, T-V *
-TTL	DELAY	Z-D, Y-E, S-W, T-V
+TTL	GATE	Z-A, Y-C, S-V, T-W
+TTL	DELAY	Z-D, Y-E, S-V, T-W

* Connections made at factory (see Figure 1).

3 INSTALLATION

INSPECTION

Upon receipt of the 2323A, it is recommended that a careful inspection be performed to insure that no damage occurred during transit.

The shipping box has been custom designed for this unit and should be saved should shipping be necessary. After removal from the box, the unit should be examined for physical damage to the body and front panel. Actuate the switches without power to assure physical integrity.

INSTRUMENT CHECK-OUT

Place unit in a CAMAC crate. Switch power on and flip CAMAC switch off.

Push the CHAN switch to A and observe that the A indicator is on. Repeat for Channel B.

Hold the CHAN switch at A and push and hold the UP switch. The display advances at about 2 Hz for the first eight counts and then changes to a faster rate. Push and hold down the DOWN switch and observe that the display counts down at the same rate as above.

Repeat for Channel B.

Note that all decimal points are lit for values from 0 to 63 and only one is lit for values thereafter.

Advance the range setting by pushing the RANGE switch. The decimal point and the range indicators show that the unit is advancing from .XXX μsec to X.XX sec. The next two increments are the Latched mode, during which the display blanks and the L indicator comes on.

Advance the delay width setting by pushing the DELAY WIDTH switch. The delay width indicators advance in the following order: 10, 30 100, 300 nsec.

Note that when the CHAN switch in the off position, the UP, DOWN, RANGE, and DELAY WIDTH switches have no effect.

4 OPERATING INSTRUCTIONS

MANUAL OPERATION

With the CAMAC switch off, the 2323A responds only to the front-panel switches and inputs. Any Gate duration and Delay width can be programmed manually into the 2323A and can be manually changed only.

After setting all values, set the trigger threshold for the START signal, select the positive and negative-going edge with the TRIGGER switch, and apply the START signal to generate an output. Since the factory presets the trigger threshold to −400 ±50 mV, a NIM pulse makes a convenient START signal. In this case, one of the two START inputs should be terminated in 50 Ω unless daisy chaining is desired.

It is possible to generate one output pulse (or a train of output pulses) without a START signal by flipping the TRIGGER switch.

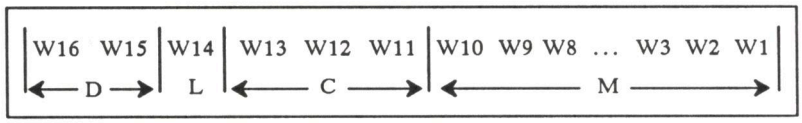
CAMAC OPERATION

With the CAMAC switch on, the 2323A responds to the CAMAC commands listed below. The unit responds to the front-panel switches, but anything programmed in manually will be overwritten immediately should a CAMAC WRITE command be executed. The unit also will respond to the front-panel inputs in this mode.

CAMAC COMMANDS

F(1)•A(0) - READ CHANNEL A PROGRAMMING WORD
F(1)•A(1) - READ CHANNEL B PROGRAMMING WORD
F(9)•A(0) - STOP CHANNEL A OUTPUT
F(9)•A(1) - STOP CHANNEL B OUTPUT
F(17)•A(0) - WRITE CHANNEL A PROGRAMMING WORD
F(17)•A(1) - WRITE CHANNEL B PROGRAMMING WORD
F(25)•A(0) - START CHANNEL A OUTPUT
F(25)•A(1) - START CHANNEL B OUTPUT
C or Z - STOP CHANNELS A AND B OUTPUTS

The CAMAC programming word is 16 bits wide and is divided up into four segments.



The first 10 bits, W1 - W10, are the mantissa (M). This number, seen in the 3-12/3 digit display, ranges from 0 to 1023.

The next 3 bits, W11 - W13, are the characteristic (C). It sets the order of magnitude of the gate duration.

The next bit, W14, is the latch bit (L). When L=0, the gate duration equals $M \cdot 10^C$ nsec. Settings of M below 100 will result in somewhat reduced accuracy and stability. When L=1, the gate duration equals the time between STOP and START.

The next 2 bits, W15 – W16, determine the delay width (D).

D	WIDTH
00	10 nsec
01	30 nsec
10	100 nsec
11	300 nsec

The CAMAC START and STOP commands perform the same function as the external START and STOP inputs.

The CAMAC C or Z commands shut down both outputs simultaneously.

NOTE: In the CAMAC mode, the TRIGGER switches and the threshold pots have no effect.

BATTERY BACK–UP

The Model 2323A has a battery backed up circuit which stores the settings of the mode, gate duration and delay width for the two channels in case of power down. The retention time is in excess of one year.

It is possible that the display will be blank after power up. In order to read the settings, you must first address the channel manually or via CAMAC.

The battery back–up is provided only for the Model 2323A, not for the earlier version 2323.

5 THEORY OF OPERATION

INTRODUCTION

The Model 2323A consists of two identical wide-range timers in a #2 CAMAC module. There are three sections to the 2323A. The first section is the gate generator (two identical gate generators). The second section is the CAMAC decoders and buffers. The third and final section provides all manual controls. The gate and the CAMAC sections are on the main pc board and the manual controls are located on the auxiliary board.

GATE GENERATOR START CIRCUITRY

The START signal is detected by a 685 comparator. The bias input is supplied by a multi-turn potentiometer (test point provided). The input range is at least ± 3 V. The outputs of the 685 are OR'd with the TRIGGER switch. This disables one of the two 685 outputs by holding it high and is used to select the positive or the negative edge. The two outputs are differentiated and used as two of the three inputs to the OR gate (U57). The third input is the CAMAC trigger, F(25). A bias voltage is applied to the latch enable input, input 6, of the 685 to provide about 50 mV of hysteresis.

The output of the start circuit is used to preset the busy flip flop. The reset of the busy flip flop is an emitter OR of the STOP pulse from the STOP level shifter and the interrupt signal from the CAMAC section (F(9) or C or Z). The clock input comes from the timing circuitry.

The Q output of the busy flip flop is OR'd with the output of the OR level shifter. The OR of these two signals is AND'd with the output of the BLANK level shifter. The output of this gate is the input to the NIM and -NIM drivers. The Q output of the busy flip flop is used to trigger the Delay Pulse single shot. The output of the single shot is translated to a NIM level signal by Q24 and Q25. TTL and ECL drivers are triggered by either signal, depending upon the options selected. TTL polarity is determined by which transistor (Q28 and Q27) drives the gate of the FET (Q26).

The Q output of the busy flip flop also goes to the busy LED driver. This is a two-stage pulse-stretcher designed to stretch a pulse of 50 nsec to a pulse wide enough to provide visible LED flash. For wider pulses the LED will appear to stay on.

The basic operation of the timing circuit in the fastest range is to switch the amount of current supplied to a capacitor so that it first charges to a programmed DAC voltage and then discharges to its starting condition (0 V). This constitutes one complete ramp cycle. The signal that comes at the end of each ramp cycle is used as a clock by a seven stage decade counter. A

multiplexer is used to select the output from the proper stage to give either 1, 10, 100, etc., ramp cycles before turning off the busy flip flop.

Transistors Q18, Q19, and Q20 form two 7 mA current sinks. One is connected to a current switch (Q22 and Q23); the other is connected to the current mirror consisting of transistors Q6, Q7, Q8, and Q9. This current mirror also divides the input current by two. The result of switching the 7 mA current sink and not the 3.5 mA current source onto the ramp capacitor is to alternately charge and then discharge the ramp capacitor. The ramp switch is controlled by the ramp flip flop. The common base stage Q21 is intended to provide an optimum load impedance for the current switch Q23–Q22 and to isolate the switching device U59 from the ramp capacitor. The upper limit of the ramp is determined by the detector formed by transistors Q11, Q12, and Q13.

When the ramp goes more positive than the voltage on the Q13 emitter, Q12 turns on and presents an ECL "1" TO U52. This signal, called High Trip, presets the ramp flip flop and turns the current sink onto the ramp, causing it to ramp down.

The lower limit of the ramp is determined by the detector formed by transistors Q15, Q16 and Q17. These transistors form a differential amplifier with one input tied to the DAC reference ground. The collector of the opposite transistor is tied to its base which allows current to be switched into the ramp to satisfy the current sink. This stops the ramp from going down below ground. The signal developed at Q15 collector is the Low Trip signal. The Low Trip signal is gated with the Off signal to reset the ramp flip flop which causes the ramp to start going high again.

The Low Trip signal is also AND'd with the counter stop signal to provide a clock to the busy flip flop to turn it off. The Q output, called Off, is OR'd with the High Trip signal to preset the ramp flip flop. The Off and Low Trip signals are translated to a TTL level and used as the clock to the scalers for the longer time ranges.

The counter is a seven–stage decade counter with the terminal count output of each stage tied to a multiplexer. The multiplexer is controlled by the range select information stored in the status register for that channel. In the 1.0 μsec full scale range (range 0) the multiplexer always presents a low at U45 pin 6 which generates a counter–stop signal. In the latch range (range 8) the multiplexer always presents a high a U45 pin 6 and no counter stop is ever generated. For all other ranges, the counter stop signal is generated during the final ramp cycle.

The upper ramp limit, and therefore the ramp cycle time, is determined by a 10-bit DAC. The DAC is programmed by the lower 10 bits of the status word, B0 to B9. A potentiometer for trimming the input voltage to the reference input of the DAC is used for gain adjustment. Another potentiometer is used to provide an offset adjustment by providing extra current to U18, an operational amplifier used as a summing amplifier.

The delay pulse width monostable is composed of a programmable current source (U15, Q67, Q68, Q69), a current switch (Q1 and Q2), ramp circuitry (Q3 and Q4), a comparator (U56), and gates (U57). At the trailing edge of the gate pulse, the current switch is turned off and the programmed current source is allowed to charge up the ramp capacitor. The comparator switches when the ramp gets above a predetermined level. If the comparator has not switched yet and the busy flip flop is still off, the 2323A will generate a delay pulse. (Note that the delay pulse will terminate as soon as the 2323A is retriggered. This will prevent the delay width pulses from overlapping).

CAMAC

The CAMAC decoding is primarily done by gates U11-1, U4, U9-11 and U9-6, and the decoder U1. The S2 pulse is differentiated and AND'd with the interrupt (F(9) or C or Z) and trigger (F(25)) decodes. The Write decodes (F(17)) are AND'd with S1. The Read decodes (F(1)) are OR'd to provide the Read signal which enables the output gates, U7, U8, U12 and U13. The Write decodes are also OR'd to provide a signal (WE) to enable the W line buffers, U5 an U6, and to disable the Channel A and b status registers. Two signals (X AND S1) and A(1) are passed to the manual control board to load the status register with the contents of the channel status register that is being addressed by CAMAC. Gates U2-6 and U2-11 are used to OR the channel display select information from the CAMAC section with the information from the manual control board. Gates U17-13 and U17-1 are used to OR the Write signals from the CAMAC section with the write signals from the manual control board.

MANUAL CONTROLS

Note: Component designations used in the following description refer to the manual control board, except as noted.

The Channel Select and Enable switch is tied directly to the preset and reset inputs of the channel flip flop (U24). The switch also is connected to gate U18-3 which serves as an OR gate and generates the manual override signal (MO). This signal is delayed through inverters U10-8 and U10-10 to

generate the manual enable signal (ME). The output of gate U18-6 is a pulse just before the leading edge of the manual enable signal. When a channel is selected with the switch, the pulse from U18-6 is used to select and enable one channel's status register. This is done with the manual display signals MDA and MDB. The trailing edge of the pulse is used to load the display status register (LOAD signal). The manual enable signal (ME) is then used to output the display status register to the channel status registers. The manual ENABLE signal is then AND'd with the clock from U-12 to provide a manual write signal (either MWA or MWB). This manual write signal constantly updates the selected channel's status registers with the contents of the display status register. Any changes made manually are then transferred immediately to the channel status register. The outputs of U24 are also buffered and used to drive the channel lights.

Debouncing of the range and delay width switches is accomplished with the circuitry associated with U8. The pulses output from these comparators are used to increment the range counter and the delay width counter.

The display clock generator provides both a two-speed clock to the time up/down counter and the address lines to the digit select decoder. Before the up or down buttons are pushed, U1 and U2 are held reset. When one of the buttons is pushed, the counter is enabled and every time U2 generates a carry-out signal one clock pulse from U11-11 is gated to the time up/down counter. The carry-out signal from U2 also allows U1 to increment. When U1 reaches a count of 8, and U2 generates a carry-out, the P enable inputs of U1 and U2 are disabled. This allows all the clock pulses from U11-11 to be sent to the time up/down counter. The two speeds are approximately 2 Hz and 32 Hz.

The display status register consists of the time up/down counter (U5, U6 and U7), the range counter (U4), the delay width counter (U3) and the display register tristate buffers (U13 and U15). The time up/down counter and the delay width counter are binary counters and the range counter is a decimal counter. Counts 8 and 9 are used for the latch mode.

The binary information in the mantissa up/down counter is supplied to the binary to BCD converter (U20, 721, 22, U29, U30, and U31). The BCD output is passed to U27 and U28 which serve as a digit multiplexer. The multiplexer output is the input of U25, a BCD to 7-segment decoder which drives the segments of the digital display. The digit select lines decode the display address and use this information to drive the digits of

the digit display (through the buffers of U35). The decoded digit information is also used to control the digit multiplexer and to provide the inputs to the decimal point decoder (U33). The most significant digit signal (MSD) is used to blank the leading digit if it is a zero. The latch signal, CRA3, is used to blank the display in the latch mode. The four most significant bits of the mantissa, CB6–9, are combined to provide an input to the decimal point driver that causes all of the decimal point segments to light if the mantissa is below 64. (This is a warning to the user to change to the next range down if possible).

A programmable Read Only Memory is used to decode the range information and the delay width information and also drive the LED's.

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