OPERATOR'S MANUAL

MODEL 2373

16 IN x 16 OUT CAMAC

MEMORY LOOKUP UNIT

16 x 16 MLU

September 16, 1992

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CAUTION

COOLING

The high power dissipation of the 2373 requires that it be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50 deg. C.

6 VOLT POWER REQUIREMENT AND THE Y1 BUS

CAMAC specifications require that no more than 3 Amp be drawn from any contact on the DATAWAY. The Model 2373 requires more than 3 Amp of -6 Volt to operate because of its speed and large memory. CAMAC specifications allow for this by providing the Y1 pin. The Model 2373 will not operate unless -6 Volt is provided on the Y1 pin. This can be accomplished by either connecting the Y1 bus to the -6 Volt bus on the back of the DATAWAY or by providing another -6 Volt supply for the Y1 bus.

INSTALLATION

Crate power should be turned off during insertion or removal of modules to avoid possible damage caused by momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instructions regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other material that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental or consequential damages, whether in contract or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration and use of LeCroy equipment are available from the Research Systems Division Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499 (914) 578-6030 or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support service. For example, Blue Ribbon service provides guaranteed three-day turn around on repairs, a direct access number for product application assistance, yearly calibration and the addition of engineering improvements. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purpose of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates in the most up-to-date circuitry.

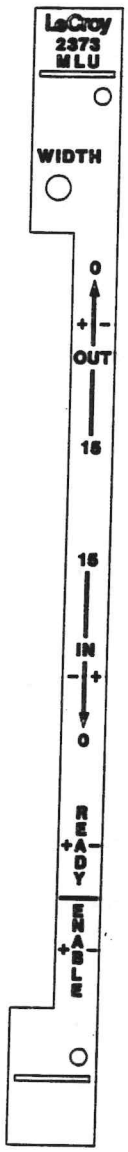
SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SECTION 2 PRODUCT DESCRIPTION

SECTION 2.1 INTRODUCTION



The Model 2373 is a 1024 K-bit dual-ported random access memory based on the LeCroy Model 2372 but with 16 times the memory thereby allowing the 16 bit input address word to generate a 16 bit output word. Packaged in a single-width CAMAC module, the Memory Lookup Module (MLU) has a 45 nsec cycle time making it a very desirable module for complex functions required of trigger logic or high speed data processing.

In normal use, the MLU is first downloaded with the required trigger data and then verified via CAMAC. This information, which defines the function of the MLU, is accessed via the two 16 bit front panel Data-In and Data-Out connectors for real time applications.

The function of the MLU is user defined to meet the application. Virtually any function may be defined: angle logic or clusterized track multiplicity are examples of complex trigger functions. When used as a trigger processor element, the MLU may be used for any operation which is a one-to-one mapping. In conjunction with an ADC, the MLU can be loaded with the calibration to energy. The MLU can also be loaded with a digital comparator function or any arithmetic calculation, e.g. summing, division, sin function, etc.

The Model 2373 has four software selectable operating modes. The Strobed Mode is the most commonly used mode. In this mode, the MLU is strobed by the ECL Input Enable signals coming from previous logic unit(s). After 45 nsec, the output "word" of the MLU becomes valid along with the four ECL Output Ready signals which may be used to strobe the output word into other ECLine type modules. The output word remains static until another Input Enable is received. Four Input Enables are provided with an Enable condition being defined as their coincidence (unused inputs are set to logical 1). This allows modules of this type to be interconnected and operate asynchronously (the slowest element controls the speed). A second mode is the Transparent Mode where the Model 2373 operates at maximum speed. This mode bypasses the latch circuitry and thus provides a slight speed advantage, offering a throughput time of only 40 nsec. A third mode is the Pulsed Mode. This mode is used when it is desirable to scale (count) any or all of the outputs. It insures that one and only one pulse appears at any of the 16 outputs, provided that the output bit is true for the given Input Word, when the Input Enable is made true. A forth mode allows the Model 2373 to operate identically to a Model 2372. The reason for this mode is to allow customers who have a large investment in the Model 2372 to add to their system without software changes. The Model 2373 has replaced the Model 2372 in the LeCroy product line.

SECTION 2.2 SPECIFICATIONS

INPUTS:

Input Word: One 16-bit ECL input on front panel 34-pin header with 100 ohm input impedance. Maximum rate: 22 MHz.

Enable: Four AND'd complimentary ECL pairs on front-panel header into 100 ohm impedance. Unused inputs are logically true. Required only in Strobe or Pulse Mode where Input Word is latched on leading edge of Enable pulse (coincidence of Enable Inputs being used).

OUTPUTS:

Output Word: One 16-bit complimentary ECL output from a front-panel 34-pin header. In the Strobe or Pulse mode, the content of memory address given by the Input Word is presented 40 nsec after Input Enable. In the Transparent mode, the content of the addressed memory is presented 40 nsec after the Input Word.

Output Ready: Four complimentary ECL pairs from a front-panel header. Provides Output Ready level for down-stream logic indicating a valid Output Word.

OPERATING MODES:

Operating modes are set by CAMAC commands.

TRANSPARENT: Latching is disabled. Output follows changing input with minimum propagation delay (40 nsec).

STROBE: Input Word latched on leading edge of AND of Input Enables. Ready appears 45 nsec after Enable.

PULSE: Same as Strobe Mode except that all true output bits go false after a delay which is adjustable (20-150 nsec) via a front-panel potentiometer. The purpose of this mode is to allow the scaling of individual bits the Output Word.

INHIBIT: Disables front-panel inputs. (Used for programming memory contents via computer.)

Memory Configuration: Four 64k 4-bit Static RAMs make up the internal memory allowing 16-bit x 16-bit operation. It also can be configured to operate as a replacement for the Model 2372 with little or no programing changes required (see both Model 2372 and Model 2373 Owner's Manual). The memory in the Model 2373 has no battery back up like the Model 2372 and MUST be reloaded upon loss of power.

Computer Control: Read and Write Control Register (setting Mode and Dimensionality); Read and Write Address Register; Read or Write data at address in Address Register; Read front panel input word or the output generated by front-panel input.

PROPAGATION DELAY:

In the Strobe and Pulse mode, propagation delay is defined as the time between the leading edge (trailing edge for "OR" condition) of the Input Enable signals at the front panel and the leading edge of the Output Ready signals. This is factory adjusted to 45 nsec. The Output Word settles at least 5 nsec before a true Ready condition, thus allowing for proper set up time at the inputs to successive stages of Programmable Data Handler Modules.

In the Transparent mode, propagation delay is defined as the time between the leading edge of the Input Word at the front panel and the leading edge of the Output Word. This time is solely a function of the SRAMs and is at most 40 nsec.

GENERAL:

Maximum Rate: Transparent Mode - 25 MHz.
All Other Modes - 22.2 MHz.

Power Requirements: +6 V at .7 A; -6 V at 2.3 A; -6 V (via Y1 pin) at .8 A.
NOTE: -6 V is required on the Y1 pin to operate. (See CAMAC pin allocation specifications.)

SECTION 2.3 CONTROL AND CONNECTORS

INPUTS: The "IN" port consists of 16 ECL complimentary inputs via a 17-pair header, with pin out matching the LeCroy ECLine standard. Input impedance is 100 ohm +/- 5% and can be made high impedance by simply removing the four, 8-pin, 100 ohm resistor networks in the strip sockets located directly behind the connector. In the Strobe and Pulse mode, this word is latched by the coincidence of the Input Enable signals (see below) and must arrive at least 2 nsec before this coincidence. The minimum pulse width is 10 nsec. In the Transparent mode, the Input Word is not latched and hence must remain as long as one wishes the output to remain valid. The minimum pulse width in this case is 50 nsec.

The "ENABLE" inputs consist of four ECL complimentary inputs via four 2-pin headers. Input impedance is 100 ohms +/- 5% and can be made high impedance by simply removing the 8-pin, 100 ohm resistor network in the strip socket located directly behind the connector. The "AND" of these inputs defines the Enable condition. The leading edge of this condition latches the Input Word (only in the Strobe or Pulse mode) and triggers the one-shot circuit which produces the Output Ready signals (see below). Unused inputs are forced to a logical "1", satisfying the "AND" condition. In the Strobe or Pulse mode, these inputs must arrive at least 2 nsec after the Input Word and must be at least 10 nsec wide. In the Transparent mode, no Enable condition is necessary.

By switching the polarity of the Input Enable signals (flipping the twisted-pair connector housing) the Enable condition becomes the "OR" of these inputs. In this condition, however, the trailing edge latches the Input Word and triggers the one-shot.

OUTPUTS: The "OUT" port consists of 16 ECL complimentary outputs via a 17-pair header, with pin out matching the LeCroy ECLine standard. The 16 bit Output Word is the contents of the memory location addressed by the Input Word.

In the Strobe and Pulse mode, this word becomes valid at least 5 nsec before the Output Ready signals. In the Strobe mode, the Output Word remains valid until after the next Input Word is latched. In the Pulse mode, the true bits of the Output Word remain true only for the time period set by the Front Panel "WIDTH" potentiometer and then go false. This width is adjustable from 20 nsec to 150 nsec. In the Transparent mode, this word becomes valid within 40 nsec after the Input Word and emains valid for as long as the Input Word is present.

The "READY" outputs consist of ECL complimentary outputs via four 2-pin headers. The Output Ready signals in the Strobed or Pulsed mode, go false 20 nsec after receipt of Input Enable and go true again 25 nsec later (total cycle time of 45 nsec). The leading edge of this true condition defines a valid Output Word and can be used as an Input Enable for successive stages of Programmable Data Handler Modules. The Output Ready signals appear at least 5 nsec after the Output Word has become valid. In the Transparent mode, the Output Ready goes true approximately 45 nsec after receipt of Input Enable and false approximately 5 nsec after the tailing edge of the Input Enable.

SECTION 2.4 CAMAC CONTROL

The CAMAC controls for the 2373 conform to the CAMAC Standard IEEE Std 583-1975. If the user is unfamiliar with the CAMAC standard, a good reference is "CAMAC Instrumentation and Interface Standards". It is published by:

The Institute of Electrical and Electronics Engineers, Inc.,
345 East 47th Street,
New York, NY 10017.

Further information is available from LeCroy Corporation in the form of Application Notes.In particular, AN-33, "Introduction to CAMAC", is very useful.

Please note that at power-on, the 2373 will NOT respond to any CAMAC commands for one second because of automatic programing of the Programmable Logic Array,

F(0)A(0): Read 16-bit Output Word addressed by CAMAC Address Register (CAR). CAR increments on S2. Inhibit Mode must be set.

F(0)A(1): In Inhibit Mode, reads 16-bit CAR address. If NOT in Inhibit Mode, reads 16-bit front panel Input Word.

F(0)A(2); Read 7-bit CCR word. The Model 2372 has only a 5-bit CCR. The two added bits are for Pulse Mode and 2373 Mode (16-bit Input with 16-bit Output). See Owner's Manual.

F(0)A(3): Read 16-bit Output Word whose address is either the latched Input Word (Strobe or Pulse Mode), CAR (Inhibit Mode) or unlatched Input Word (Transparent Mode).

F(0)A(4): Same as F(0).A(1) so as to be compatible with Model 2372.

F(16)A(0): Write 16-bit word into memory location addressed by CAR. Requires operation in Inhibit Mode.

F(16)A(1): Write 16-bit CAR address. Data word at ECL output will change accordingly. Requires operation in Inhibit Mode.

F(16)A(2): Write 7-bit CCR word which sets the Mode of operation. There are five Modes: Strobe, Transparent, Inhibit, Pulse and 2372.

Z: Reprograms the programmable logic array which takes about a second. The module will NOT respond to any CAMAC commands during this interval.

Q: A Q=1 response is generated for F(16)A(0) and F(0)A(0). A Q=0 response is generated for these commands when CAR reaches terminal count. This Q response is valid only when CAR has been loaded via F(16)A(1) after power up.

X: An X=1 response is generated for any valid N.F.A.

SECTION 3 INSTALLATION

SECTION 3.1 GENERAL

The 2373 is a CAMAC module and as such must be installed in a CAMAC crate. Care must be taken to ensure the crate power is off before the module is installed. It can be installed in any slot except in the crate controller position (slots 24 and 25).

CAMAC specifications require that no more than 3 Amp be drawn from any contact on the DATAWAY. The Model 2373 requires more than 3 Amp of -6 Volt to operate because of its speed and large memory. CAMAC specifications allow for this by providing the Y1 pin. The Model 2373 will not operate unless -6 Volt is provided on the Y1 pin. This can be accomplished by either connecting the Y1 bus to the -6 Volt bus on the back of the DATAWAY or by providing another -6 Volt supply for the Y1 bus.

SECTION 3.2 CABLES

Once the unit is installed in the crate, the front panel Input and Output connectors must be connected to cables. These cables can be purchased directly from LeCroy Corp. as Model DC2/34-L (L = length in feet) or can be made by user. Application Note AN-49 provides manufacturers and part numbers. To complete the cable connections of the 2373, Enable and Ready should be connected if required.

SECTION 4 OPERATING INSTRUCTIONS

SECTION 4.1 CAMAC COMMANDS

Note that the Model 2373 can be a replacement for the Model 2372 and will respond to all the CAMAC commands required by the Model 2372. See 2.2 CAMAC Control Register (CCR) and Model 2372 Owner's Manual.

The Model 2373 generates an X=1 response for each of the following Read commands:

F(0)A(0) Read 16-bit Output Word addressed by CAMAC Address Register (CAR) and increment CAR. This command functions properly only when the front panel Input Word is disabled, i.e., the Inhibit mode.

F(0)A(1) Read 16-bit CAR when the Inhibit mode is activated. Read front panel Input Word when Inhibit is deactivated and either Strobed, Pulsed or Transparent mode is activated.

F(0)A(2) Read 7-bit CCR.

F(0)A(3) Read 16-bit Output Word whose address is either the latched Input Word (Strobe or Pulse Mode), CAR (Inhibit Mode) or unlatched Input Word (Transparent Mode).

F(0)A(4) Same as F(0).A(1). (To be compatible with Model 2372.)

The Model 2373 generates an X=1 response for each of the following Write commands.

F(16)A(0) Write 16-bit word into memory location addressed by CAR and increment CAR. The Inhibit mode must be activated.

F(16)A(1) Write 16-bit CAR. The Inhibit mode must be activated.

F(16)A(2) Write 7-bit CCR.

A Q=1 response is generated for each F(0)A(0) and F(16)A(0), until the CAR has reached terminal count, at which point Q=0. This is the Stop on Word mode Q response for block transfers as described in the CAMAC Instrumentation and Interface Standards (IEEE Standard 583-1975). The CAR must be loaded with the desired starting address first. See the Model 2372 Owner's Manual when using the Model 2373 in the Model 2372 mode.

A Z command reprograms the Programmable Logic Array. The reprogramming takes no more than one second during which the Model 2373 will not respond to any commands. A power up also causes a reprogramming of the Programmable Logic Array. Loss of power causes the memory contents to be lost.

SECTION 4.2 CAMAC CONTROL REGISTER (CCR)

The 7 bits of the CCR are organized in the following manner:

CAMAC Read/Write Lines:

R/W7 R/W6 R/W5 R/W4 R/W3 R/W2 R/W1
M D

D = Dimensionality

These 3 bits determine the Input and Output Word sizes when operating in the Model 2372 mode (see Mode below). A detailed explanation of these bits is in the Model 2372 Owner's Manual and will not be covered here. These bits are ignored in the Model 2373 mode.

M = Mode

These 4 bits determine which part of the circuit drives the address bus and how the Output Word is generated.

R/W4 = 0 The STROBE mode.

Input latches receive the Input Word and drive the address bus. Output Word latched until after next Input Enable.

R/W4 = 1 The TRANSPARENT mode.

Input buffers (without latches) receive the Input Word and drive the address buss. Output Word latch is transparent.

R/W5 = 1 The INHIBIT mode.

The CAR receives an Input Word from CAMAC and drives the address bus. The front panel latches and buffers are disabled. Used for writing to and reading the memory and the CAR. (Over rides condition of R/W4.)

R/W6 = 1 The PULSE mode.

Same as the Strobe mode except that true bits of the Output Word go false after the Width interval.

R/W7 = 0 The Model 2372 mode.

The Model 2373 responds to all the Model 2372 CAMAC commands. See Model 2372 Owner's Manual.

R/W7 = 1 The Model 2373 mode.

The Model 2373 is a 16 x 16 MLU. The CAR is a 16 bit address register and the memory excepts and generates 16 bit Output Words.

NOTE: Jumper P4 can be used to force the Model 2372 mode. When in place, it causes both R/W6 and R/W7 to equal "0".

SECTION 4.3 CAMAC ADDRESS REGISTER (CAR)

This is a 16-bit register that drives the address bus only in the Inhibit mode.

All 16 bits are active in the Model 2373 mode and are accessed via R/W1. . . . . R/W16. When operated in the Model 2372 mode, the number of active bits depends on the Dimensionality setting (see Model 2372 Owner's Manual).

SECTION 4.4 PROGRAMMING THE MEMORY

The first step in programming the memory in the Model 2373 mode involves loading the CCR (F(16)A(2)) with binary number 1010000. This sets the Inhibit and Model 2373 mode. The loading can be verified by doing a read of CCR (F(0)A(2)). Next load CAR (F(16)A(1)) with the starting address (normally all zeros). The loading can be verified by doing a read of CAR (F(0)A(1)). The memory can now be loaded by doing a F(16)A(0) until loss of Q and verified by doing a read (F(0)A(0)) until loss of Q.

Programming the memory in the Model 2372 mode is much more complex. The Model 2372 Owner's Manual describes the correct procedure in detail.

SECTION 5 THEORY OF OPERATION

SECTION 5.1 INTRODUCTION

The circuitry of the Model 2373 can be divided into two sections. The first section is the high speed circuitry, consisting of the front panel inputs and outputs, the input latches and buffers, the RAMs and output multiplexers, and the Enable-Ready one-shot. The second section is the CAMAC control, consisting of the CAR, the CCR, the read multiplexers and the command decoding.

SECTION 5.2 HIGH SPEED CIRCUITRY

5.2.1 Input Word to Output Word

The ECL differential signals comprising the IW, arriving at the front panel via the 17 twisted pair cable, are terminated in 100 ohm (or high impedance if the 100 ohm SIPS are removed). The 10E116 input receivers (U5, U6, U7 and U8) invert the incoming signals to yield a low active internal signal level. Floating inputs represent a "0" level. In the Inhibit mode, the 10E155 2:1 multi-plexers with latch (U12, U13 and U14) select the internal address from the 10KHT5578 CAR latches (U32 and U38). Otherwise, the IW is selected. In the Strobe and Pulse mode, IW is latched at the leading edge on Input Enable. Otherwise, the latches are in the Transparent mode. The latched outputs are converted to TTL by 10H125 translators (U20, U21, U22, U23 and U24) and drive the address bus of four CY7C191 64k*4-bit SRAMs (U31, U37, U4 and U43) which provide a maximum of 16 input and 16 output memory lookup capacity. The outputs are converted back to ECL signals M0-M15 by 10H124 translators (U30, U36, U39 and U42) and go to the output multiplexer, which consists of U27, U34 (10E163); and U17, U18, U19 (10E155).

In the 2373 mode, the output multiplexer passes along the 16 bit data word addressed by IA0-IA15 to the four 10101 output drivers (U1, U2, U3 and U4). This is because, when pin 12 of U29 is high (2373 mode), pin 14 of U35 is also high (-0.9V). However, R25 level shifts this signal to -1.3V which is connected to the inverting inputs of U21 and thereby make the 4 MSBs IA12-IA15 active. In the 2372 mode, pin 14 of U35 is low making the level at the inverting inputs of U21 about -2.2V thereby causing the outputs of U21 high and forcing the 4 MSBs (IA12-IA15) to be always "1". The 4 MSBs of address from U20 (IA12P-IA15P) go to dimension control logic U29 (16L8B2). Together with the dimension control bits DM0, DM1 and DM2 derived from the 3 LSBs of CCR, this logic generates the output multiplexer control signals A, B, C and D.

For dimensionality of:

D=0 (1 OW bit)	DCBA =	IA15P	IA14P	IA13P	IA12P
D=1 (2 OW bits)	DCBA =	IA14P	IA13P	IA12P	0
D=2 (4 OW bits)	DCBA =	IA13P	IA12P	0	0
D=3 (8 OW bits)	DCBA =	IA12P	0	0	0
D=4 (16 OW bits)	DCBA =	0	0	0	0

The value of D (dimensionality) is decoded directly from the three LSBs of CCR. Any value >4 is handled as D=4

The output multiplexer determines (using the selector bits) to which of the lower 8 bits of the OW a given bit of the data bus is directed. Their outputs OW0-OW7 drive the two 10101 output drivers (U1 and U2) which produce the lower 8 bits of OW. Only in D=4 are the upper 8 bits OW8-OW15 enabled by OEC on pin 12 of U3 and U4.

For dimensionality D=0, only OW0 is active (all other bits are disabled by OE1, OE2, OEB and OEC which in turn are enabled by the selected dimensionality).

D C B A	OW0
0 0 0 0	M0
0 0 0 1	M1
0 0 1 0	M2
.	.
.	.
.	.
1 1 1 1	M15

For D=1, OW0 and OW1 are active.

D C B A	OW1	OW0
0 0 0 0	M1	M0
0 0 1 0	M3	M2
0 1 0 0	M5	M4
.	.	.
.	.	.
1 1 1 0	M15	M14

For D=2, OW0, OW1, OW2 and OW3 are active.

D C B A	OW3	OW2	OW1	OW0
0 0 0 0	M3	M2	M1	M0
0 1 0 0	M7	M6	M5	M4
1 0 0 0	M11	M10	M9	M8
1 1 0 0	M15	M14	M13	M12

For D=3, OW0 to OW7 are active.

D C B A	OW7 OW6 . . . . . OW0
0 0 0 0	M7 M6 . . . . . M0
1 0 0 0	M15 M14 . . . . . M8

For D=4, all bits are active. This is the same configuration as the 2373 mode.

D C B A	OW15 . . . . OW8	OW7 . . . . OW0
0 0 0 0	M15 . . . . M8	M7 . . . . M0

In the Strobe mode, the output latch (U17, U18 and U19) is updated only when the memory output has settled to guarantee glitch free operation. In the Pulse mode, the output latch is latched when the output (U1, U2 and U3) is enabled and transparent after the output is disabled. This prevents glitching in the Pulse mode. In the Transparent mode, the output latch is always transparent.

5.2.2 Input Enable to Output Ready

The ECL differential signals comprising the Input Enables (IE), arriving at the front panel via individual twisted pair cables, are each terminated in 100 ohms (or high impedance if the 100 ohm sip (U63) is removed). The signals are received by 10E116 line receiver (U8) and logically AND'd by U16C (10E101). Floating inputs represent a "1" input. Note that if the IE signal polarity is switched by flipping the cables, a wired OR output results, whose trailing (falling) edge produces the enable condition.

The input latches have two latch enables (ILEN1 and ILEN2). In the Inhibit or Transparent mode, both signals are low (U16B and U16D) and the latches are transparent. In the Strode and Pulse mode, ILEN1 is the inversion of IE and ILEN2 is ILEN1 inverted and delayed. When IE goes high, ILEN1 goes low (ILEN2 is already low) and IW goes through the latch. ILEN2 then goes high after ILEN1 propagates through U16D and latches IW. The output of U16C also triggers the delay circuit comprised of flip-flop U26B, current source Q1 and Schmidt trigger U33B. Its output resets the ready flip-flop U26A by clocking it (in the Transparent mode, U26A is reset by U16A immediately after Input Enable goes low) and triggers the next delay circuit similarly comprised of U26D, Q4 and U33E. The output of U33E is delayed by U33C and Q2 and it sets the ready flip-flop U26A high. The ready flip-flop enables U15 (10101) which provides the front panel Output Ready.

The output latch enable (OLEN) and the output enables (OEA, OEB and OEC) are provided by U9B, U9C, U9D and U9E respectively.

In the Transparent or Inhibit mode, if U26C is "1", U33D and U41B will eventually reset U26C to "0" and once there, the path of U25C, U41C and U41B will keep U26C at "0". This makes OLEN low and the output latch transparent. Assuming D=4, OEA, OEB and OEC will be low and the output always enabled. If an Input Enable occurs, U26C will be triggered by U33B and give only a short Q output because its reset is on via U25A, U25C, U41C and U41B. OLEN goes high latching the OW but then goes low making the latch transparent again.

In the Pulse mode, the output latches are normally transparent and the output drivers disabled. When Q of U26C goes high, OLEN goes high latching OW followed by OEA, OEB and OEC (U9A provides a delay) going high enabling the output drivers. When Q of U26C goes low, it f first disables the output drivers by making OEA, OEB, and OEC low and then OLEN goes low delayed by inverted OEA thru U25B to U9B. Because the output of U41C is forced low by PLSTTL via U45, U26C can only be reset by U33D or U33B, which ever comes first. Normally it is reset by U33D and the time delay adjusted by R32 (front panel potentiometer) determines the output pulse width. If the next Input Enable occurs before the time delay is completed, U33B will reset U26C ensuring only one output pulse for every Input Enable.

In the Strobe and Pulse mode, R33 controls the time delay (adjusted to 20 nsec) between the leading edge of Input Enable and the disabling of Output Ready. R34 controls the time delay between the disabling of Output Ready and the leading edge of OLEN (adjusted so that OLEN is 35 nsec after Input Enable leading edge). R35 controls the time delay between OLEN and Output Ready enabled (adjusted so that Output Ready is enabled 45 nsec after Input Enable leading edge).

SECTION 5.3 CAMAC CIRCUITRY

Camac commands are decoded by U49 (20L8A) which generates the following signals:

WRT — CAMAC Write - active low. It gates the CAMAC write bus signals W1-W16 to internal data bus D0-D15 during S1.

RD — CAMAC Read - active low. It gates the data onto the CAMAC read bus during S1.

BA1 — Sub-Address bit 1 - active high. It combines sub-address A1 and A4 so that F(0)A(4) executes as F(0)A(1). F(0)A(4) is kept only to be compatible with the Model 2372. During configuration of the XC3020 programmable logic array, BA1 is forced low.

BA2 — Sub-Address bit 2 - active high. During configuration of the XC3020 programmable logic array, BA2 is tri-stated to avoid contention.

SS — Timing Signal. It goes low at the leading edge of S1 and high at the leading edge of S2.

ARCLK — Address Clock - active low. Clock for CAMAC Address Register (CAR) U32 and U38 (SN10KHT5578 TTL/ECL level converter with edge triggered register). For F(16)A(1), data is clocked into CAR at S1. For F(0)A(0) and F(16)A(0), the input to CAR is incremented by U44 at S2 only in the Inhibit mode.

MEMWE — Memory Write Enable - active low. This signal is for writing to the memory and occurs only with a F(16)A(0), S1 and in the Inhibit mode.

RDOW — Read Output Word - active low. This is an enable to U10 and U11 (SN10KHT5539 ECL/TTL open collector level converter) to gate OW to the internal bus D0-D15. For F(0)A(0), the bus is released at the trailing edge of S1 so that CAR can be incremented at S2.

The remaining CAMAC control logic is contained inside U44 (one sheet of the schematics shows the internal logic of U44 (XC3020) using conventional IC logic symbols). There is a seven bit CCR. CCR0, CCR1 and CCR2 control the dimensionality in the 2372 mode. To save I/O pins, they are encoded with CCR6 (2373 mode bit) into three bits DM0, DM1 and DM2. Any dimensionality >4 will be encoded as 4. If CCR6 is set, DM0, DM1 and DM2 are encoded as 7 to indicate 2373 mode. CCR3, CCR4 and CCR5 are encoded as TRSTTL, PLSTTL and INHTTL corresponding respectively to Transparent, Pulse and Inhibit modes. The Strobe mode is implied when both TRSTTL and INHTTL are false. When switching from Inhibit mode to Strobe mode, U17A (see U44 internal logic diagram) delays TRSTTL and thus guarantees the OW latched corresponds to the front panel IW. In the 2372 mode, OW is masked by OE1, OE2, OEA, OEB and OEC depending on the selected dimensionality. The XC3020 has an internal bus DB0-DB15 which is connected to the external bus D0-D15 via bidirectional bus drivers. Memory address bus IA0-IA15 is connected to DB0-DB15 via an ADD1 circuit which increments the memory address if CAMAC sub-address is 0. In the case of CAR overflow, Q response is disabled. Any read/write command will generate an X response. For the command F(0)A(0) and F(16)A(0), RD and WRT go false at the trailing edge of S1 to allow incrementing of CAR on S2. In order for the X response to be there during S2, it is latched on the leading edge of SS (same as leading edge of S1). For the same reason, R0-R15 are also latched on the leading edge of SS.

The XC3020 is a SRAM based programmable logic array. This means a power loss will cause a memory loss. An on-chip power failure detection circuit will automatically start a reconfiguration. To be on the safe side, this reconfiguration can also be initiated by a CAMAC Z command.