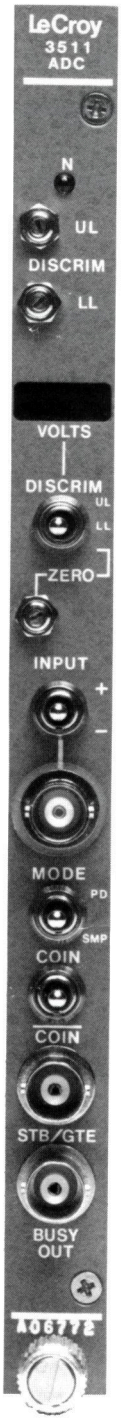
TECHNICAL DATA

LeCroy



CAMAC Model 3511

High Performance Spectroscopy ADC

- **Model 3511 combines low dead time and 5 μsec conversion time for 8K channels permitting 150 kHz throughput rate**
- **250 to 8K programmable conversion gains**
- **Directly compatible with LeCroy Model 3500M Multichannel Analyzer for complete multiple-input pulse height analysis with built-in acquisition, display, data analysis, and I/O**
- **Memory transfer time of <1 μsec/conversion with Model 3500M**
- **Peak-detect, strobed sampling and gated inputs with built-in self-strobe capability**

INTRODUCTION

LeCroy's Model 3511 is a high-speed, high resolution, ADC for gamma and x-ray spectroscopy applications offering 250 to 8000 channel conversion gains with a conversion time of 5 μsec for an 8000 channel conversion.

GENERAL DESCRIPTION

Model 3511 operates in either peak-detect mode, with coincidence or anti-coincidence gating, or strobed sample mode for sampling DC or slowly varying AC signals. Built-in self strobing permits sampling the input signal from 100 nsec to 35 μsec after triggering the lower level discriminator. Both bipolar and monopolar, positive or negative, DC-coupled inputs in the range of 0 to 8 V can be accepted with risetimes of 300 nsec to 20 μsec.

Upper and lower discriminator and zero adjust are precisely set by 22-turn potentiometers with settings read on an LED display. An ADC prompt or delayed busy output can be provided to enable successive ADC's or for external timing or control.

ZERO DEAD TIME MEASUREMENTS

With several 3511 ADC's cascaded, dead time of the analysis system can be effectively eliminated.

COMPATIBLE WITH MODEL 3500 MULTICHANNEL ANALYZER

To take full advantage of its fast conversion times, Model 3511 is directly compatible with and fully supported by LeCroy's Model 3500M Multichannel Analyzer System. Model 3500M includes firmware for programming acquisition parameters and permits direct memory access (DMA) data transfer to 8192 channels of histogramming data memory in less than 1 μsec/conversion. In the basic 3500M, up to eight 3511 modules can be directly interfaced for inputting data to Model 3500M. With sufficient data memory in Model 3500M, each ADC can be used with maximum conversion gain for maximum resolution.

Model 3511 is a high-density, single-width CAMAC module measuring only 0.7 inches by 9 inches—one-half the size of a single-width NIM module, and one-fourth to one-sixth of most NIM ADC's.

Innovators in Instrumentation

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SPECIFICATIONS
CAMAC Model 3511
HIGH PERFORMANCE SPECTROSCOPY ADC

GENERAL

Type: Model 3511 is a 13-bit (8000 channel) modified successive approximation type analog-to-digital converter.

Packaging: Single-width CAMAC module

Operating Modes: Model 3511 provides two input conversion operating modes: Peak-Detect and Sample. In the Peak-Detect (PD) mode, conversion is self-triggered upon detection of a signal peak within discriminator settings. In the Sample (SMP) mode, conversion is initiated by a strobe pulse for a signal within discriminator settings. Built-in self-strobing capability permits sampling the input 100 nsec to 35 μsec after the lower level discriminator is triggered.

CONVERSION

Conversion Gain: 250, 500, 1K, 2K, 4K, or 8K channels full scale. Programmable through CAMAC Dataway.

Conversion Time: Fixed at 5 μsec for 8K channels

Total Conversion Dead Time: ADC conversion time plus 0.3 to 20 μsec risetime, plus 0.5 to 2.0 μsec risetime compensation (selectable by internal switch in 0.5 μsec steps), plus 100-400 nsec storage offset processing time, plus 400 nsec buffer memory transfer time.

Conversion Triggering: Conversion is initiated by peak detection or a strobe pulse for an input signal within discriminator settings.

INPUT

Peak-Detect Mode: Shaped pulses, positive or negative (switch-selectable) bipolar or monopolar, 50 mV to 8 V input range. Risetime range—300 nsec to 20 μsec in five internal switch-selected ranges. Each selection optimizes peak detection response for that range of risetimes. (See Risetime Select Switch.)

Sample Mode: Positive or negative (switch-selectable) bipolar or monopolar, 0 to 8 V input range. Minimum duration—500 nsec.

Coupling: DC input

Input Impedance: 1 kΩ

Str/Gate Input: The Strobe/Gate Input serves two functions. In the Peak-Detect mode, a gate pulse enables or inhibits conversion in conjunction with the Coincidence/Anti-Coincidence switch. In the Sample mode, a strobe pulse initiates conversion of a DC signal or slowly varying AC signal. The input is both TTL and NIM compatible.

A unique feature of Model 3511 is a self-strobe capability, achieved by using the delayed busy signal output initiated by the lower level discriminator firing as the input to the Strobe/Gate Input. The Busy delay is adjustable from 100 nsec to 35 μsec for selecting the desired time after the signal exceeds the lower level discriminator for sampling.

OUTPUT

Busy Output: Signals that the 3511 is performing a conversion. The Busy Output permits cascading several ADC's to reduce overall system dead time. A Busy Output connects to the Strobe/Gate Input of the next ADC to enable it only when all of the preceding ADC's are performing a conversion. A delay (internally adjustable from 100 nsec to 35 μsec) determines the time after peak detection, or after lower

level discriminator firing when the Busy Output is present, such that only one ADC will convert any given pulse. An internal jumper permits selecting either peak detect (delayed) or lower level discriminator (prompt) initation of the Busy signal. A prompt Busy Output is available on the rear panel. An internal jumper permits bringing the prompt Busy rather than a delayed Busy Output to the front-panel Busy connector for external timing and control requirements. The front-panel Busy Output pulse is positive TTL logic.

Zero Adjust: Provides for ± 0.5 V analog offset in input signal such that a zero energy (volt) input can correspond to channel zero. Set by a 22-turn potentiometer with the setting read on a LED Display for reproducibility.

Storage Offset: A converted signal for histogramming can be assigned to memory segments of 8192, 4096, 2048, 1024, 512, or 256, depending upon the conversion gain selected and memory available. With 8K of memory and conversion gain of 4K, a converted signal can be assigned to either memory half. One ADC is programmed for a storage offset of 4K channels to assign its conversions to the 4K to 8K memory segment. Up to 32 ADC's can be accommodated by 8K of memory if conversion gains on each are 250. Storage offsets of up to 65,280 channels can be provided. Storage offset programming is through the CAMAC dataway.

LINEARITY AND STABILITY

Integral Non-Linearity: Better than ± 0.0375% over 99% of 50 mV to 8 input range for shaped pulses. Typically better than ± 0.0125% over upper 99.9% of 0 to 8 V input range for strobed DC input.

Differential Non-Linearity: Better than ± 2% over upper 99% of 50 mV to 8 V input range for shaped pulses.

Temperature Stability: Less than 0.01%/°C baseline shift over 15°C to 55°C. Less than 0.01%/°C conversion gain shift over 15°C to 55°C.

DISCRIMINATION

Upper and Lower Level Discriminators: Separate controls continuously adjustable from 0 to greater than 8 V monitored by 3-digit display accurate to ± 10 mV. In the Peak-Detect mode, the discriminators' range is from 50 mV to 8 V.

CAMAC COMMANDS

All conversion data transfers and module control instructions are carried through the CAMAC dataway. When Model 3511 is used in a Model 3500M Multichannel Analyzer System, Model 3500M firmware automatically sets CAMAC functions for DMA data transfer to memory. CAMAC functions for the 3511 are:

F(0): Read data.
F(2): Reads and Clears Data, Clears LAM, and generates Q response, if LAM is present.
F(8): Test LAM, generates Q response.
F(10): Clear LAM.
F(16): Writes into control register conversion gain storage offset.
F(24): Disable.
F(26): Enable.

Initialize (Z), Clear (C), Inhibit (I) also implemented.

FRONT-PANEL CONTROLS

PD/SMP Switch: Selects either self-triggering Peak-Detect mode or strobed Sample of a DC or slowly varying AC input.

Positive/Negative Input Polarity Switch: Set for the polarity of unipolar input signal, or polarity of leading phase of bipolar input signals.

Coincidence/
Anti-Coincidence Switch:

Two-function switch dependent on operating mode selection. In Peak-Detect mode, the gate input can be used for either Coincidence or Anti-Coincidence operation, depending on the switch position. In Sample mode, the Coincidence position selects the front edge of a positive TTL or standard NIM logic pulse for initiating conversion. Anti-Coincidence position selects the back edge of triggering. When peak detecting with no gating requirement, Anti-Coincidence position is used.

Discriminator/
Zero Switch:

Select either Upper (UL) or Lower (LL) level discriminator or zero adjust setting for readout in volts on the LED display.

Discriminator
Adjustments:

Screwdriver adjustable 22-turn potentiometers set UL and LL discriminator settings. Range is from 0 to greater than 8.00 V read on the LED display. In the Peak-Detect mode, the usable discriminator range is 50 mV to 8 V (0.05 to 8.00 on the LED display).

Zero Adjust:

Screwdriver adjustable 22-turn potentiometer reproducibly sets input offset such that zero voltage input corresponds to channel zero. Offset range is ± 0.5 V. Zero setting is displayed on LED indicators which read from 0.00 to 1.00 V (where 0.00 V reads as – 0.5 V offset; 1.00 V reads as + 0.5 V offset; and 0.50 V reads as 0.00 V offset).

Risetime Select
(Side-Panel) Switch:

In the Peak-Detect mode, Model 3511 accepts shaped input pulses with risetimes in the range of 300 nsec to 20 μsec. Five switch-selectable subranges are provided to optimize the input circuit's response to the appropriate input risetime.

Position	Risetime Range
1	300 nsec to 400 nsec
2	350 nsec to 1 μsec
3	1 μsec to 4 μsec
4	3 μsec to 10 μsec
5	7 μsec to 20 μsec

For risetimes longer than 20 μsec, the input should be strobed either by an external strobe to the Str/Gate input connector, or the input should be strobed using the self-strobing capability of Model 3511 (refer to Str/Gate Input).

POWER REQUIREMENTS

1.2 A at + 6 V
150 mA at + 24 V
150 mA at – 24 V