CAMAC MODEL 3511, 3512, 3514, AND 3515
3510 SERIES

High Performance Spectroscopy ADC

Revised
September, 1984

WARRANTY

LeCROY RESEARCH SYSTEMS CORP. warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. Custom monolithics and hybrids sold separately and all spare or replacement parts are warranted for 90-days. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, LeCroy will repair and calibrate an instrument returned to the factory or an authorized service facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident or abnormal conditions or operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

The foregoing warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy Research Systems Corp., shall not be liable for any special, incidental or consequential damages, whether in contract, tort or otherwise.

IF ANY FAILURE OCCURS, notify LeCroy Research Systems Corp., or the nearest service facility, giving full details of the difficulty, and include the Model number, serial number, and FAN (Final Assembly Number) or ECO (Engineering Change Order) number. On receipt of this information, service data or shipping instructions will be forwarded to you. On receipt of the shipping instructions, forward the instrument, transportation prepaid. A Return Authorization number will be given as part of shipping instructions. Marking this RA number on the outside of the package will insure that it goes directly to the proper department within LeCroy. Repairs will be made at the service facility and the instrument returned, transportation prepaid.

ALL SHIPMENTS OF LeCROY INSTRUMENTS FOR REPAIR OR ADJUSTMENT should be made via Air Freight or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

IN EVENT OF DAMAGE IN SHIPMENT to original purchaser the instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the LeCroy factory or the nearest service facility).

DOCUMENTATION DISCREPANCIES OR OMISSIONS. LeCroy Research Systems is committed to providing unique, reliable, state-of-the-art instrumentation in the field of high-speed data acquisition and processing. Because of this commitment, the Engineering Department at LeCroy is continually refining and improving the performance of products. While the actual physical modifications or changes necessary to improve a model's operation can be implemented quite rapidly, the corrected documentation associated with the unit usually requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying unit. There may be small discrepancies that were brought about by customer-prompted engineering changes or by changes determined during calibration in our Test Department. These differences usually are changes in the values of components for the purposes of pulse shape, timing, offset, etc., and only rarely include minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry. Whenever original discrepancies exist, fully updated documentation should be available upon your request within a month after your receipt of the unit.

ANY APPLICATION OR USE QUESTIONS, which will enhance your use of this instrument will be happily answered by a member of our Engineering Services Department, telephone 914-425-2000 or your local distributor. You may address any correspondence to:

LeCroy Research Systems Corp., 700 S. Main Street,
Spring Valley, New York 10977, ATTN: Engineering Services Dept. or
LeCroy Research Systems Corp., 14800 Central S.E.,
Albuquerque, New Mexico 87123

European Customers can contact:

LeCroy Research Systems Ltd.
Elms Court
Botley
Oxford OX2 9LP England

LeCroy Research Systems SA
101 Route Du Nant-D'Avril
1217 Meyrin 1-Geneve
Switzerland

LeCroy Research Sys. S.a.r.l.
Avenue Du Parana
Z.A. De Courtaboeuf
F-91940 Les Ulis, France

LeCroy Research Systems GmbH
Werderstrasse 48
Postfach 10 37 67
6900 Heidelberg
West Germany

A T T E N T I O N

ALL 3510 SERIES ADC'S WILL BE CONFIGURED FOR STANDARD CAMAC OPERATION UNLESS THE ADC HAS BEEN ORDERED SPECIFICALLY FOR USE WITH THE MODEL 3500 MULTICHANNEL ANALYZER. REFER TO SECTION 5 OF THE OPERATOR'S MANUAL FOR DETAILS OF THE JUMPER OPERATIONS.

SEE POCKET IN BACK FOR SCHEMATICS AND PARTS LISTS.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

A T T E N T I O N

Table of Contents

SECTION 1
INTRODUCTION

LeCroy's Models 3511, 3512, 3514, and 3515 are high-speed, high resolution, ultra-linear ADC's for gamma and X-ray spectroscopy applications. The Models 3511 and 3512 offer 250 to 8000 channel conversion gains with a conversion time of 5 μsec.

The Models 3514 and 3515 offer 1.2 μsec conversion time with 4000 channel maximum conversion gain. (Note: there is an additional readout time which causes an increase in the total effective conversion time. See Appendix C for details.)

The Models 3512 and 3515 also include a buffered memory and a front-panel data connector for routing to external memories, data routes, etc.

The ADC's operate in either peak detect mode, with coincidence or anti-coincidence gating, or strobed sample mode for sampling the input signal from 100 nsec to 35 μsec after triggering the lower-level discriminator. Both bipolar and monopolar, positive or negative, DC-coupled inputs in the range of 0 V to 8 V can be accepted with risetimes of 300 nsec to 20 μsec.

Throughout the rest of this manual the four different versions of this unit will be referred to as the 3510 series or as ADC's. Only where the information is different will reference to individual versions be highlighted.

SECTION 2
DESCRIPTION

2.1 Front-Panel

Figure 2.1 shows a 3512 Front-Panel only. The 3515 is identical to the 3512. The 3511, 12 have single width and do not have the 50-pin conector or BUF FUL indicator.

2.1.1 Mode Select Switch

This switch allows the user to select a self-triggering peak detect mode or a strobed sample mode for DC or slowly varying AC signals.

2.1.2 Coincidence/Anti-Coincidence Switch

This switch serves two functions, depending on the mode of operation. In peak detect mode, the gate inputs can be used for a coincidence or anti-coincidence decision depending on the position of the switch. In coincidence position, an event will be valid if at the gate input there is either a high TTL level (2.5 V to 5 V) or a standard NIM level (-600 mV to -800 mV into 50 Ω). When using peak detect mode with no gating requirements, the switch should be in the anti-coincidence position (ANTI-COIN).

In sample mode the switch position selects the edge of a strobe pulse used to start conversion. Coincidence indicates a 0 V to +5 V TTL transition or a 0 V to -800 mV into 50 Ω NIM transition. Anti-coincidence selects the opposite transitions, i.e., 5 V to 0 V for TTL and -800 mV to 0 V into 50 Ω for NIM.

2.1.3 STROBE/GATE Input

The Strobe/Gate input serves two functions, depending upon the mode of operation. In peak detect mode this input enables conversion or disables conversion in conjunction with the coincidence/anti-coincidence switch position. Refer to section 2.1.2 for further details.

In sample mode this input receives a strobe to initiate conversion. The strobe may be TTL or NIM and polarity can be selected by the coincidence/anti-coincidence switch. (See section 2.1.2.)

2.1.4 Input Polarity Switch (+/-)

The input polarity switch is used to select the positive or negative 8 V range of input. If bipolar pulses are to be converted this switch identifies which lobe is selected for conversion.

In the negative (-) position, the signal input is directly coupled to the Track-and-Hold circuitry. In the positive (+) position the signal is inverted through a fast unity gain operational amplifier.

2.1.5 Signal Input

All 3510 series ADC's will accept positive or negative input signals (switch selectable), bipolar or monopolar from 0 V to 8 V. The input impedance is 1000 Ω for positive signals and 600 Ω for negative signals. Allowable risetime for peak detect mode is from 300 nsec to 20 μsec. One of five ranges may be selected by a side-panel switch (section 2.2.3) to optimize the response of the ADC. Minimum pulse duration is 1 μsec.

2.1.6 Display Select Switch

The front-panel switch labeled "Display" allows the user to monitor one of three voltages via the three-digit, seven-segment LED display. These voltages are the Lower and Upper Level discriminator settings and the Zero Level Offset.

2.1.7 Upper- and Lower-Level Discriminators

The lower-level discriminator sets the lower limit of analog signals to be analyzed. A 22-turn, screwdriver-adjustable potentiometer is available on the Front-Panel for changing the lower threshold level from 0 V to 8 V. A three-digit, seven-segment display indicates the voltage when the display switch is in the appropriate position.

The upper-level discriminator sets the upper limit of analog signals to be analyzed and is adjusted in the same manner. In sample mode, LLD and ULD act together to define a "window" of operation for the ADC. If the signal to be converted is not within this set range, conversion will not take place. A signal below the LLD will fail to enable the conversion circuitry, whereas a signal greater than the ULD will disable the conversion circuitry until the signal goes below the ULD setting.

In peak detect mode, the LLD and ULD provide the same functions with a slight exception. Should a signal to be converted exceed the ULD, a latch is set preventing the conversion circuitry from being triggered until the input signal drops below the LLD, resetting the flip flop. The next peak within the window will start a conversion cycle. This technique will prevent conversion of signals having long tails or secondary peaks.

2.1.8 Zero-Level Adjust

Zero level is defined as that analog input level which corresponds to channel zero after conversion. This control permits the user to adjust the scale for a given conversion gain to a convenient value to aid in interpreting data.

The front-panel screwdriver adjustment is a 22-turn potentiometer which ranges over ±6.25% of full scale. Monitoring of the offset is provided with the 3-digit front-panel display.

When the display select switch is in the "zero" position the indicated voltage is +0.50 V greater than the actual offset at the ADC. A setting of 0.75 V, therefore, is a 0.25 V offset where a setting of 0.30 V is a negative 0.20 V offset.

To adjust the offset to a desired value:

1. Toggle the display select switch to zero position.
2. Add the desired offset (+ or -) to 0.50 V.
3. Adjust the potentiometer until the display shows the value calculated in step (2).
4. The setting may be recorded for future reference and computations.

The voltage for conversion is the voltage input less the voltage offset where the voltage offset is equal to the front-panel displayed voltage minus 0.50 V.

NOTE: The zero level adjust does not affect the discriminator settings in any way.

2.1.9 Busy Out Signal

Busy is a signal which is generated when the ADC is literally Busy. By definition, once a signal exceeds the LLD setting, the ADC is enabled to perform a conversion. The Busy signal is generated at this time and remains set until the signal input falls below the LLD setting and the conversion is read. Thus, Busy gives a direct indication of the deadtime of the ADC.

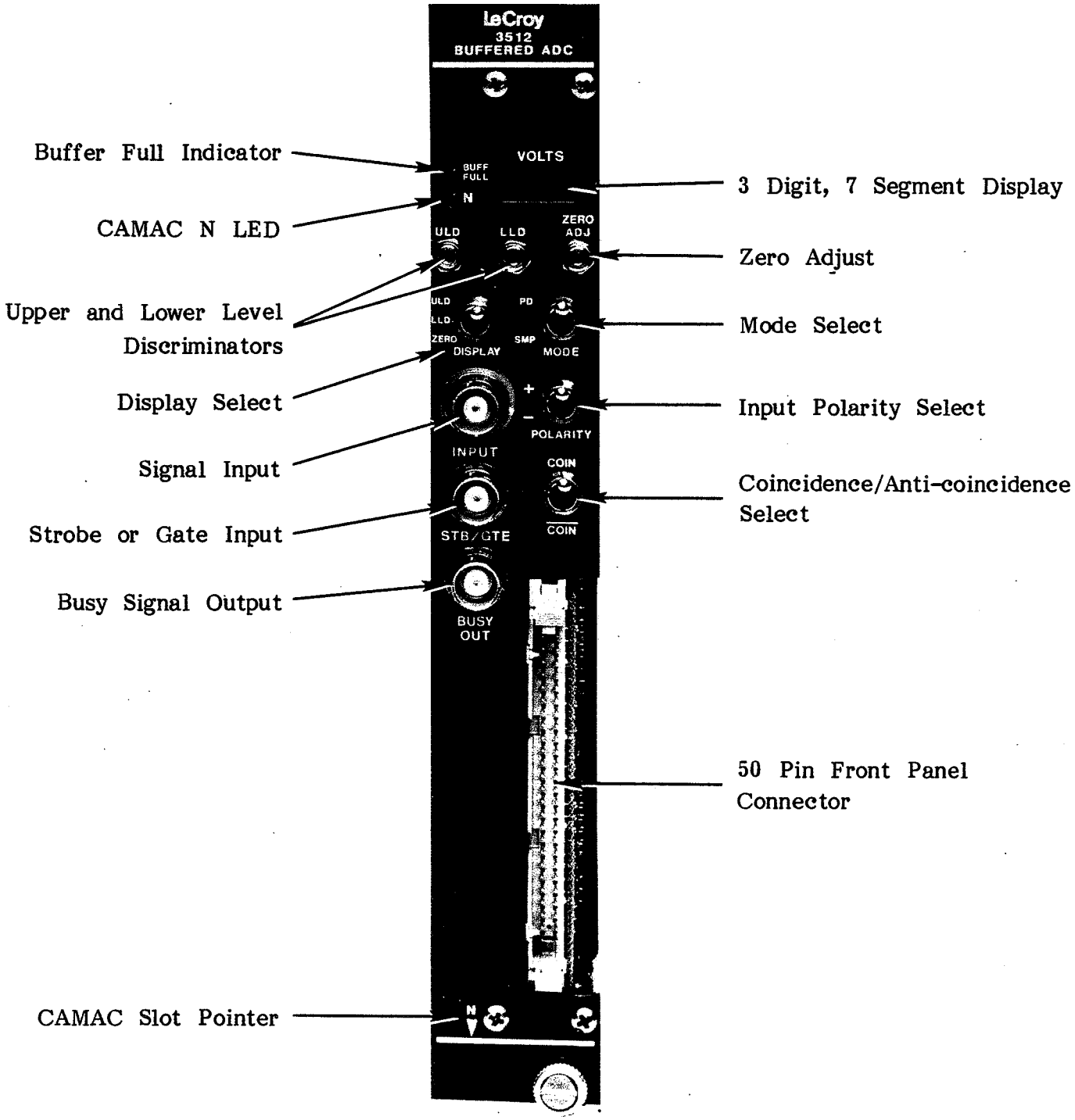

Figure 2-1
3512 Front-Panel shown
(See Section 2.1)

An internally jumpered option for a delayed Busy (relative to LLD or Trigger flip flop output) is available and accessible to the user through the side panel (section 2.2.1). This option adds flexibility where:

1. Two or more ADC's are cascaded using the Busy of one to gate a second, etc.; a delayed Busy will prevent the second ADC from converting on long tailed pulses, i.e. two conversions of one pulse. In this mode, all but the first ADC must be set for coincidence (COIN) mode.

2. The delayed Busy may be used to provide a strobe in sample mode where the time relationship is known between the LLD firing and the desired point for conversion. Thus, it becomes an internal delay generator.

2.1.10 50-Pin Front-Panel Connector (Models 3512 and 3515 only)

This connector allows a 16-bit data word to be read directly out of the ADC, bypassing the internal memory section. Control lines are provided which allow for a full handshake in the data transfer.

Alternatively, a 13-bit data word may be Jammed into the buffer memory via this connector, and control lines are provided for this purpose.

An internal switch must be set to select one of these modes (section 2.4.1).

Signal (Ext. Jam Mode)	Signal (3588 Bus)	Pin
Ext. Jam Data Ready	BRI	1
Ext. Write Enable	WRITE	3
Not Used	BRO	5
Not Used	GRANT	7
Jam. Ack.	ACK	9
Bit 0	Bit 0	11
Bit 1	Bit 1	13
Bit 2	Bit 2	15
Bit 3	Bit 3	17
Bit 4	Bit 4	19
Bit 5	Bit 5	21
Bit 6	Bit 6	23
Bit 7	Bit 7	25
Bit 8	Bit 8	27
Bit 9	Bit 9	29
Bit 10	Bit 10	31
Bit 11	Bit 11	33
Bit 12	Bit 12	35
Bit 13	Bit 13	37
Bit 14	Bit 14	39
Bit 15	Bit 15	41

NOTES:
1. All even numbered pins are grounded.
2. Bits 16, 17, 18, and 19 are not implemented (and are left open).
3. ODD numbered pins are on the left side of the connector (as seen from the front) with pin 1 at the top. EVEN numbered pins are on the right with pin 50 at the bottom.

Table 2-1
Pin Designations for Front-Panel Connector

2.1.11 N Station Indentifier

A front-panel LED labeled N refers to CAMAC station N. The LED is strobed with a pulse, approximately 100 msec in duration, each time the station occupied by the ADC is addressed.

2.1.12 Buffer Full Indicator (Models 3512 and 3515 only)

This front-panel LED indicates when the internal buffer memory contains 1024 words. At this point, no more conversions will occur until CAMAC read cycles start to empty the buffer.

2.2 Side Panel

2.2.1 Delayed Busy Adjustment

The delayed Busy is a unique feature in that if the time relationship is known between the time of LLD crossing and the time of the signal of interest to be converted, a delayed Busy output may be adjusted and used to strobe the ADC. Thus, the Busy becomes an internal delay generator. Use of this feature requires the jumpers to be in the following position:

E-10 to E-11 (Busy signal initiated by firing of LLD)
E-15 to E-14 (Delayed Busy)

Refer to Figure 2-2.

An oscilloscope should be used to measure the time between the delayed Busy and the desired peak for conversion. Adjust the delay potentiometer so that the positive going edge of Busy Out occurs 100 nsec after the peak of interest. The delay will range from 100 nsec to 35 μsec.

A second jumper option, also accessible through the side cover, determines when Busy (prompt or delayed) is initiated; at the time the LLD fires (E-11 to E-10) or when the Trigger flip flop is clocked (E-11 to E-12).

When cascading ADC's, only the unit nearest the 3541 Deadtimer will be jumpered such that Busy is generated by the LLD crossing.

If strobing or digitizing DC levels or slowly varying AC inputs which do not go below the LLD setting, Busy will be a function of the Trigger flip flop and indicate the time of conversion.

NOTE: Jumper setting E13 - E14 selects a prompt Busy.

2.2.2 Cascaded Busy Selection

Unless the ADC's are being cascaded to reduce dead time, the side-panel jumper should be set to connect E-17 to E-18. This provides the normal Busy discussed above.

However, if several ADC's are being cascaded, it is necessary to modify the Busy OUT by connecting E-17 to E-16. This assures that only one unit will convert a given pulse, by ANDing the gate input with the Busy signal. Note that all units after the highest-priority unit should be set to coincidence (COIN) mode.

2.2.3 Risetime Select

Peak detection is performed in the ADC by applying the signal for conversion and a delayed version of the signal at the inputs of a comparator. The Track-and-Hold circuitry is switched into hold when the comparator senses a zero crossing.

In order to cover a wide range of pulse shapes and risetimes, five overlapping ranges of user-selectable values of phase delay are available via the Risetime Select switch. These delays are calibrated to specific ranges of risetimes and should be adjusted by the user so that the range selected overlaps the risetime of the signal to be converted.

Switch Position	**Risetime Range**
1	300 nsec - 400 nsec
2	350 nsec - 1 µsec
3	1 µsec - 4 µsec
4	3 µsec - 10 µsec
5	7 µsec - 20 µsec

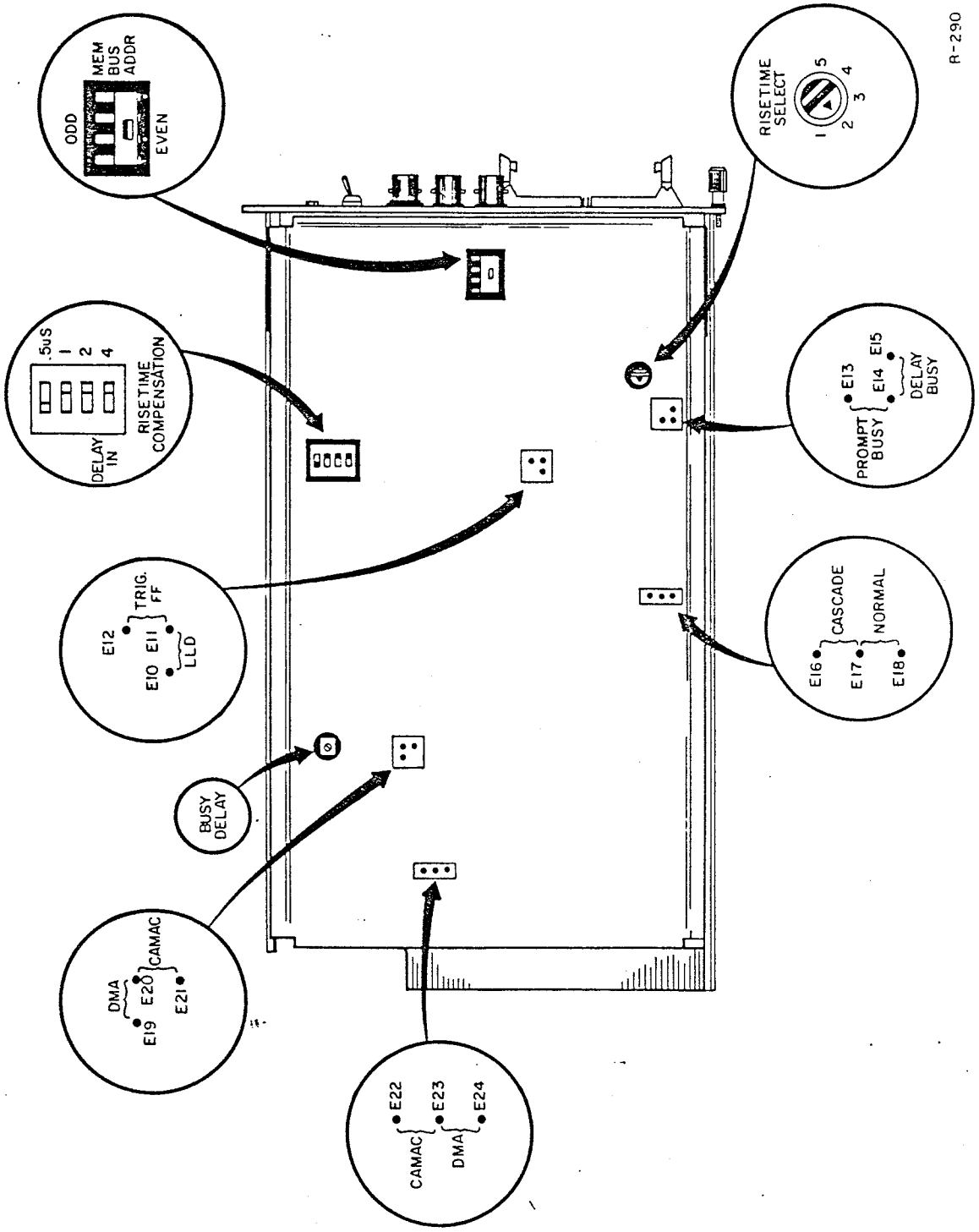

Figure 2-2
3512(15) Side Panel
3511(14) Identical except for no MEM BUS ADDR Switch

2.2.4 Risetime Compensation Adjustment

The risetime compensation switch sets the delay between the capture of the peak and the beginning of the conversion. This time should be set to the smallest value possible. Therefore, turn switch 1 OFF (OPEN for rocker switches) and leave switches 2, 3, and 4 ON (CLOSED for rocker switches). Note that all the switches ON (CLOSED for rocker switches) is an illegal setting.

2.2.5 Memory Bus Address Switch (Models 3512 and 3515 only)

This switch is located on the rightmost circuit board of the 3512(15) (as seen from the front) and is visible through the side-panel opening labeled "MEMORY BUS ADDRESS". The Memory Bus Address switch is needed only when the 3512(15) is used with LeCroy's Model 3587 Data Router or Model 3588 Histogramming Memory. When more than one 3512(15) is connected to either of the above named modules, the Memory Bus Address switch is used to indicate whether the 3512(15) is in an "ODD" or "EVEN" position in the chain. "ODD" is selected when the switch is "thrown" toward the top of the module. See Appendix A for more details.

2.2.6 CAMAC/DMA Jumpers

The ADC is factory set to operate with the standard CAMAC cycle (ESONE Report EUR 4100e). A jumper option is contained within the unit, however, to change the CAMAC read control to a modified read/write cycle. This cycle is compatible only with the 3500 Acquisition and Control System DMA cycle.

CAMAC Position: E22 - E23 and E20 - E21
DMA Position: E23 - E24 and E19 - E20

See section 2.4.2 for details on an internal CAMAC/DMA jumper.

2.3 Rear Panel

2.3.1 Rear-Panel Connectors J2 and J3

Two dual in-line 10-pin connectors are provided at the right rear panel. From bottom to top they are identified as J2 and J3. These connectors are used for interconnecting modules in multiple ADC applications and with the Model 3541 Deadtimer.

Right-hand portion of Figure 2-3 illustrates the pin assignment for each connector. Pin 2 of both J2 and J3 is an open collector common signal which can be received by and/or transmitted to disable all ADC modules which may be operating in parallel. Pin 8 of J2 is a prompt Busy output signal to be cabled directly to a 3541 Deadtime module.

2.3.2 Rear-Panel LAM Select J6 (3512 and 3515 only)

To facilitate reading out the 3512(15)'s buffer, a rear-panel jumper option (J6) allows the user to select when a LAM is generated. By positioning the jumper in the appropriate position, the LAM can be asserted when the buffer contains 1, 2, 4, 8,...,512, or 1024 words. (Refer to Figure 2-3).

Once the LAM has been asserted, it stays on until the buffer has been emptied, thus facilitating block transfers. The state of the LAM can be tested with an F(8) or an F(2). (Note however, that an F(2) is a destructive read).

2.4 Internal Switches and Jumpers

2.4.1 Front-Panel Read Enable Switch (3512 and 3515 only)

This switch positioned on the 3512(15)-1 board (i.e., the right hand board as seen from the front), directly behind the Front-Panel, is used to select either Buffer Memory Mode or External Read Mode via the 50-pin front-panel connector. The switch, six ganged double-pole double-throw switches, route the appropriate control lines to the front-panel connector. Buffer Memory Mode includes the external Jam handshake logic. This is the normal mode of operation, and units will be shipped with the switch in this position unless shipped with a LeCroy 3588 Histogramming Memory Module. See Figure 2-4 for information on setting this switch.

2.4.2 CAMAC/DMA Jumper on 3512(15)-1 Board (3512 and 3515 only)

An additional CAMAC/DMA jumper is located on the 3512(15)-1 board (the righthand board as seen from the front of the module) for ECO #1034 and later. This 2-position jumper is located on the component side of the board between chips CO and DO (near CAMAC card edge connector). The upper position is for DMA operation and the lower position selects CAMAC operation.

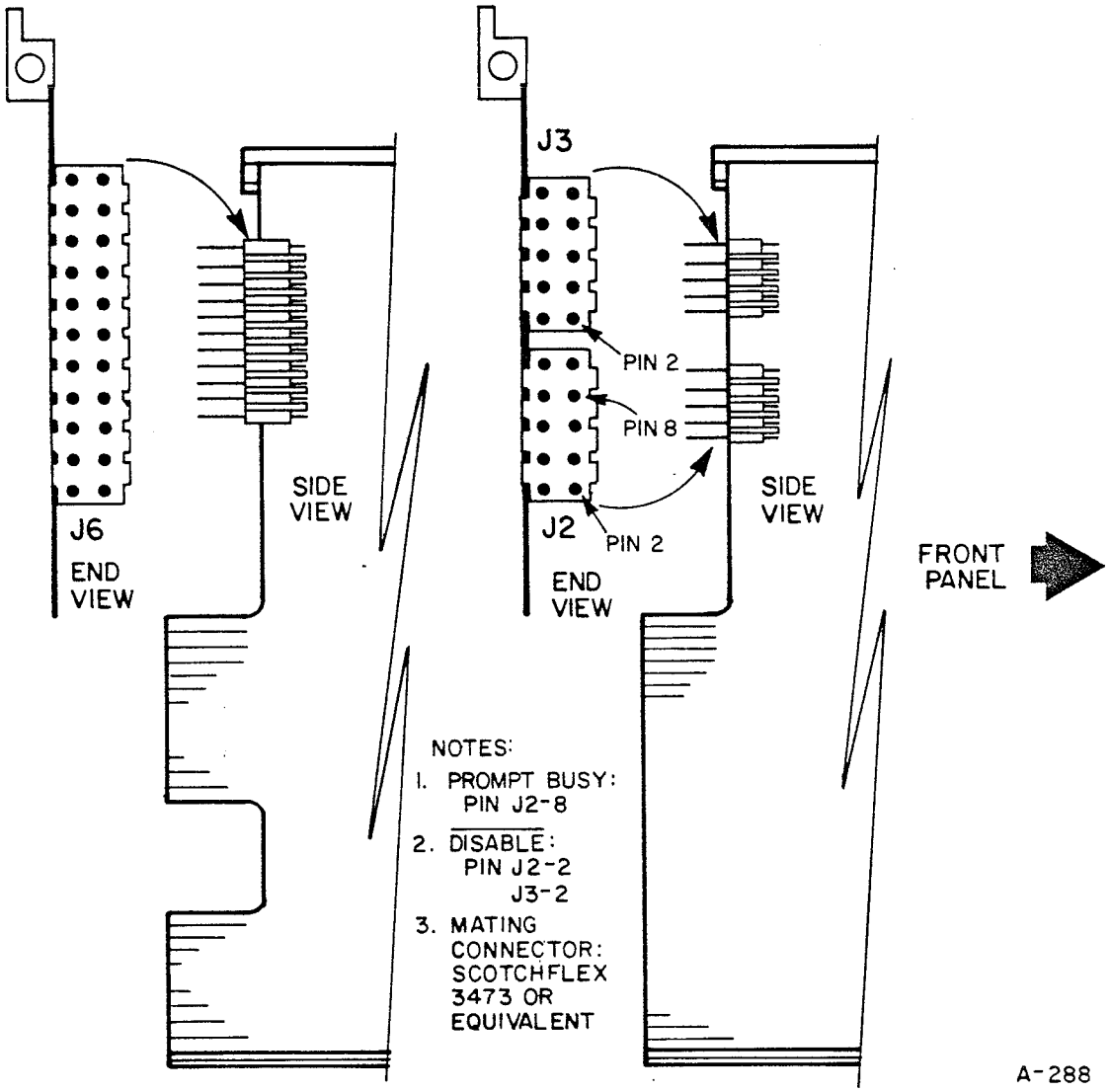

Figure 2-3
Rear Panel

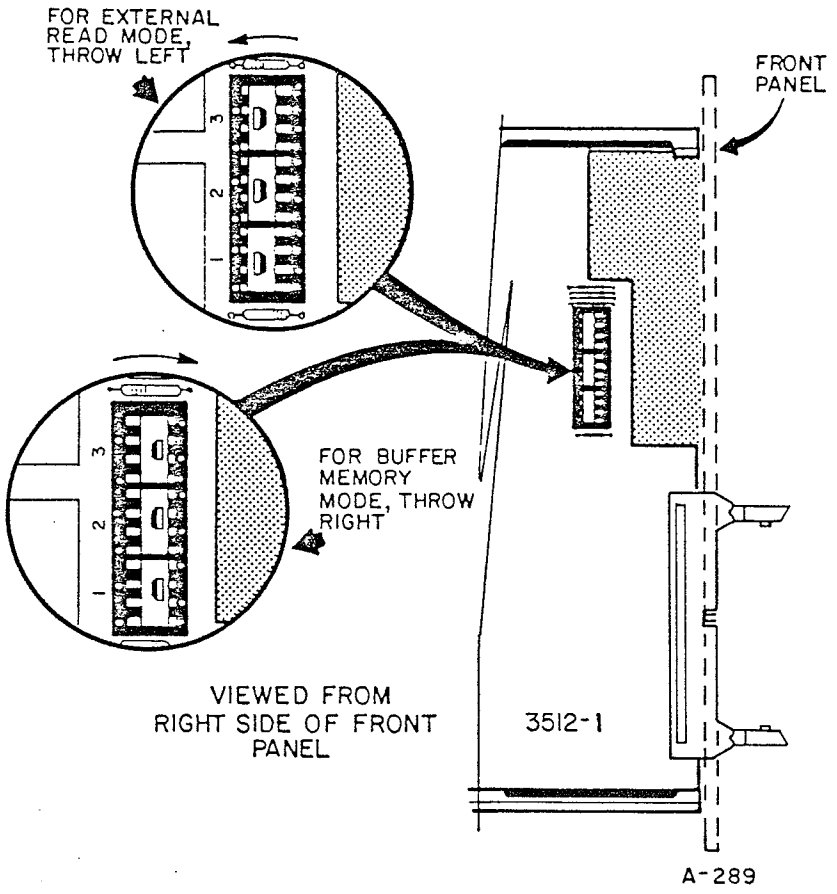

Figure 2-4
Front-Panel Read Enable Switches
(3512 and 3515 only)

SECTION 3
CAMAC CONTROL

3.1 CAMAC Function Codes

The operational function codes for the 3510 series ADC's are explained in the following text. These codes are valid for any sub-address and only with a valid station number (N), with the exception of Z, C, and I. Sub-addresses are not decoded.

F(0) Read Data. Non-destructive read. Causes increment memory read pointer after read.

F(2) Read Data. Destructive read. Generates Q response if data is present, clears LAM when buffer is empty.

F(8) Test LAM. Generates Q response if LAM is present. Can be used to test state of LAM flip flop even if LAM is disabled (F(24)).

F(9) Reset Offset DAC. Used for test purposes.

F(10) Clear LAM and buffer.

F(16) Writes into control register conversion gain, storage offset, mode select, and acquisition enable/disable (see Table 3-1).

F(24) Disable LAM.

F(26) Enable LAM.

Initiates (Z), Clear (C), and Inhibit (I) are also implemented.

3.2 Programming the 3510 series ADC's

Refer to Table 3-1 while reading this section.

Storage offset and conversion gain are programmable for the ADC through the CAMAC Dataway write lines, W1 through W11. W1 through W8 define the storage offset which may be as small as 256 or as large as 65280 and any increment of 256 between these limits. Note that the offset must be an integral multiple of the gain.

W9 through W11 are used to form a binary code which defines the conversion gain. Note that codes of 0 and 7 are illegal as indicated in Table 3-1 and should be avoided.

W12 is a decrement/increment flag. It is not normally used in CAMAC operation but is used when the ADC is operated in LeCroy's 3500 Acquisition and Control System. W12 should be set to 0 for normal DMA operation (i.e., increment memory at the address).

W13 (3512 and 3515 only) selects between Multi-parameter or Normal operation.

W14 (3512 and 3515 only) is used to program the ADC for operation in either a normal CAMAC environment or in a System 3500 when multi-parameter operation has been chosen.

W15 is not used.

W16 is used to enable or disable data acquisition.

W17 thru W24 are not used.

Conversion Gain	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
8000(4000)	0	0	1								
4000	0	1	0								
2000	0	1	1								
1000	1	0	0								
500	1	0	1								
250	1	1	0								
Storage Offset											
32768				1	0	0	0	0	0	0	0
16384				0	1	0	0	0	0	0	0
8192				0	0	1	0	0	0	0	0
4096				0	0	0	1	0	0	0	0
2048				0	0	0	0	1	0	0	0
1024				0	0	0	0	0	1	0	0
512				0	0	0	0	0	0	1	0
256				0	0	0	0	0	0	0	1

W16	**W14**	**W13** (3512 or 3515 only)	**W12**
0 Enable Acquisition	0 3500	0 Normal	0 INCR FLAG
1 Disable Acquisition	1 CAMAC	1 Multi-parameter	1 DECR FLAG

Table 3-1
3510 Series Control Register

3.2.1 Normal CAMAC Operation (Model 3512 and 3515 only)

This mode of operation is entered when a zero is written as bit 13 (W13) of the control word. In this mode, Storage Offset and Conversion Gain can be programmed and implemented as shown in Table 3-1. If this mode is selected, bit 14 (W14) will not have any effect on operation of the 3512(15).

As an example, suppose a conversion gain of 2000 is to be offset by 4096. Selecting the appropriate values in the left column of Table 3-1 and following the lines to the right will identify the proper write bits to enable. The conversion gain of 2000 indicates bits W10 and W9 while the storage offset of 4096 requires bit W5.

After the front-panel controls are set appropriately, and after the jumpers and switches accessible through the side cover have been set, the rear-panel LAM select jumper must be set to generate LAM after the buffer has filled to the required depth.

Suppose, for example, that this jumper is set to 512 words. Then when acquisition starts, a LAM will not be generated until there are 512 words in the buffer. Either the LAM can be directly used to generate a controller interrupt (assuming LAM has been enabled with an F(26), or the state of the LAM status register can be tested with an F(8) command (which will generate Q=1 when LAM is set). In either case, when the LAM is asserted, the buffer is read out using an F(2) command. The F(2) will generate a Q=1 response for all reads in the buffer. Hence, more than 512 words (in our example) will be read out before the buffer is emptied.

Figure 3-1 shows a typical Flow Diagram.

3.2.2 Multi-parameter Operation (Modles 3512 or 3515 only)

The 3512(15) can be used for multi-parameter operation in either a conventional CAMAC environment, or in the 3500 System. Basic operation is the same in both environments but the 3500 System allows a little more flexibility of operation.

If Bit 13 W(13) of the control word is a 1, then the 3512(15) will be configured for multi-parameter operation. This modifies the normal operation of the 3512(15) in the following ways:

(1) It is assumed that a common gate will be provided to all modules. If a peak is not detected in the gate interval, the back edge of the gate will cause a zero data word to be written into the buffer. This assures that data from different 3512(15)s can be correlated, since all will generate the same number of data words. As a check on this, tag bits are provided. These tag bits constitute the 14th, 15th, and 16th bits of the dataword. An internal counter generates these tag bits, the counter being incremented after each gate. By monitoring these three bits, it is possible to see discontinuities in the sequence, indicating missing data.

(2) A 13-bit delimiting word may be simultaneously Jammed into all 3512(15) memories via the 50-pin front-panel connector. This provides a time reference to facilitate reconstruction of an event. By combining this with the information in the tag bits, accurate reconstruction and correlation is possible, and bad data blocks can be disregarded. For more information on the external Jam operation see Appendix B.

In 3500 multi-parameter operation (bit 13 asserted and bit 14 off), it is possible to read the same data twice. This is accomplished by alternating an F(0) read sequence (until buffer empties) with an F(2) read sequence. When an F(0) read is performed, the read pointer and buffer length counter values are latched internally, and re-loaded when the first F(2) read is performed. This has the effect of making the F(0) read non-destructive. During F(0) reads, the three high order bits (R14, R15, and R16) will consist of the tag bits, while during an F(2) read the upper bits will contain the storage offset. This allows the "simultaneous" storing of the list mode data (from the F(0) reads) and fast histogramming (using the F(2) reads).

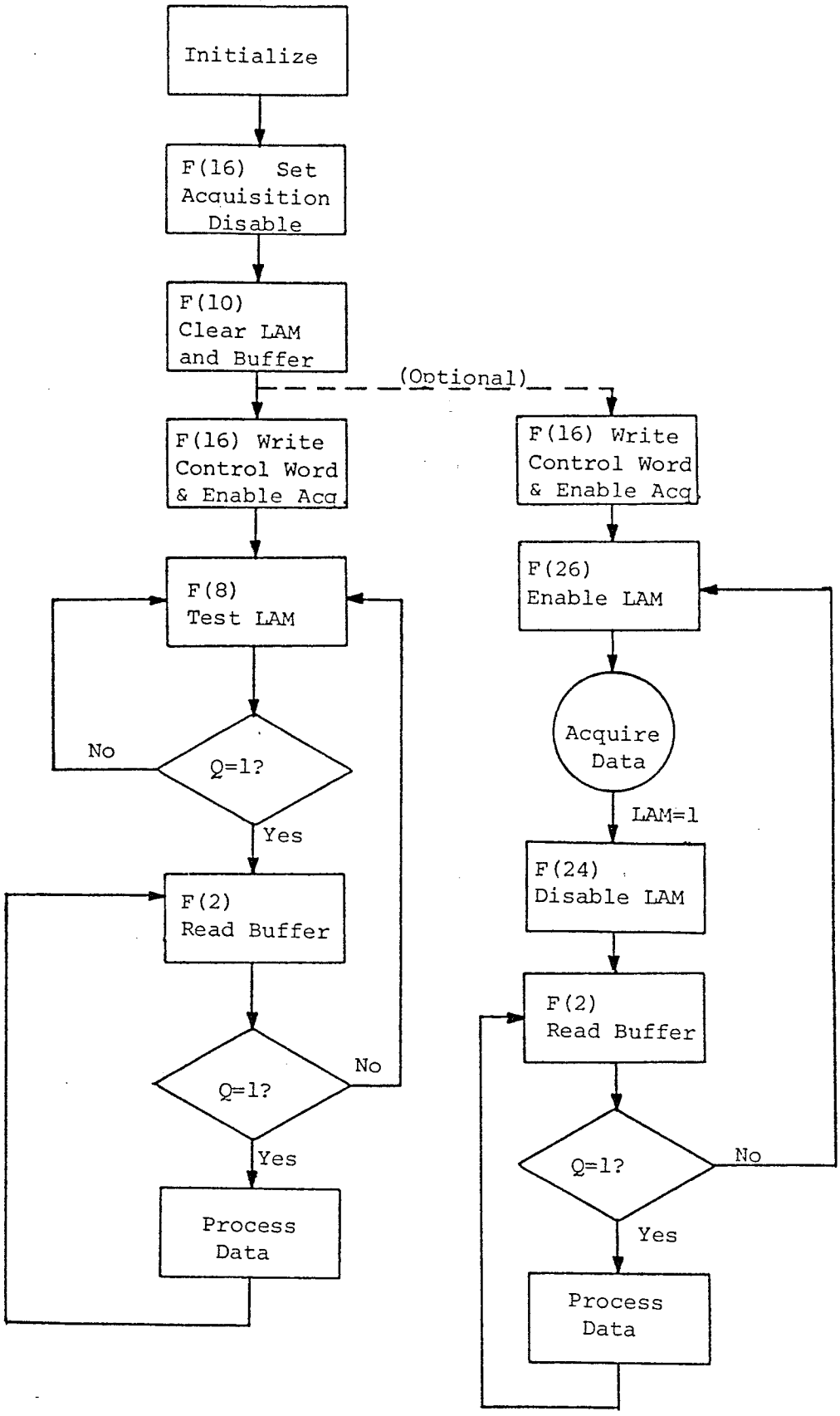

Figure 3-1
Typical Flow Diagram
in 3512(15)

SECTION 4
OPERATIONAL DESCRIPTION

4.1 Sample Mode

4.1.1 Functional Description

In sample mode, the signal for conversion is tracked by the Track-and-Hold circuitry. If a positive signal is at the input, it is fed first through an inverting op-amp with unity gain. The same signal is seen by the lower level and upper level discriminators. This signal level must be more negative than the lower level setting and less negative than the upper level setting to enable the ADC. When the input signal exceeds the LLD setting, a prompt Busy signal is generated and output at pin 8 of J2 and optionally at the Busy Out BNC.

If one of the above conditions is not met, the conversion circuitry is disabled.

At this time, a strobe signal (leading edge) will switch the track-and-hold into the hold mode and initiate the ADC conversion.

The signal input is summed with the Zero Adjust Offset and an offset DAC output whose value increments automatically with every conversion. The offset DAC output acts as a sliding scale offset which is then digitally subtracted from the ADC output after conversion. The use of this "random" offset permits excellent differential linearity characteristics, matching those of a Wilkinson ADC but with a fraction of the conversion time (5 μsec for a 13-bit conversion).

Conversion gain is the number of channels into which the 0 V to +8 V input range is divided. This is programmable and adjustable in binary steps from 250 to 8000 (4000 in 3514 or 3515) full scale (refer to section 3). After a digital subtraction of the DAC offset mentioned above, the previously programmed conversion gain is applied to the converted word.

Conversion gain provides for an adjustment of the ADC resolution. For smaller memory systems (less than 8K) full dynamic range can be employed but at the expense of resolution. An example is a memory size of 4K channels where a full spectrum can be stored but with only one-half the maximum resolution.

Storage offset, also programmable, is then applied to the conversion signal before it is read out on the CAMAC Dataway. A converted signal can be assigned to memory segments of 256 to 64K in binary steps depending on the conversion gain selected and memory available. With 4K of memory and a conversion gain of 2K, a converted signal can be stored in either half of the memory. The remaining half of memory can then be used with another 3510 series ADC or perhaps the same ADC but with different conditions.

4.1.2 Examples

4.1.2.1DC Levels

Assume conversions are to be done on negative DC levels which will be strobed by a high to low TTL edge. The only levels of interest are those between -2.15 V and -6.75 V.

Adjust the ADC as follows:

1. Set risetime adjust to 500 nsec (minimum setting).

2. Set the side-panel jumpers E-11 to E-12 and E-14 to E-15 (delayed Busy signal initiated by trigger flip flop).

3. Set the display select switch to Zero and adjust the Zero Offset potentiometer to display 0.50 V.

4. Set the display select to LLD and adjust the lower-level discriminator potentiometer to display 2.15 V.

5. Set the display select switch to ULD and adjust the upper-level discriminator potentiometer to display 6.75 V.

6. Set the INPUT switch to (-), the negative input position.

7. Set the MODE switch to SMP, sample.

8. Set the coincidence/anti-coincidence switch to anti-coincidence, (ANTI-COIN).

9. Connect the signal input and the gating signal to the INPUT and STB/GTE front-panel connectors, respectively.

The ADC is now ready to be programmed for conversion gain and enabled to receive and convert data.

4.1.2.2 Wide Pulse Signals

The following example of a Sample Mode conversion is based on a slowly varying input signal, risetime of 25 μsec and duration of approximately 100 μsec. By knowing the time associated with the peak of interest, the internal Busy Delay adjust will be used to generate a strobe input to convert the exact peak of interest.

To measure the delay at Busy Out a short CAMAC routine will be required to enable the ADC and to cycle the ADC with F(2) commands.

1. Set the side-panel jumpers to provide a LLD initiation of Busy, E-10 to E-11, and delayed Busy to Busy Out, E-14 to E-15.

2. Toggle the display switch to Zero Offset and adjust the zero potentiometer until 0.50 V is displayed.

3. Toggle the display switch to LLD and adjust the lower-level discriminator to the minimum possible value without going below the noise or background level of the input signal.

4. Toggle the display switch to ULD and adjust the upper-level discriminator to its maximum setting.

5. Toggle the Input switch to (+) positive.

6. Toggle the Mode switch to SMP, sample.

7. Toggle the coincidence/anti-coincidence switch to coincidence (COIN).

8. Connect the Input signal to be converted to the INPUT BNC.

9. Connect Busy Out to STB/GTE input.

10. With an oscilloscope and the above mentioned CAMAC routine, observe the Busy Out in relation to the desired input peak.

11. Adjust the Busy delay monostable so that Busy Output goes high 100 nsec after the peak of interest.

The ADC is now ready to take data.

4.2 Peak Detect Mode

4.2.1 Functional Description

In Peak Detect Mode, the signal is seen by the upper level and lower level discriminators, the Peak Detect circuitry and the Track-and-Hold. If the signal is positive, it is first inverted by an op-amp with unity gain.

Once the leading edge crosses the lower-level discriminator threshold (with gate enabled) the peak detection circuitry and the conversion Trigger flip flop are enabled.

The Peak Detection circuitry utilizes the pulse input signal and a delayed version of the same signal at the inputs of a comparator. When a zero crossing is detected, the conversion flip flop is triggered and the Track-and-Hold circuitry is switched to the hold mode. Conversion begins after the risetime compensation delay.

If the upper level discriminator threshold is exceeded, a latch is set preventing the conversion flip flop from being triggered until the trailing edge of the signal to be converted falls below the lower level discriminator threshold.

The analog signal is now summed with the Zero Adjust Offset and the output of an offset DAC. After conversion the digital value of the DAC offset is subtracted from the converted word. This bin width averaging technique achieves excellent differential linearity characteristics.

The ADC can pre-process data with respect to storage offset and conversion gain. The conversion gain and storage offset are programmed into the ADC prior to conversion. Thus the data presented at the read lines of the CAMAC dataway may be transferred directly to memory.

4.2.2 Operation

Peak Detect Mode of the ADC provides a 13-bit (12-bit for 3514 or 3515) channel address proportional to the amplitude of the input signal. Conversion can be performed on positive or negative pulses from $\pm$50 mV to $\pm$8 V in amplitude or on bipolar signals when the front-panel switches are set properly for the lobe of interest.

As described in the Sample Mode, operation of a CAMAC software routine will be required to program conversion gain and storage offset and to enable and cycle the ADC. Refer to the section 3 for more programming information.

Peak Detect conversions will be performed on a negative pulse in the following example. The pulse risetime is 4 μsec and pulse duration is 12 μsec. A region of interest will be defined between 750 mV and 6 V.

1. Toggle the display select switch to Zero and adjust the Zero Adjust to display 0.50 V.

2. Toggle the display select switch to LL and adjust the LL potentiometer until the display indicates 0.75 V.

3. Toggle the display select switch to UL and adjust the UL potentiometer to display 6.00 V.

4. Toggle the Input polarity switch to the negative (-) position.

5. Toggle the Mode switch to Peak Detect (PD).

6. Gating will not be used, therefore, toggle the coincidence/anti-coincidence switch to anti-coincidence (ANTI-COIN).

7. Connect the Input signal to the front-panel INPUT BNC.

The ADC is ready to convert the input pulses.

4.3 Buffer Memory Mode (Modles 3512 or 3515 only)

If a CAMAC read cycle is initiated while a data transfer to the buffer is taking place, erroneous data can result. It is recommended, therefore, that the 3512(15) be disabled (with an F(24) or by asserting the CAMAC Inhibit line) during readout. If the 3512(15) is in External Read Mode, the buffer is disabled and the unit need not be disabled for readout.

SECTION 5
TECHNICAL DESCRIPTION
(For 3511 only, except all ADC boards of 3510 series are similar.)

5.1 Introduction

The diagram below illustrates the functional blocks of the 3511. A Technical Description of each section follows. The 3511 can be divided into five independent sections.

FUNCTIONAL BLOCKS, 3511

Input Gating - includes selection of Mode, Input Polarity, Risetime Select, Upper and Lower Discriminator Levels. In effect, all conditions must be met by the analog input in this section before conversion can take place.

ADC - is the heart of the 3511. In this section are the Track-and-Hold, the ADC, an offset DAC providing bin width averaging, and the zero adjust offset.

Control Logic - combines CAMAC control with the Input gating to provide the timing and initialization of conversion plus control of the BUSY OUT.

The Data Processor - performs pre-programmed manipulations on the converted input signal. These include storage offset, digital conversion gain and digital subtraction of the DAC offset. The CAMAC read and write lines tie into this section but are enabled by the control logic section.

Display - provides for the front-panel 3-digit readout of either of the discriminator levels or of the zero offset adjustment.

5.2 Input Gating

5.2.1

The gating circuitry for the 3511 has been designed to accomodate both TTL (logical 1 = 2.0 to 5.0 V) NIM input levels. (Logical 1 = 600 mV to -800 mV into 50 Ω.) The circuitry inverts the gating signal, thus requiring a second inversion in coincidence mode, through gate HA-4.

With the gate input at ground potential, Q11 is biased on and provides standing current through the 1K resistor to ground and a high TTL level at the input of the inverting gate HA-5. The NPN transistor Q12 provides a low impedance path for negative signals (NIM) forcing the input lead at gate HA-5 to go low. Similarly, a positive input (TTL) will turn off transistor Q11 allowing the 1K resistor to pull the input of gate HA-5 low.

A low impedance (50 Ω) will be seen by NIM signals, whereas TTL signals will see a high impedance at the Strobe/Crate input.

5.2.2

A 74S74 is used at the Trigger flip flop. The Q and Q-outputs of this flip flop trigger the circuitry for conversion. Conditions for a trigger are a TTL high at the D input and a positive going edge at the CLK input of the Trigger flip flop.

The valid D input level will exist when:

1)Coincidence is valid,
and 2)The lower level discriminator (LLD) setting is exceeded by the analog input signal,
and 3)the upper level discriminator (ULD) setting is <u>not</u> exceeded.

The discriminating comparators see a negative analog signal at their respective inverting inputs. This signal is compared with the operator adjustable DC levels at the non-inverting inputs (upper/lower limits).

5.2.3

In Sample Mode when the signal at the LLD input exceeds the LLD setting, the comparator output will switch to a TTL high allowing the output at gate FB-11 to go high. In a similar manner, if the signal exceeds the ULD setting, its output will switch to a TTL high, be inverted at gate HA-13 to a low and force the output at gate FB-11 low. The latter will disable the Trigger flip flop until the analog signal falls below the ULD setting.

The gating circuitry in sample mode, provides a coincidence condition (a high at the input of gate HA-3) as well as the clock input for the Trigger flip flop (positive edge at the input of gate FC-1) using the same signal.

5.2.4

In Peak Detect Mode the low level output of LLD sets a high level at the Q output of the ULD flip flop, HB-6. When the LLD output goes high (LLD setting is exceeded by analog signal) the peak detect circuitry is enabled. Should the input signal exceed the setting of the ULD the ULD flip flop HB-6 will go low to disable gate FB-4. The flip flop is reset (HB-6 goes high) when the input signal falls below the LLD setting. This will prevent spurious triggering of the flip flop on long tail analog inputs. If gating is not provided, the Gate/Strobe input should be terminated or left open circuited. The coincidence/anti-coincidence switch must be in the coincidence (COIN) position to enable gate HA-3. Once the D input of the Trigger flip flop (AD-12) goes high, the peak detect circuitry must generate a clock edge to trigger the flip flop.

The Peak Detector is a gated comparator having the analog signal on each input, but with an adjustable delay (Risetime Select) on the inverting input. The comparator output switches to a high level when the delayed input level crosses the non-delayed input level, or at a zero slew rate. The variable delay allows the user to optimize the zero crossing for a variety of pulse shapes and risetimes, i.e., a longer delay for slow risetimes to prevent false triggering of the Peak Detector on the rising edge.

The low to high transition propagates through two gates to clock the Trigger flip flop. The non-inverting input of the peak detector also has an offset control. This is adjusted at the factory to provide the best response. It should not be further adjusted by the user as it will affect linearity.

5.3 ADC

5.3.1 Track-and-Hold

If the analog input is positive, it is inverted by a fast slewing op-amp (CA) of unity gain to provide a negative signal at the input of the Track-and-Hold circuitry. The Track-and-Hold circuitry input ranges between 0 and negative 8 V.

While tracking, transistor Q9 is on providing gate voltage to the DMOSFET, Q6. Thus, the FET switch is closed and the op amp DA is an inverting amplifier with a gain of 1.25. Upon receiving a trigger, the base of Q10 is pulled low turning it on and Q9 off. The FET switch is opened and the op-amp becomes a simple integrator without the feedback resistor, and holds the gated voltage constant at the input of the ADC.

5.3.2

Charge injection from gate to source during the switching of the FET will be cancelled by the transient compensation, C22.

The ADC input must remain stable during conversion to prevent any missing codes. Should a fast edge appear at the analog input during conversion, signal injection due to the drain source capacitance will be nulled by feed forward compensation. This is provided by opposite phase injection of the same signal by Q7 and C25.

Both C25 and C22 are trimmed at the factory for best operation and performance and should not require further adjustment by the user. The Track-and-Hold circuitry will remain in the hold mode until the Trigger flip flop is reset by CAMAC read (F(2)), clear LAM (F(10), Inhibit, Initialize or Clear.

5.3.3. Offset DAC

The offset DAC is a device whose function in the 3511 is to provide a variable analog offset to the ADC input, whose digital equal is then subtracted from the converted signal. The net effect is to improve the differential and integral linearity characteristics by the technique of bin-width averaging.

The offset DAC is automatically incremented after each conversion by the Q output of the LAM flip flop, AE-5, whose state changes with the last positive edge of Shift Register Clock. When a count of 383 is reached in the offset DAC Counter, it is reset to zero and the cycle continues. One LSB of the offset DAC will provide an offset equal to one half an LSB of the 13 bit output word from the ADC. In other words, the maximum offset from the DAC is comparable to 191 mV at the input of the ADC.

Should the user not wish to use the offset DAC, it can be disabled by generating a CAMAC F(9) after each read cycle of the 3511. The F(9), strobed with S1, will load zero offset into the counters.

The zero level adjust is a 22-turn front-panel potentiometer (See section 2.1.8) which provides an adjustable standing voltage at the ADC input. The offset can be varied between positive 0.50 V and negative 0.50 V.

The offset DAC output, Zero Adjust and the Track-and-Hold output are "summed" at the input to the ADC and a 13-bit word is generated proportional to the voltage seen at the ADC input.

5.4 Control and Data Processing

5.4.1

An 11-bit word format is used to write into the Storage Offset Register and Conversion Gain Counter, using CAMAC F(16), strobed with S1. The first 8 bits (W1 - W8) are used to write storage offset where W1 equals 256 and W8 equals 32K. W9, W10 and W11 are used as a binary code 1, 2 and 4 respectively to program a conversion gain from 8000 to 250 by binary increments, (1=8000, 2=4000, 3=2000, etc.) W9 - W11 are loaded into the conversion gain down counter (BE).

A minimum word of one must be written into the down counter for a conversion gain of 8000. If "n" represents the word written into the down counter, there will be n+1 clock pulses from Shift Reg. Clk. With generation of Trigger Clock (See Input Gating), the Q output of the trigger flip flop (AD-8) will go low. This edge switches the Track-and-Hold to Hold and triggers the Risetime Compensation Monostable. The monostable is adjustable through the side cover from 500 nsec to 7.5 μsec to provide adequate settling time of the Hold circuitry before conversion starts (see charts for proper ranges). The trailing edge of this pulse triggers the conversion start command for the ADC. The DAC offset word is digitally subtracted from the 13-bit converted signal and the difference is loaded into the conversion gain shift register.

ADC status is high during the time of conversion (5 μsec). The high to low transition of this signal clocks a J-K flip flop generating Shift Reg. Clk. En., (AE-9). This signal, TTL high, enables the conversion gain shift register clock (approximately 20 MHz) and generates a low at the Q output of the LOAD flip flop, (AF-8). Shift/LD remains low for the first positive clock edge and forces the 13-bit conversion data to be loaded into the Conversion Gain Shift Registers. The clock also decrements the conversion gain down counter by one.

Shift/LD is reset high after the first positive clock edge so that each successive clock edge decrements the counter and shifts the converted word down one place. When the counter reaches an underflow condition a Ripple Out is generated (BE-3) which will inhibit the clock after one more positive edge.

Six bits of the 8-bit storage offset are OR'd with the converted data at the input to the Read buffers. The two MSB's of storage offset (W7 and W8 representing 16K and 32K respectively) are wired directly into the buffers.

The switching of Shift Reg. Clk. Enable from high to low clocks the LAM flip flop (AE-5) which advance the offset DAC and, when the station N is not selected, will generate a LAM on the CAMAC dataway.

Tri-state buffers (DK, HK) are enabled with F(2) or F(0) to gate the converted data and storage offset onto the CAMAC Read lines R1 through R16.

The LAM flip flop is reset by F(2), Z or C strobed with S2.

5.4.2

The Q output of the Trigger flip flop (AD-9) is OR'd with the LLD output (optionally at ground) to provide a prompt busy (TTL high) at pin 8 of the read panel connector, J2. This signal remains high for the total time the 3511 is busy.

The Busy Out front-panel BNC can either be the prompt busy or a delayed version of the prompt busy. If jumpered for the delayed version, the prompt busy triggers a monostable (AD-2) whose delay is variable from 100 nsec to 35 μsec. The trailing edge of this pulse (AD-4) clocks the Busy flip flop (HB-9) providing a high TTL level at the Busy Out BNC.

The Trigger flip flop (A9-9) is cleared by F(2), Z or C, strobed with S2. The prompt busy and delayed busy require the trigger flip flop cleared and the input signal to be below the LLD setting (jumper optional E10 - E11) to be reset low.

5.4.3

The 3511 is disabled with CAMAC I, Z or F(24). These signals are OR'd at BF and provide a high active state at the K input of the Disable J-K flip flop, BD-12. This flip flop is clocked by Strobe S1. An open collector buffer (AL-3) inverts the Q output and is wired to pin 2 of both rear-panel connectors J2 and J3. These connectors are provided for an external Disable from, as an example, the Model 3541 dual deadtimer. The internally latched Disable prevents the operation of the Trigger flip flop (AD) until a CAMAC F (26) is given. The external Disable is a TTL level, active only when held low.

APPENDIX A
FRONT-PANEL PORT
(Models 3512 and 3515 only)

A.1 Multiple 3512(15) Operation with 3588 Histogramming Memory Module

Model 3512(15) generates a Bus Request Out signal in order to gain control of the bus for writing data to the Histogram Memory Module, Model 3588. A standard 50-conductor flat cable is used when only one ADC is in the circuit.

Multiple ADC's operating in parallel with one 3588 require a special ribbon cable which is modified to route the Bus Request signals such that multiple simultaneous requests will ripple through the ADC's giving priority to the farthest ADC from the 3588. The special cable also requires ADC identification switches to be in appropriate positions (section 2.2.5) to designate an ODD or EVEN position in the chain of ADC's. Note that when the cable is installed it is important that there are no unused connector positions between active modules.

Figure A-1 shows switch settings and typical cabling. The switch is accessible when the left side cover is removed.

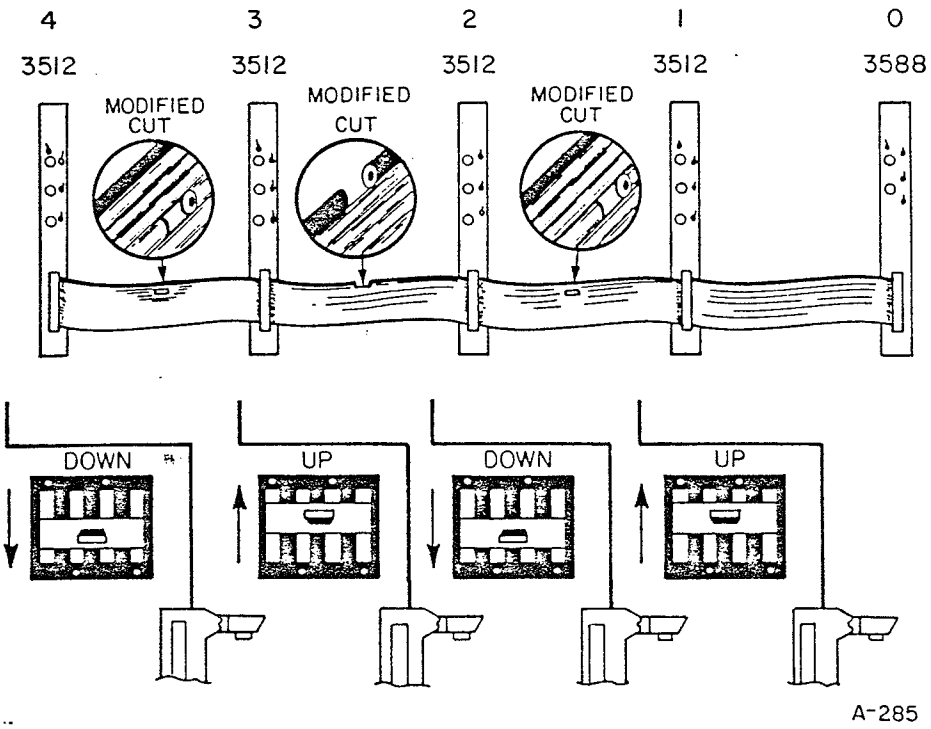

Figure A-1
Multiple 3512(15) Operation with 3588

A.2 Front-Panel Bus Control Timing

Model 3512(15)'s front-panel bus requires the timing shown in Figure A-2 for its control signals.

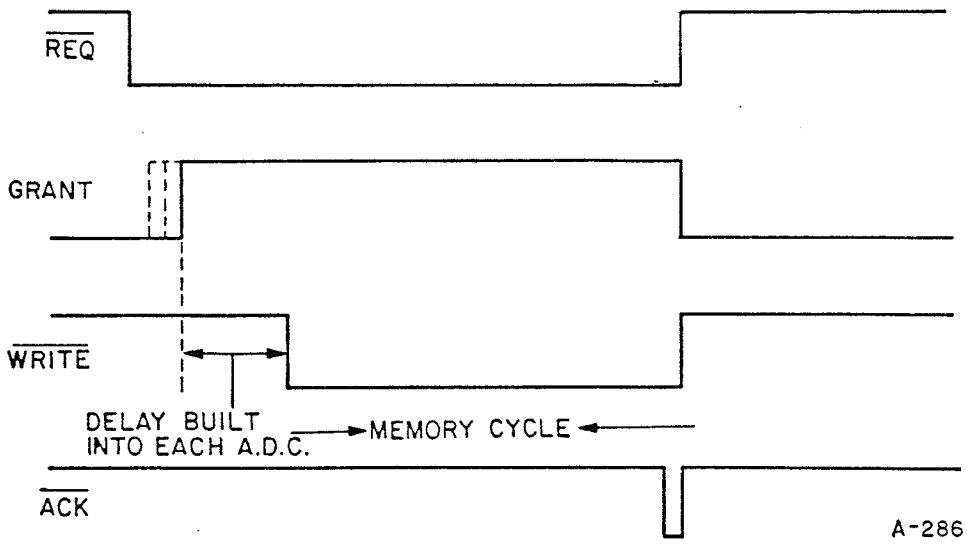

Figure A-2
Control Timing

Notes

1. Controllers respond to REQ with GRANT.

2. Controller responds to WRITE with ACK after data can be removed from bus. Data will be stable 100 nsec after falling edge of WRITE.

3. GRANT is an open-collector, wire-AND'd function; that is, when all GRANTS are asserted, the GRANT line will go high.

4. Both GRANT and ACK are gated with REQ.

5. All signals are negative logic.

6. Data lines are tri-state, positive logic.

7. ACK is open-collector, wire-OR'd.

APPENDIX B
EXTERNAL JAM VIA FRONT-PANEL CONNECTOR

A 13-bit word may be Jammed into the buffer memory of the 3512(15) to provide a delimiting word or to provide information about the experiment. The data lines are tri-state TTL signals, positive logic. Handshake signals are open collector TTL, wire-OR'd logic, except the External Write Enable line and the Jam Acknowledge which is wire - AND logic.

At the beginning of a Jam sequence, the user's module must generate an ADC gate disable and maintain this until the write has been acknowledged. By 15 µsec after this disable is generated, all 3512(15)s should have responded and the Ext. Write Enable line will be high. At this time the Ext. Jam Data Ready line can be taken high, generating a write cycle. The Jam Acknowledge line will go high when all 3512(15)s respond, signifying the end of the Jam cycle. Figure B-1 shows the timing.

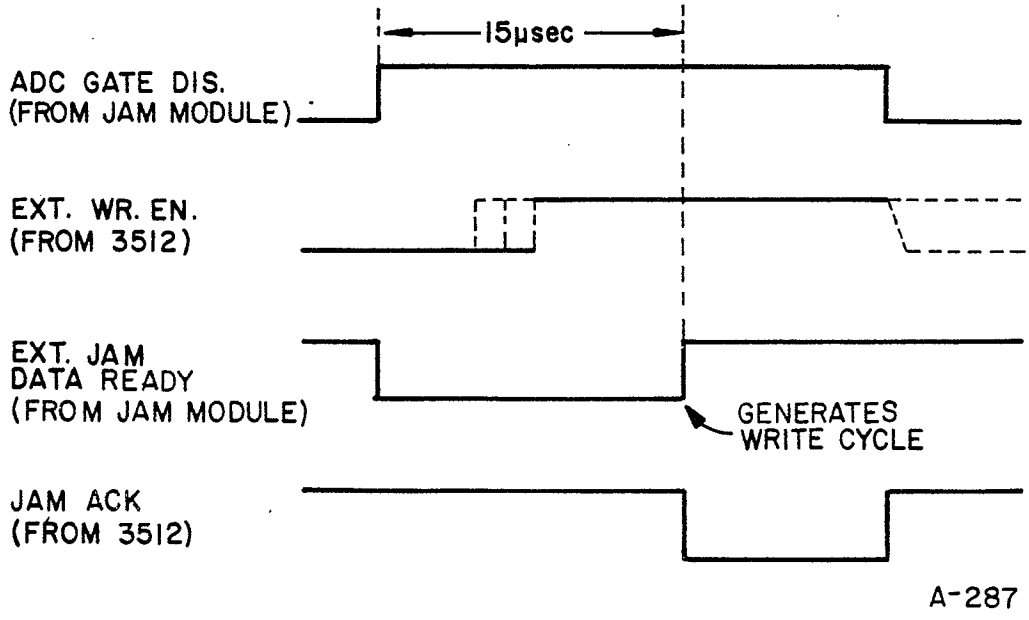

Figure B-1
External Jam Handshake Timing

APPENDIX C
ADC CONVERSION TIME CALCULATION

Conversion time for the 3510 series ADC's is dependent on a number of factors. The following outline may help in determining the actual total conversion time for any given set of conditions. Add the appropriate times listed on the right hand side of the outline to calculate the total time needed to convert a signal and be ready to accept the next signal. Space is provided at the right for copying the appropriate delays. An example is given later.

I. Conversion Triggering		
A. Peak Detect Mode (Risetime Select Switch Setting)		
a. 300 nsec to 400 nsec		150 nsec
b. 350 nsec to 1 µsec		200 nsec
c. 1 µsec to 4 µsec		600 nsec
d. 3 µsec to 10 µsec		1000 nsec
e. 7 µsec to 20 µsec		2000 nsec
B. Sample Mode		100 nsec
II. Risetime Compensation		650 nsec
III. ADC Speed	3511 or 3512	5000 nsec
	3514 or 3515	1000 nsec
IV. Gain		
A. 8000 channels (13 bits, 3511 or 3512 only)		200 nsec
B. 4000 channels (12 bits)		300 nsec
C. 2000 channels (11 bits)		400 nsec
D. 1000 channels (10 bits)		500 nsec
E. 500 channels (9 bits)		600 nsec
F. 250 channels (8 bits)		700 nsec
V. ADC Readout Mode (applies to 3512 or 3515 only)		
A. With 3588		1500 nsec
B. With internal buffer		570 nsec
(time to LAM ... 630 nsec)		

For example, assume that a 3512 is being used with a 3588. The 3512 is programmed for a gain of 8000 and is set for the fastest possible risetimes. Then . . .

Factor	Time
Conversion triggering	150 nsec
Risetime compensation	650 nsec
ADC speed	5000 nsec
Gain	200 nsec
Readout Mode	1500 nsec
Total	7500 nsec = 7.5 μsec

NOTE: Times listed are typical and may vary from unit to unit.