CAMAC ECLINE
MODEL 4508

DUAL 8-INPUT/8-OUTPUT
FULLY PROGRAMMABLE LOGIC UNIT

USER'S MANUAL

September 1980

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

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and use of LeCroy equipment are available from the Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499 (914) 578-6059, or your local field service office.

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LeCroy offers a selection of customer support service. For example, Blue Ribbon service provides guaranteed three-day turn around on repairs, a direct access number for product application assistance, yearly calibration and the addition of engineering improvements. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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- Copy the software for backup or modification purposes in support of your use of the software on a single machine.

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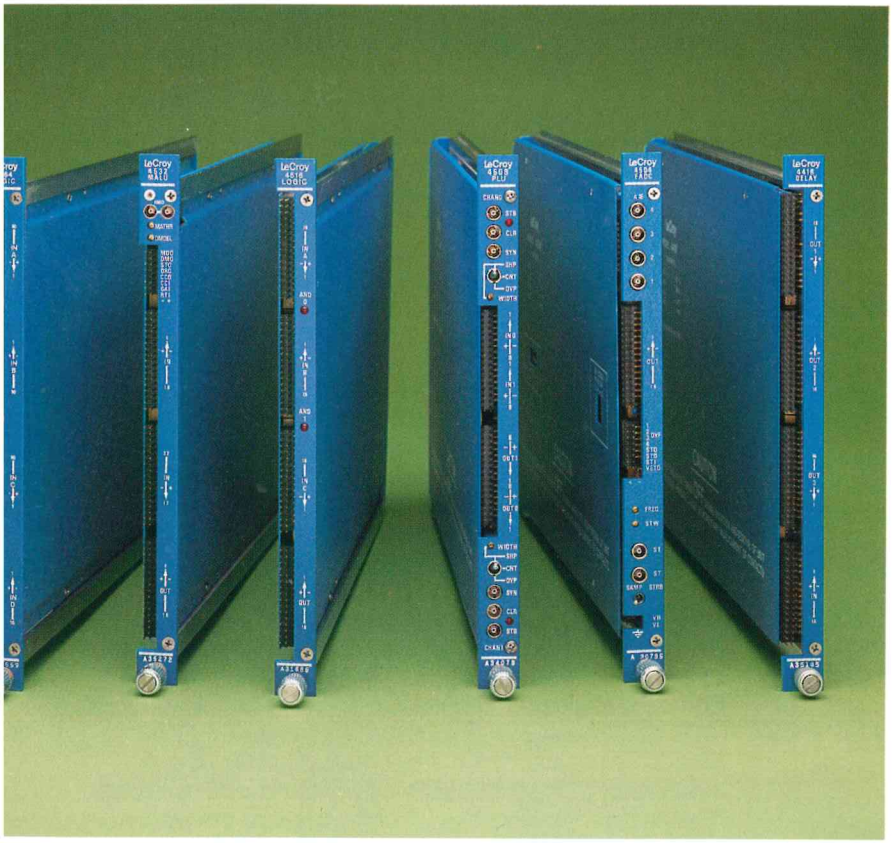
ECLine PROGRAMMABLE LOGIC
FIRST LEVEL TRIGGER MODULES

LeCroy

4418 PROGRAMMABLE LOGIC DELAY/FAN-OUT
4504 FLASH ADC
4508 PROGRAMMABLE LOOKUP UNIT
4516 PROGRAMMABLE LOGIC UNIT
4532 MAJORITY LOGIC UNIT
4564 OR LOGIC UNIT



- **High Speed First Level Trigger Decisions**
- **Programmable Logic Functions**
- **Compatible with ECLine Data Handler Modules**
- **Compatible with ECLine Discriminators, ADC/TDC, and MWPC Systems**
- **Designed-in Expandability**

FAST, FIRST LEVEL TRIGGER PROCESSING

The LeCroy ECLine family of programmable logic modules include logic delays, Boolean logic and other functions vital for high speed trigger systems. It also includes fast table lookup permitting pre-programmed responses to digital data. Functions are performed in only a few tens of nanoseconds, permitting data to be screened prior to recording and increasing the sensitivity of the experiment.

FEATURES

High Speed - Maximum rates of 65 to 150 MHz , depending on module and programmed features.

Multiple Functions - Relative timing adjustable by programmable logic delay, Majority Logic and simple Boolean Logic (AND/OR) for coincident events, Programmable lookup for complex functions.

Fan-Out Capability - Use of ECL (Emitter Coupled Logic) levels provides outputs suitable for fan-out to several modules (termination resistors may need to be removed on inputs).

Use of Multichannel Differential ECL - Signals for economic, fast, noise immune interconnections.

FUNCTIONAL DESCRIPTION

LeCroy's ECLine family of programmable logic modules are designed to quickly characterize data so that a rough go/no-go decision can be made for further processing. For example, discriminators are employed to ensure that analog signals are of sufficient amplitude to be interesting, and to provide logic outputs of fixed duration. This stage is then followed by a coincidence latch which records the pattern of "interesting signals" that occur within the same time window. The First Level Trigger modules ensure that specific combinations of signals have occurred. (Information on Discriminators and Latches may be found on other ECLine Programmable Logic Data Sheets.)

This first stage of data handling can then either reject the event as uninteresting, or can pass data on for further processing. The more sophisticated line of ECLine Data Handling modules include data conversion, arithmetic operations, fast "do loop" type operations, and specialized pattern recognition/ interpretation. Information on LeCroy Data Handling modules may be found on the Data Handlers technical data sheet. All functions are programmable to provide complete computer control of the triggering and data acquisition systems.

The LeCroy ECLine modules are compatible with the sophisticated FERA (Fast Encoding and Readout ADC) analog and time interval digitizing systems, as well as with the PCOS III Multiwire Proportional Chamber System. For exceptional data rates and on-board event accounting, the ECLine modules are also compatible with the LeCroy FASTBUS Multiple Event Buffer Memory, Model 1892. This compatibility provides a convenient method of storing data from ECLine modules, combining data from ECLine and FASTBUS (IEEE-960) systems, and provides the exceptional speed and data handling capability of the FASTBUS Standard.

Model 4418
Logic Delay/Fan-Out

Fast, passive logic delays are of prime importance for allowing all signals to arrive simultaneously at a data acquisition module. The LeCroy Model 4418 has 16 passive, tapped delay lines, one for each input. Each delay is individually set by computer via CAMAC in 1, 2 or 4 nsec increments (depending on sub-model or "MOD" selected), over a range of fifteen increments. The selection directs an output to "view" a particular tap on the delay line. For example, this feature would give the user a means of accurately aligning signals in time to compensate for differences in cable lengths.

Deadtimeless operation at speeds up to 100 MHz is assured by using passive delay lines and ECL switches. This feature provides the reliability of cable delays together with the speed and fan-out of ECL circuitry. As an added feature, each output is present three places on the front panel to provide additional fan-out capability. The cost of this device rivals cable delays.

Model 4504
Flash ADC

Four independent 4-bit (plus overflow) Flash ADC's are incorporated in the Model 4504. The sampling rate is adjustable from 20 to 100 MHz via front-panel control. Alternatively, a front-panel strobe input can be used to externally control the sampling rate.

The 4-bit ECL outputs are accompanied by a strobe output signal to indicate that the outputs are valid. This feature provides a convenient means to strobe subsequent logic (for example, the Model 4508 Programmable Logic Unit) that uses the Flash ADC results. A front-panel VETO input is provided for disabling the unit during periods when no input data can be processed.

The most common use of the 4504 is as a multiple threshold discriminator . The input may be derived directly from the detectors themselves or the analog outputs of other ECLine modules (Model 4532 for example).

Model 4508
Programmable Lookup Unit

Two independent 8-bit Programmable Lookup Units (PLU's) are included in the Model 4508. Each unit has an 8-bit digital input and an 8-bit digital output. The unit functions as an 8-bit addressable RAM. The contents are pre-programmed via CAMAC by the user. Each 8-bit input is a RAM address, and each 8-bit output is the content of this addressed location.

Output patterns are programmed into the PLU for each of the 256 possible input patterns. This unit can act as a complex logic module , a programmable calibration unit, or it may control the actions of subsequent logic based on the input pattern and programmed lookup table.

Each section of the Model 4508 can operate in one of three modes: Shaped, Overlap or Continuous. In the Shaped Mode, the outputs are a pulse of duration set by a front-panel adjustment. The inputs must be accompanied by a front-panel Strobe input signal . In Overlap Mode, the output pulse width (on all 8 bits) equals the input width if the Strobe input signal arrives before the input. Finally, in Continuous Mode, the output width reflects the time coincidence between Strobe and the inputs pulses.

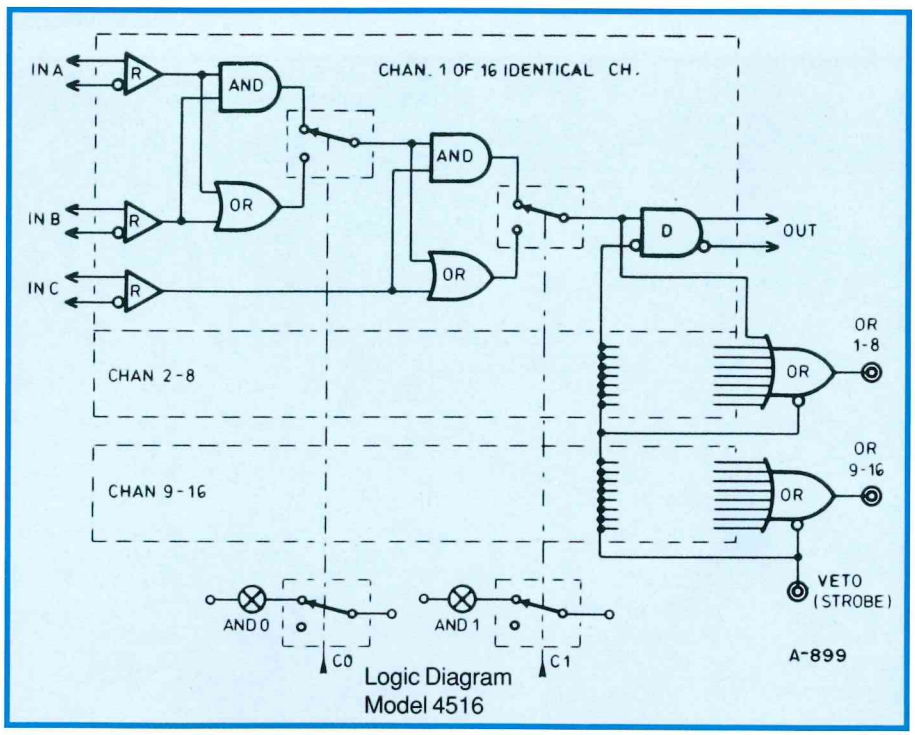
Model 4516
3-Fold AND/OR Logic Unit

Each of the 16 channels of the Model 4516 has three inputs (A, B and C). All channels have a front-panel output that is one of the Boolean combinations: (A•B•C), (A+B)•C, (A•B)+C, or (A+B)+C. The choice of logical function, AND(•) or OR (+), is set for all channels by two switches. These switches are set either by rear-panel manual switch settings or by computer command via CAMAC.

The 150 MHz speed of Model 4516 lends great versatility to this simple module. It can be used as a front-end AND/OR logic module, or an integral component in a higher level trigger processor.

Model 4532
Majority Logic Unit

Experiments that require a minimum number of signals to be present need a Majority Logic Unit. Each of the 32 inputs of the 4532 that is in a logical 1 state gives an incremental increase in a current sum output. An



Logic Diagram
Model 4516

onboard discriminator may then be used to signal when a user set current threshold (multiplicity) is exceeded. The current sum of each 4532 is available on two bridged outputs than permit daisy chaining of several modules. This feature extends the useful number of input sums by 32 inputs per daisy-chained module. For dynamic sampling, the analog output may be connected to an input of the Model 4504 Flash ADC. This unit provides a 4-bit digital output useful for trigger processing circuits.

The status of up to 32 inputs can be monitored and recorded by issuing a strobe. Since the inputs are edge-triggered, the strobe may be a gate of arbitrary duration. Then any inputs which are on during any portion of the gate are recorded and stored in a pattern register. The pattern register can then be read by computer via CAMAC. Alternatively, the 4532 can operate in Overlap Mode where the input pattern is not latched, and the outputs follow the inputs dynamically.

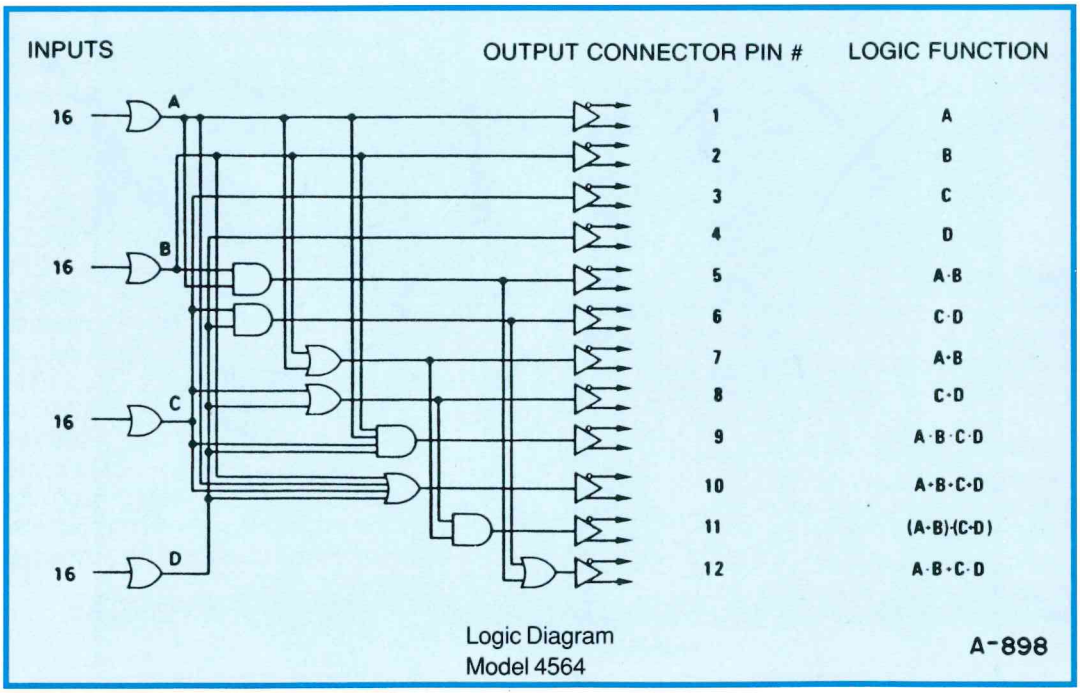
Other features of the Model 4532 are fast OR'ing of adjacent inputs, cluster mode operation, and provisions for cascading several 4532s for use in large detector arrays. Sixteen front-panel outputs give a fast OR output of inputs 1 and 2, 3 and 4, etc. These outputs reduce the number of signals that a second level trigger processor must view, while still maintaining a segmented set of signals. Next, in Cluster Mode, the 4532 will assume that adjacent hits indicate a single event and present only a single increment to the current output. This feature is useful in wire chambers where the close wire spacing often results in two or more adjacent wires giving signals from a single track. Finally, there is a provision for cluster Carry In and Carry Out to permit cascading several modules and permit cluster mode operation across module boundaries.

Model 4564
16 to 64 Fold OR Logic Unit

The Model 4564 is a simple and versatile logic module. It consists of four groups (A,B,C and D) of 16 input OR's followed by a set of additional 2 fold and 4 fold OR and AND functions. These various logic outputs, shown pictorially below, are simultaneously available on a rear-panel connector and the transit time is independent of the function. In addition, the outputs are capable of rates in excess of 100 MHz. Output width is dependent on the input pulse overlap.

For greater flexibility, the 4564 also offers four discriminator/ shaper channels. Internal jumpers allow any of the 12 logic combinations to be input to these channels. The output of discriminators/shapers can be triggered on the leading or tailing edge of the input (jumper selectable) and the width is adjustable from 15 nsec to greater than 500 nsec. Output polarity is also selectable via internal switches. These outputs can be used simply as an adjustable width logic fan-out or can allow for more sophisticated functions.

A typical application of the 4564 is to perform a simple track or pattern recognition for Veto or gate applications.



Logic Diagram
Model 4564

SPECIFICATIONS

Model 4418
Programmable Logic Delay/Fan-Out

Inputs: 16, DC coupled 100 Ω impedance, on 34-pin header for ECL signals. 100 MHz maximum rate (>35 MHz for Long Range Option), <10 nsec double pulse resolution (<30 nsec for long range option). Minimum width: 5 nsec.

Delay: 15-30 nsec in 1 nsec steps (4418/16), 15-45 nsec in 2 nsec steps (4418/32),15-135 nsec in 8 nsec steps (4418/128): Long Range Option. Delays set by computer for each channel individually.

Outputs: Three for each input, on three 34-pin headers, for compatibility with complementary ECL devices. Width equal to input duration ±1.2 nsec (±4 nsec Long Range Option). Risetime and falltime: 2.5 nsec.

Battery Back-Up: Preserves stored delays for at least 2 hours in the event of power loss.

Crosstalk: Synchronous pulses in adajcent channels can be affected by ±1 nsec typical.

Power: +6 V/50 mA, –6 V/2.5 A (15.3 W total)

Model 4504
Flash ADC

Inputs: Four on coaxial connectors, 50 Ω impedance, 10 nsec minimum width. Analog input range user defined between –2.5 V and +2.5 V. Range, set by computer command by giving low and high voltage reference levels, is divided by 15 to obtain resolution (4 bits).

Strobe: One ECL input for external strobe selected by front-panel switch. Leading edge initiates digitizing of all four inputs simultaneously; falling edge transfers digitized values to outputs and holds until next strobe. Maximum frequency 100 MHz. Alternate switch setting provides internal 20 MHz-100 MHz free-running strobe. Internal strobe frequency set by front-panel adjustment.

Veto: One ECL input inhibits strobe signal.

Outputs: Four, 4-bit ECL outputs on 8-pin headers. Overflow bits provided on 4 two-pin headers.

Strobe Out: Two on two-pin headers (ECL pulses) and two on Lemo connectors (–600 mV pulses) timed with digital outputs for downstream logic. Width is adjustable by front-panel potentiometer in the range of 5 to 25 nsec.

Test Points: Two front-panel test points permit measurement of voltage reference levels.

Input-Output Delay: Strobe trailing edge to digital outputs, typically 15 nsec.

Power: +6 V/1.1 A, –6 V/1.5 A, +24 V/6 mA (15.7 W total)

Model 4508
Memory Lookup Unit

Inputs: Two, 8-bit inputs on 34-pin header, 100 Ω for complementary ECL. Minimum width 10 nsec, maximum rate 65 MHz.

Strobe: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires –600 mV signal, 5 nsec minimum width and must precede input by 2 nsec for exact time coincidence. Latches inputs, except in overlap mode. Maximum frequency >65 MHz. Strobe must be followed by clear except in Overlap Mode.

Clear: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires –600 mV signal, 5 nsec minimum width to clear. Clears pattern register and resets outputs in all modes.

Outputs: Two, 8-bit outputs on 34-pin headers, ECL signals. Width of output in Shaped mode set by front- panel adjustment between <5 nsec to >100 nsec.

Synchro Output: Two on Lemo connectors, one per output section, 50 Ω impedance. Supplies –600 mV pulse out when outputs are ready. Typically used for strobing next unit, or for self-clearing.

Modes: Overlap (OVL) - Output pulse width determined by coincidence between Inputs and Strobe.

Shaped (SHP) - Output pulse width is determined by a front - panel adjustment from <5 to >100 nsec. The unit must be cleared before another input can be latched.

Continuous (CNT) - Output state is latched by the Strobe, until a Clear is applied.

Propagation Delay: (17 ±3) nsec in Overlap Mode. In other modes (21 ±1) nsec independent of logic function and determined by Strobe timing.

Power: +6 V/0.5 A, –6 V/2.6 A (18.6 W total)

Model 4516
Programmable Logic Unit

Inputs: 16 sets of three inputs, 100 Ω (high impedance by removal of socketed terminators), DC coupled, on 34-pin headers, for ECL signals, minimum 2 nsec risetime. Maximum rate 150 MHz.

Veto: One rear-panel Lemo connector, 50 Ω impedance. Requires –600 mV signal. Permits gating of outputs, including OR outputs. Must overlap coincidence for the three front-panel inputs by >5 nsec.

Outputs: 16, one per set of three inputs, complementary ECL logic levels on 34-pin header.

OR Out: Two, one for OR of first 8 outputs, one for second 8 outputs (factory option permits OR'ing of all 16 outputs).

Double Pulse Resolution: 5 nsec at minimum input width.

Coincidence Width: >3.5 nsec determined by input pulse width.

Input-Output Delay: A or B to OUT by 11 nsec typ.; A or B to OR by12 nsec, typ.; C to OUT by 8 nsec, typ.; C to OR by 9 nsec typ.; VETO to OUT by 8 nsec typ.; VETO to OR by 6 nsec typ.

Power: +6 V/50 mA, –6 V/1.25 A (7.8 W total)

Model 4532
Majority Logic Unit

Input : All inputs accept differential ECL level (–0.8 V, –1.7 V) into 110 Ω input impedance (high input impedance is possible by removing socket-mounted terminators).

Data Input (IN): 32 in two 34-pin front-panel connectors; minimum input pulse width 6 nsec.

Reset Input (RTI): Fast reset of the input registers; generates a reset of the analog majority output and of the comparator outputs (MDO, DMO). When the analog output is cascaded with other units, the RTI resets only the contribution from the modules that received the RTI. Minimum input pulse width 6 nsec, maximum width DC. In Memory Disable mode, the RTI is inhibited.

Gate Input (GAI): Normally open when unconnected. Normally closed when connected to a cable providing standard ECLine levels. In Memory Disable Mode, data pulses having an overlap with the GAI will contribute to the outputs. In Memory Enable Mode, data pulses having their leading edge inside the GAI time will be accepted and stored. By deriving the GAI from the DMO, an internally generated time window is possible. Minimum overlap time width with input pulses for majority decisions, 10 nsec. Minimum overlap time width with input pulses for logical OR's, 3 nsec, maximum width DC.

Cluster Carry (CCI): When Cluster Selection is Enabled, receives the carry information on the cluster from the Cluster Cary Output (CCO) of any adjacent majority logic unit.

Analog Majority Inpt/Output (AMIO): High impedance current source; AMIO connectors can be used for daisy chaining of analog majority information within a unit. Transit time between AMIO connectors 2 nsec. Unused output must be terminated with 50 Ω.

Output: All logic outputs provide complementary ECL levels (–0.8 V, –1.7 V) and are capable of driving differential 110 Ω loads.

Data Outputs (OUT): 16 in a 34 pin front-panel connector. In Memory Disable Mode, provides pulses corresponding to an overlap coincidence between the gate pulse and the data inputs. In Memory Enable Mode, provides levels started by the coincidence between the gate pulse and the leading edge of the data pulses.

OR Output (ORO): Provides the logical OR of the 32 channels, otherwise behaves as data outputs.

Strobe Output (STO): Provides a pulse, suitable for strobing of subsequent logic units, at the end of the gate input and delayed by the internal transit time (6 nsec). Width adjustable from 10 to 25 nsec by a trimmer (STROBE WIDTH) accessible from the side of the module.

Majority Discriminated Output (MDO): The AMIO input/output is internally used as input to an adjustable threshold comparator providing the MDO output. Threshold adjustable from 1 to 16 hits by a front-panel potentiometer (MA THR). The output will be a pulse or a level depending on the selected operating mode.

Delayed Majority Output (DMO): Reproduces the output MDO above, after an adjustable delay. A switch on the side of the module (DM RANGE) selects one of two delay ranges; 10-100 nsec or 50-1000 nsec. A front-panel potentiometer (DMO DELAY RANGE) permits continuous adjustment. The DMO is cleared as soon as the MDO is cleared.

Cluster Carry (CCO): When Cluster Selection is Enabled, indicates that Output channel 32 was hit for use in conjunction with channel 1 of a logically adjacent cluster logic in another 4532 module (CCI) input.

Mode Selection: A Memory Enable switch, accessible on the side of the module, selects one of the following modes: Memory Disable - Functions are disabled; the multiplicity calculation is performed on theoverlap of the data inputs. Memory Enable - The data inputs are latched; the multiplicity is determined by the number of leading edges of data input pulses occurring during the gate time. In this mode the unit needs to be cleared either by the reset input (RTI) or by a resetting function.

Cluster Slection: The Cluster Enable switch, accessible on the side of the module, determines one of the two following modes: Cluster Disable - Each data input provides one hit on the Analog Majority Output AMIO; the Cluster Carry Input (CCI) is disabled; Cluster Enable - Any group of adjacent input data pulses will be considered as a single hit. Provision has been made for the clusters to extend beyond the 32 inputs. If an input is present on the logically adjacent channel to input 1 of this unit but is located in another unit, the CCI can be used to indicate its presence. The CCO of this module indicates that channel 32 of this module is present.

Input-Output Delay: Data IN to AMIO - 16 nsec; AMIO to MDO output - 5 nsec; End of gate IN to Strobe OUT by 6 nsec; Data IN to Data OUT by 12 nsec; Data IN to OR OUT by 16 nsec; Reset IN to Data OUT by 20 nsec; Reset IN to OR OUT by 24 nsec; Data IN 32 to Cluster Carry OUT by 11 nsec; Cluster Carry IN to Data IN 1 by 2 nsec. Gate pulse must precede Data pulse by at least 7 nsec.

Power: +6 V/200 mA, –6 V/<3.6 A, +24 V/ 5 mA, –24 V/7 mA (23 W total).

Model 4564
16 to 64 Fold OR Logic Unit

Inputs: 64 in four 2 x 17 front-panel connectors, 110 Ω impedance. Minimum width 6 nsec, maximum frequency >100 MHz.

Overlap Outputs: Rear-panel 2 x 17 pin connector, pins 1 to 12, ECL signals. Width corresponds to overlap (±2 nsec) of inputs of logic function, minimum output 5 nsec, maximum output frequency >100 MHz; transit time 12 nsec ±1 nsec typical, independent of logic function; double pulse resolution 10 nsec typical.

Shaped Outputs: Rear-panel connector pins 13 to 16, any of overlap logic can be converted via jumper option to any of the four discriminator/shapers, output is differential ECL levels and width is internally adjustable from 15 to >500 nsec, can be triggered in leading or trailing edge of inputs (jumper selectable); output polarity internally switch selectable; maximum frequency: 30 MHz, double pulse resolution: 33 nsec.

Power: +6 V/150 mA, –6 V/1.5 A, –24 V/20 mA (10.4 W total)

CAMAC COMMANDS, FUNCTION CODES AND RESPONSES

Model 4418 Programmable Logic Delay/Fan-Out

F16•(A0 to A15):	Load delay time setting on write lines W1 to W4. One subaddress for each channel.
X, Q:	An X and Q response are generated when a valid N, A, F command is recognized.

Model 4504 Flash ADC

F(0)•A(0):	Read digital outputs; R1 to R16, 4 bits per channel.
F(0)•A(1):	Read digital overflow, R1 to R4, 1-bit per channel.
F(16)•A(0):	Write Low Reference Voltage (VL) on 8 bits; range from –2550 mV to +2250 mV in steps of 20 mV.
F(16)•A(1):	Same as above but for the High Reference Voltage (VH).
F(25)•A(0,1):	Equivalent to C.
C:	Generates a strobe during S2 time. This function is not affected by I or VETO input and may be disabled by a side-panel switch. The digital outputs will be set depending on the analog value of the inputs; in particular, if the inputs are disconnected all the digital outputs will correspond to 0 V at the inputs. The output logic state will be determined by the VL and VH reference voltages.
I:	Inhibit strobe.
X, Q:	X=1 and Q=1 responses are generated for any of the above functions.

Model 4508 Programmable Lookup Unit

F(0)•A(0):	Read first section 8-bit input pattern.
F(0)•A(1):	Read second section 8-bit pattern.
F(0)•A(2):	Read first section memory content at the given address; the memory content is displayed on read lines R1-R8, the given address on read lines R9-R16.
F(0)•A(3):	As F(0)•A(2) but for the second section.
F(2)•A(0):	Read first section 8-bit pattern and reset at S2; reset output levels when operating in continuous mode.
F(2)•A(1):	Same as F(2)•A(0), but for the second section.
F(2)•A(2):	Read first section memory content at the given address (as for F(0)•A(2)) and increment address by one at S2.
F(2)•A(3):	Same as F(2)•A(2), but for the second section.
F(9)•A(0):	Clear first section pattern; reset first section output levels when operating in continuous mode.
F(9)•A(1):	As above, but for the second section.
F(9)•A(2) or F(9)•A(3):	Reset memory address in both sections.

F(16)•A(0):	Load first section memory content at the given address; data have to be sent on write lines W1-W8;
F(16)•A(1):	As above, but for the second section.
F(16)•A(2):	Random access to the first section memory (the selected address has to be sent on write lines W9-W16); load memory content with data present on W1-W8, at the selected address.
F(16)•A(3):	Same as above, but for the second section.
F(18)•A(0):	Load first section memory content, at the given address, with data present on W1-W8; increment address by 1.
F(18)•A(1):	As above, but for the second section.
F(18)•A(2) or F(18)•A(3):	Load the memory's address register (this address has to be sent on write lines W9-W16).

Z or C:	The address register for the memories of both sections is set to 0; pattern registers are cleared.
X:	An X=1 response is generated for any valid CAMAC function.
Q:	A Q=1 response is generated for any valid CAMAC function, except when the memory addresses overflow. (This latter feature permits one to recognize when the reading or the loading of a memory has been completed).

Model 4516 Programmable Logic Unit

F(26)•A(0):	Sets all C0's to AND Mode.
F(24)•A(0):	Sets all C0's to OR Mode.
F(26)•A(1):	Sets all C1's to AND Mode.
F(24)•A(1):	Sets all C1's to OR Mode.
F(27)•A(0):	Gives a Q response if C0 switch is in AND Mode.
F(27)•A(1):	Gives a Q response if C1 switch in in AND Mode.

X:	An X response is generated when avalid N, A, F command is recognized.
Z:	Sets all channels to OR Mode.

Model 4532 Majority Logic Unit

F(0)•A(0), A(1):	Read input pattern. A(0): channels 1 to 16. A(1): channels 17 to 32. A Q response is generated in Memory Enable Mode only.
F(1)•A(0):	Read status register; R1 = 1 if LAM isON; R2 = 1 if LAM Enable switch is ON; R3 = 1 if MEMORY Enable switch is ON; R4 = 1 if CLUSTER Enable switch is ON. Q response is always generated.
F(2)•A(0):	Read input pattern, channels 1 to 16. Q response is generated in Memory Enable Mode only.
F(2)•A(1):	Read input pattern, channels 17 to 32, and clears the 32-channel memory and LAM at S2. Q response is generated in Memory Enable Mode only.
F(8)•A(0):	Test LAM; a Q response is generated if L is ON.
F(9)•A(0):	Clears the data memory and LAM.
F(10)•A(0):	Test and clear LAM, clears LAM . Q response is generated if L is ON. The clear LAM operation is not executed if Q response is missing.

Z, C:	Clears data memory and LAM .
L:	A Look-At-Me signal is generated (in Memory Enable Mode only) at the end of the gate input if the OR output is set. The LAM may be enabled or disabled by the LAM enable switch accessible on the side of the module.
X:	An X=1 response is generated for any executable function.
Q:	A Q=1 response is generated for any executable function in Memory Enable Mode only.

Model 4564 OR Logic Unit - The Model 4564 does not utilize CAMAC Commands or Function Codes.

LeCroy

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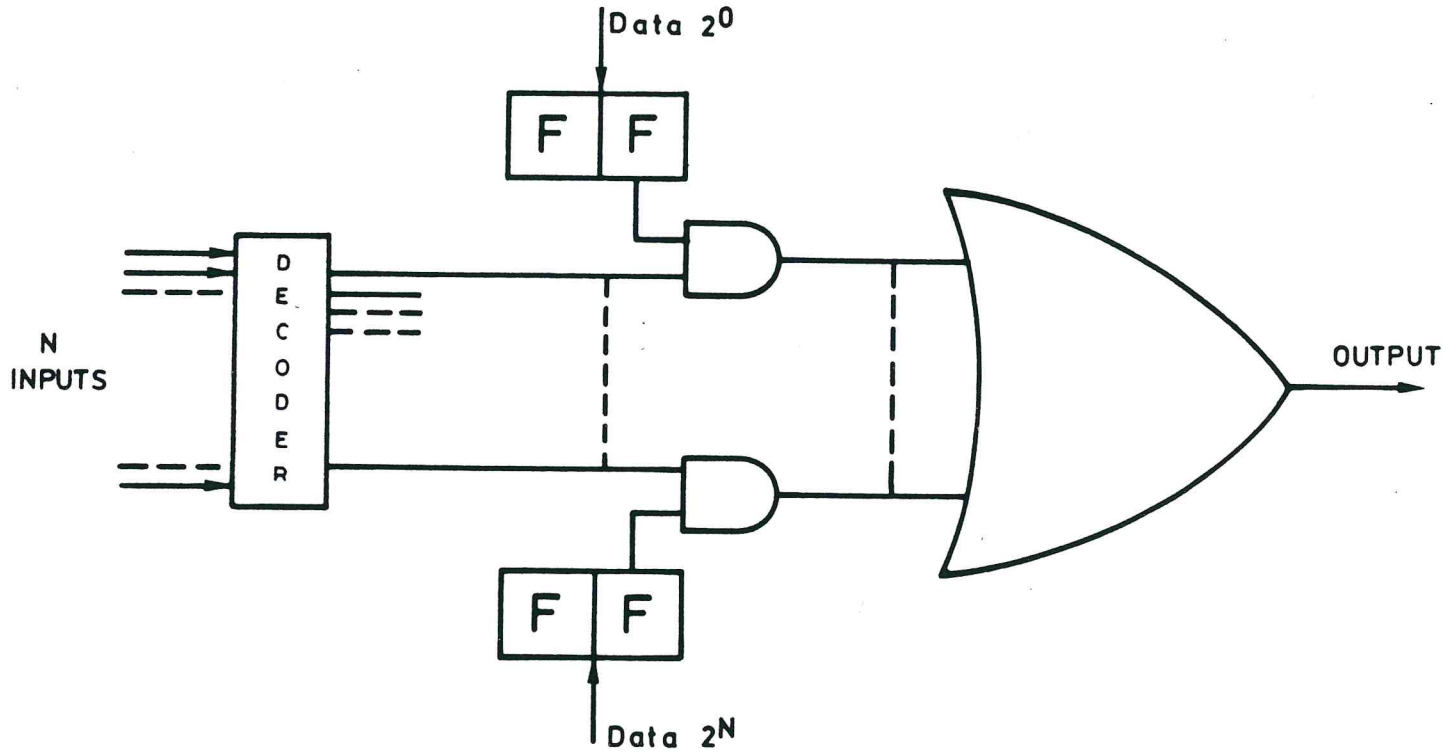
A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LIST ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N


Data 2^0
F F
D E C O D E R
N INPUTS
OUTPUT
F F
Data 2^N

CIRCUIT DESCRIPTION

INTRODUCTION

Each of the two identical units in the module can be logically divided into two main sections: one for the CAMAC handling of the module, the second for its normal running.

These two main sections have part of the circuitry in common, mainly the memories, but while one section is working, the other is automatically disabled.

CAMAC HANDLING SECTION

Purpose of this section is:

- Loading of RAM's with the proper content, that is loading of the program for the right execution of the wanted logic function;
- Reading back of RAM's content in order to compare it with the foreseen content and verify then that the program actually loaded is the correct one.
- Reading of the input pattern, once this has been latched by a strobe pulse.
- Moreover CAMAC commands and functions are provided for resetting and initializing purposes.

LOADING OF RAM's

The eight bit word generating the RAM address is provided by an eight bit counter (IC: 410, I10) which is common to both sections of the module.

This counter can be reset by the CAMAC commands C or Z or by the function F(9)·A(2)(F(9)·A(3)).

The counter, and hence the RAM address, is increased by one every time a F(0)·A(2)·S2 (F(0)·A(3)·S2) or a F(18)·A(0)·S2 (F(18)·A(1)·S2) are generated.

Moreover a random address can be generated by loading into the counter, through the parallel load, the content of write lines W9 - W16, using F(18)·A(2)(F(18)·A(3)) or F(16)·A(2)·S1 (F(16)·A(3)·S1). Data loading into a particular RAM address, specified by the counter, occurs during F(16)·A(0) (F(16)·A(1)) or F(16)·A(2)·S1 (F(16)·A(3)·S1) or F(18)·A(0)·S1 (F(18)·A(1)·S1).

Data to be loaded have to be set, in all cases, on write lines W1 - W8.

The different possibilities of data loading have been foreseen in order to cover a complete range of needs. In particular F(16)·A(0)(F(16)·A(1)) makes loading at the address already present;
F(16)·A(2)(F(16)·A(3)) select the RAM address and loads data on it.
F(18)·A(0)(F(16)·A(1)) loads data at the address already present and then increments the address by one.
F(18)·A(2)(F(18)·A(3)) is just a random selection of the address.

Normally, in order to load a complete program into the RAM's one has first to select address zero through C or Z or F(9)·A(2)(F)9)·A(3)), then make a loop of the address from O to 255 using F(18)·A(0)(F(18)·A(1)) for the second section in the module to load data and automatically increment the address.

In the transition from address 255 (all addresss bits equal to one) to address 0 (all address bits equal to zero) no Q response is generated. This can be used as an easy way to check whether the RAM's addresses have been completely scanned.

In the following the reader will find examples of computer programs for particular applications.

READING BACK OF RAM's CONTENT

Reading back of the memories is useful in order to verify the correctness of the program loaded. On the other hand, periodical check of the memory content will prevent from memory failures as well as it will warn against power failures.

The memory content can be read through F(0)·A(2)(F(0)·A(3))or F(2)·A(2)(F(2)·A(3)).

F(0) performs just a reading out of a memory location previously addressed while F(2) reads a memory location previously addressed and, at S2, increments the address of one.

In both cases the word read contains the address in the second eight bits and the memory content in the first eight bits. A standard read procedure demands. first a reset of the address through C or Z or F(9)·A(2)(F(9)·A(3)) and then loop on F(2)·A(2) (or F(2)·A(3) for the second section) 256 times.

Also when reading, no Q response is generated when transition from address 255 to address 0 happens, X = 1 response is on the contrary always generated.

READING OF INPUT PATTERN

The input configuration of pulses at the input is latched in correspondence of any strobe pulse. The latching is performed by IC C4, C5 (C6, C7). Reading of the latch content can be performed via CAMAC using F(0)·A(0)(F(0)·A(1)) or F(2)·A(0)(F(2)·A(1)). F(0) performs just the reading out of the latch content, F(2) reads during S1 and clears latches during S2. In both cases the latch content is displayed on read lines R1 - R8.

The pattern can be also cleared by C or Z or F(9)·A(0) for the first section, F(9)·A(1) for the second section, or finally by a fast clear on the front panel.

RUNNING IN NORMAL CONDITIONS

It should be stressed that the running with external pulses it's only possible when the module doesn't receive a CAMAC N. The running with external pulses should start once the module has been loaded with the appropriate program. The ECL inputs, with their configuration, realise an address for the RAM's. The RAM output will be then the content of that address, which has been previously loaded.

Three operation modes have been included in the module, that is overlap (OVP), shaped (SHP) and continuous (CNT), to make it the most flexible.

Any strobe pulse, whichever operation mode has been chosen, performs coincidence with the inputs. The logic result of this coincidence is latched and it is readable via CAMAC.

INPUT CIRCUITRY

The complementary ECL input pulses are terminated at the input with 2 x 56 Ω resistors. The resistors are grouped in single in line hybrid circuits on sockets. They are then remouvable if high input impedance is needed.

The line receivers accepting the input pulses, IC A4 and A5 (A6, A7), transmit pulses to an AND gate, IC B4 and B5 (B6, B7), which is normally open, and it is closed as soon as a strobe pulse or an active CAMAC cycle arrives. The outputs of these gates go directly to provide an address to the memories, IC E1O, D1O (E8, D8). If a strobe occurs, its leading edge will freeze the memory address at the level of IC's C4, C5 (C6, C7). The address will remain then constant, until a next clear will occur, either by the front panel clear input, or by a suitable CAMAC operation.

INPUT PATTERN

As mentioned above, the leading edge of a strobe pulse generates a latching of the input configuration into IC's C4, C5 (C6, C7). The input pattern is stored there and it is readable via CAMAC as soon as gates E4, E5 (E6, E7) are gated by a suitable CAMAC function.

An important consideration is that the latches storing the input configuration are in series, and not in parallel, with the address lines. So that strictly the same input configuration is stored into the latches and at the same time is responsible for the outputs.

OUTPUT CIRCUITRY

The memory outputs are going to the final outputs only passing through a final gate, IC A11, A10 (A9, A8).

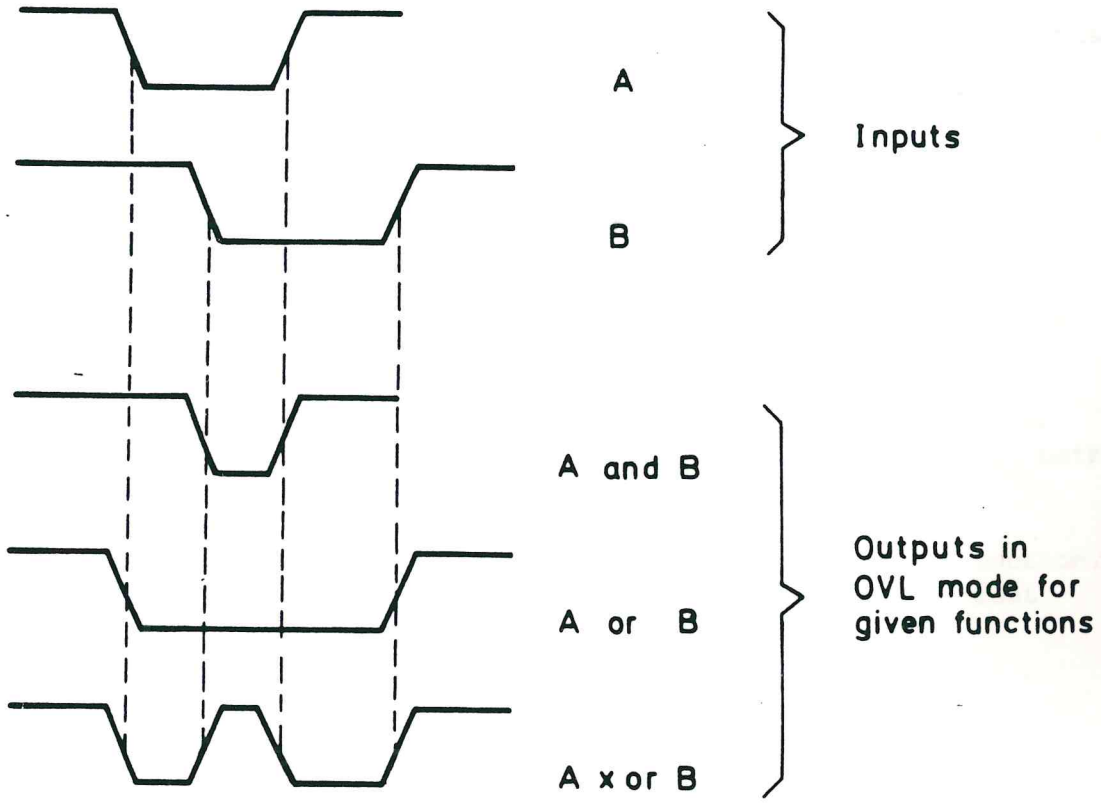
The way to enable these final gates depends on the chosen operation mode. They are always enabled in overlap mode; they are anabled during a fixed time in shaped mode, in order to have a fixed width output; they are enabled during the time between a strobe and a clear in continuous mode.

Memory outputs feed also, in parallel, gates B10, B11 (C10, C11) for memory read-out through CAMAC.

OPERATION MODES

Each section features three different operation modes, selectable by a front panel three position switch. These are:

Overlap (OVP): The outputs will change of state during the time in which the configuration of pulses in input satisfies the programmed logic function. Following figure better explains the output behaviour. If a strobe pulse is sent in overlap operation mode, the input pattern will be stored and the output levels will be kept until the next clear.



Shaped (SHP): This operation mode requires necessarily a strobe pulse whose actions are multiple. The strobe is latched by IC A1 (A13) and a level is set to disable gates B4, B5 (B6, B7) and to latch the input configuration on gates C4, C5 (C6, C7). Also, the strobe is enabling the output gates A11, A10 (A9, A8) during a fixed time. In order to do that the strobe pulse is reshaped by a transistor stage and it is delayed in order to compensate for the memory transition time.

So a fixed output width will result, but the input stages will remain disabled to allow for pattern read-out.

Only a front panel clear or a CAMAC clearing action will defreeze the input stages. On the other hand, for each strobe pulse in input, a synchronization output (SYN) is provided on the front panel, which is timed with the outputs, and having also the same width as the outputs. If the input pattern is not needed, the SYN output can be sent to the clear (CLR) input to make the unit working in handshake mode. An even better frequency response can be obtained if a negative NIM DC level is applied to the CLR input. In that case however, the outputs will not have a fixed width, but they will depend on the overlap between the memory output and the strobe pulse as it is at the input.

It should be noted that the SYN pulse can also be used as a strobe for successive units.

Continuous (CNT): Also this operation mode requires necessarily a strobe pulse. Its action is as in the shaped mode for the input stages, while the output AND is enabled from the arrival of the strobe pulse and until the arrival of the next clear. The outputs are then made static in the meantime between a strobe and a consecutive clear.

This facility allows to build electronic chaines where timing problems are meaningless.

OUTPUT WIDTH ADJUSTMENT

In SHAPED operation mode, the output width can be adjusted through regulation of the front panel potentiometer.

In the following a possible procedure to regulate the potentiometer is indicated.

a) Make a CAMAC cycle with F(9)·A(2)(F(9)·A(3)). Word 0 will be then addressed in the memory.

b) Make a CAMAC cycle with F(16)·A(0)(F(16)·A(1) setting write lines W1 to W8 to the "1" state. A "1" is then written into the memories at the address zero.

c) Put the front panel switch on the position SHP.

d) Send a train of NIM pulses into the strobe input. Minimum width 5 ns. No other input is needed.

e) Looking at any one of the eight outputs at the scope, adjust the potentiometer until the needed width is reached.

PROGRAMMING THE MODEL 4508

INTRODUCTION

The loading of the circuit with the wanted logical functions, is made by computer program, via CAMAC. Due to the fact that any modern computer language contains already the AND, OR and NOT functions, the loading program becomes very short and easy. It consists essentially of 256 consecutive steps, each step corresponding to a different memory address. For each address the data has to be calculated, which then has to be fed into the memory. The data value should be zero if no output is needed for that combination, it should be one in the opposite case.

An example of loading program, written in FORTRAN for a micro NOVA computer is shown in the following figure.

```
C
C     ************************************************************
C     * THIS PROGRAM SHOWS HOW                                   *
C     * THE LECROY MODEL 4508 , FULLY PROGRAMMABLE LOGIC UNIT    *
C     * CAN BE LOADED WITH PARTICULAR LOGIC FUNCTIONS .          *
C     ************************************************************
C
      DIMENSION IA(0:255)
1     ACCEPT "SLOT OF 4508 (0=STOP) ? ",N      ;READ 4508 SLOT
      IF (N.EQ.0) STOP
      CALL ARRAY (IA)                          ;FUNCTION CONSTRUCTION
      CALL CAMO (N,9,2,0)                      ;RESET MEMORY ADDRESS
      DO 2 M= 0,255                            ;WRITE LOOP
      CALL CAMO (N,18,0,IA(M))                 ;WRITE 256 WORDS
2     CONTINUE
      CALL CAMO (N,9,2,0)                      ;RESET MEMORY
      DO 4 I= 0,255                            ;READ LOOP
      CALL CAMI (N,2,2,IX,IQ,IR)               ;READ 256 WORDS
      IADD = ISHFT (IR,-8)                     ;DECODE THE ADDRESS
      IF (I.EQ.IADD) GO TO 3                   ;VERIFY THE ADDRESS
      WRITE (10,5) I , IADD
      GO TO 4
3     IW= IR.AND.255                           ;DECODE THE WORD
      IF (IW.EQ.IA(I)) GO TO 4                 ;VERIFY THE WORD
      WRITE (10,6) I,IA(I),IW
4     CONTINUE
      GOTO 1
5     FORMAT (" ERROR : EXPECTED ADDRESS",I4," PRESENT ADDRESS =",I4)
6     FORMAT (" ERROR : ADDRESS :",I4,"  LOADED WITH",I4,"  CONTAINS :",I4
      END



      SUBROUTINE ARRAY (IA)                    ;CONSTRUCTION OF FUNCTIONS
C
C     ****************************************
C     * THIS SUBROUTINE BUILDS THE ARRAY IA(255) *
C     * WHICH WILL BE LOADED INTO THE MEMORY     *
C     * AS THE WORKING PROGRAM .                 *
C     ****************************************
C
      DIMENSION IA(0:255) , J(8) , I(8)
      DO 3 M= 0,255                            ;LOOP ON THE ADDRESS
      L= 1
      DO 1 K= 1,8                              ;LOOP TO DECODE ADDRESS IN BINARY
      J(K) = (M.AND.L)/L                       ;J(K) SIMULATE STATUS OF INPUTS
1     L= L*2
      CALL FUNCTIONS (I,J)                     ;USER FUNCTIONS
      L= 1
      IA(M) = 0
      DO 2 K= 1,8
      IA(M)= IA(M) + (I(K).AND.1)*L            ;IA(M) IS THE WORD TO BE LOADED
2     L= L*2                                   ;AT THE ADDRESS M
3     CONTINUE
      RETURN
      END
```

```
      SUBROUTINE FUNCTIONS (I,J)
C
C     ************************************************
C     * THIS SUBROUTINE BUILDS THE DATA I(8) WHICH HAVE *
C     * TO BE LOADED INTO THE MEMORY PER EACH ADDRESS   *
C     * ON THE BASIS OF THE WANTED LOGIC FUNCTIONS .    *
C     * USER HAS TO WRITE ESPLICITELY THE DESIRED       *
C     * LOGIC FUNCTIONS PER EACH OUTPUT .               *
C     * I(1-8) = 1 WHEN LOGIC FUNCTIONS SATISFIED       *
C     * I(1-8) = 0 IN ALL OTHER CASES .                 *
C     ************************************************
C
      DIMENSION I(8) , J(8)
C     J= INPUT BITS
C     I= OUTPUT BITS
      I(1) = J(1)
      I(2) = J(2)
      I(3) = J(3)
      I(4) = J(4)
      I(5) = J(5)
      I(6) = J(6)
      I(7) = J(7)
      I(8) = J(8)
      RETURN
      END
```

This program is composed of a main program and of two subroutines, ARRAY and FUNCTIONS.

The main program is essentially composed of two main loops each of them of 256 steps. The two loops are needed, the first one in order to load for each memory address the right content previously calculated and stored into an array IA (256); the second one is used in order to read back the memory content and compare it with the calculated one for checking purposes.

Subroutine ARRAY makes two essential things. First of all it decodes the memory address, going from 0 to 255 in a set of eight binary bits J(8). This set of eight bit simulates the status of the inputs for each of the 256 addresses. Secondly, for each address, the value to be loaded into the memory is calculated and stored in an array IA.
This value is calculated as the decimal translation of a set of eight bit I(8). Each of these I(8) represents the status of one of the eight outputs, for the given input configuration.

Subroutine FUNCTIONS is the real customer subroutine, that is where the bits I(8) are calculated for each memory address on the basis of the physical requirements. The example shown is the simplest case of a complete transparency of the module.

I(1)=J(1) means for instance that every time the input 1 is equal to 1 also the output 1 must be equal to 1. The same will be true for the other inputs/outputs.

This is the program which will be loaded into the circuit and, once this is done, every time the input 1 will receive a pulse, output 1, and only that, will provide a pulse.

EXAMPLES OF SIMPLE LOGIC

In order to show how simple logic functions can be implemented by the module, let us take only inputs 1 and 2 (J(1), J(2)) and output 1(I(1)), and let us consider the following examples.

COINCIDENCE BETWEEN J(1) and J(2)

The statement which has to be written if we want an output when there is coincidence between the two inputs is simply:

I(1) = J(1) AND J(2)
I(1) will be then equal to 1 when and only when both inputs J(1) and J(2) will be equal to 1. I(1) will be equal to zero in all other cases.

OR OF J(1) and J(2)

The needed statement is:

I(1) = J(1) OR J(2)

J(2) IN ANTICOINCIDENCE TO J(1)

I(1) = J(1). AND, (.NOT J(2))

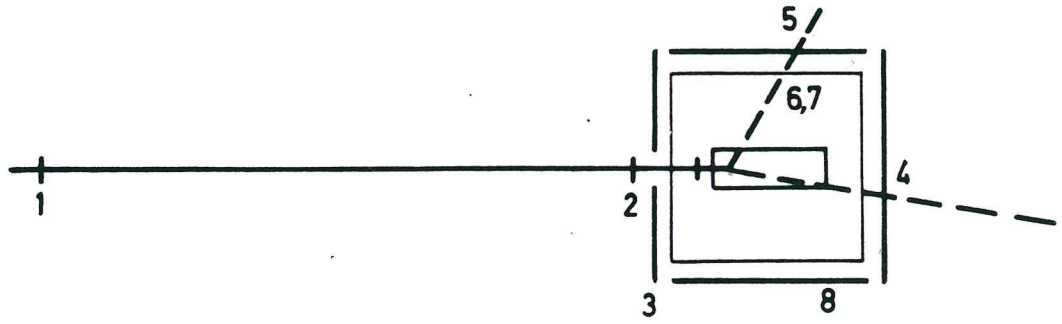
EXAMPLES OF MORE COMPLEX LOGIC

The three logic functions shown are the basic logic functions. Any more complex logic can be built on this three basic functions. This will be shown on the following examples implementing more complex logic.

It should be stressed again that the inputs/outputs can be interpreted as single lines as well as bits of a more complex binary word.

MIXED LOGIC

Let us suppose to have the physical problem depicted in figure below.



A charged beam strikes a target and interacts. We would like to isolate completely neutral final states and trigger on them. To do so, counters 1 and 2 individuate the beam, counter 3 should anticoincide the beam halo, counter 4 anticoincides forward charged particles, counters 5 to 8 anticoincides charges recoils. The physically interesting counting rates could be:

BEAM = $1*2$

BEAM-HALO = $1*2*\bar{3}$ = BEAM$*\bar{3}$

NEUTRAL FORWARD = $1*2*\bar{3}*\bar{4}$ = $\overline{\text{(BEAM-HALO)}}*\bar{4}$

NEUTRAL FINAL STATE = $1*2*\bar{3}*\bar{4}*\overline{(5+6+7+8)}$ =

= $\overline{\text{(NEUTRAL FORWARD)}*(5+6+7+8)}$

The 8 counters can be used then as inputs to one section of 4508. The first four outputs for instance can be programmed in order to give the desired rates. The statements which could be used then are:

```
I(1) = J(1)·AND·J(2)                                          (= BEAM)
I(2) = I(1)·AND·(·NOT·J(3))                                   (= BEAM-HALO)
I(3) = I(2)·AND·(·NOT·J(4))                                   (= NEUTRAL FORWARD)
I(4) = I(3)·AND·(·NOT·(J(5)·OR·J(6)·OR·J(7)·OR·J(8)))  (=NEUTRAL FINAL STATE)
```

If higher fan-out is needed for instance on the final trigger, another output can be defined as: I(5) = I(4)

MULTIPLICITY

A problem which is often encountered in physics experiment is, given a set of counters, the determination of the hit multiplicity. This information can be interesting in itself, that is, event per event, one want to know the exact number of hit counters, in coincidence with a strobe pulse.

Or one could need a trigger when the hit multiplicity is greater, or equal, a given value. Let us explore the different possibilities.

Let us suppose that we have eight counters connected at the inputs of the 4508, and possibly a strobe. The input hit multiplicity can range then from zero to eight, that is a number which expressed in binary, takes four bits. Let us reserve the first four outputs to give this number.

The statements to write into the subroutine FUNCTIONS and relative to the first four outputs, could be then:

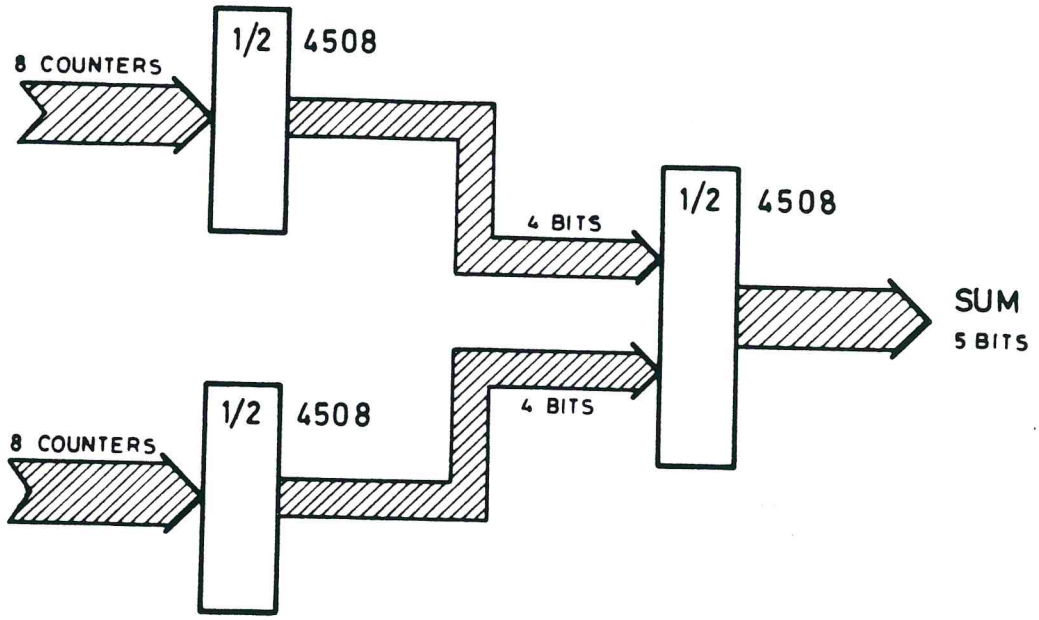
```
  N = J(1)+J(2)+J(3)+J(4)+J(5)+J(6)+J(7)+J(8);  INPUT MULTIPLICITY IN DECIMAL
  L = 1
  DO 1 k = 1,4
  I(k) = (N·AND·L)/L ;  INPUT MULTIPLICITY EXPRESSED IN
1 L = L*2            ;  BINARY AT THE OUTPUTS I(1)-I(4)
```

Let us now suppose that we want an output when the input multiplicity is equal to four. Let us reserve output 5 to this purpose. We should then add into the subroutine FUNCTIONS the following statements;

```
I(5) = 0
IF(N·EQ·4) I(5) = 1
```

SUM

We could have 16 counters and we could need the multiplicity over the all 16. We can then divide them in two groups of height counters and send the two groups to two different sections of 4508, as in figure:



Each of these sections will be programmed in order to give in output the input multiplicity expressed as a binary number of 4 bits, as before.

We have then to add the two four bit words and this can be done with a third section of 4508 programmed as follows:

```
  N1 = J(1)+2*J(2)+4*J(3)+8*J(4)  ; FIRST NUMBER IN DECIMAL
  N2 = J(5)+2*J(6)+4*J(7)+8*J(8)  ; SECOND NUMBER IN DECIMAL
  N  = N1+N2                      ; SUM IN DECIMAL
  L  = 1
  DO 1 k = 1,5
  I(k) + (N·AND·L)/L              ; SUM EXPRESSED IN BINARY AT THE OUTPUTS
1 L = L*2                         ; I(1)-I(5)
```

The sum will occupy five outputs, since it will be a number ranging from 0 to 16.

Three outputs are still left free. They can be used for instance to give triggers on fixed multiplicity as in the example before.

CONCLUSION

We hope to have demonstrated, with the above examples, the flexibility of the 4508 and the extreme facility in programming. Many more applications could be envisaged. Generally speaking most of the problems of logic encountered in experimental physics can be faced with this module.

It could be helpful to think that each 4508 sections accepts up to eight bits in input and provides up to eight bits in output. In the middle there is a box which can be programmed in order to apply any kind of algorithm on the inputs and give the result at the outputs.

TIMING CONSIDERATIONS

When running in overlap operation mode, the outputs may have a maximum time spread of ± 3 ns (see technical specifications). This is due to the RAM properties. The RAM access time is indeed dependent from the address chosen, within the quoted time spread.

The figures below show examples of how the transit time depends on the address.

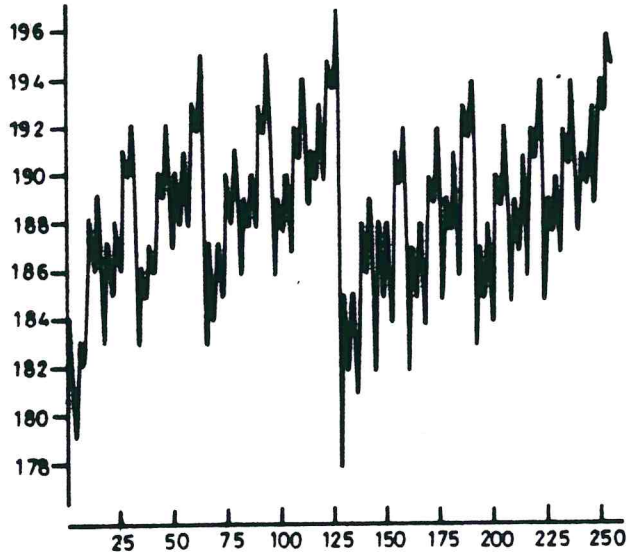
It can be seen that most of the addresses have a quite contained time spread. But, periodically, time spikes come out which have a direct influence on the minimum input width, as well as on the maximum frequency.

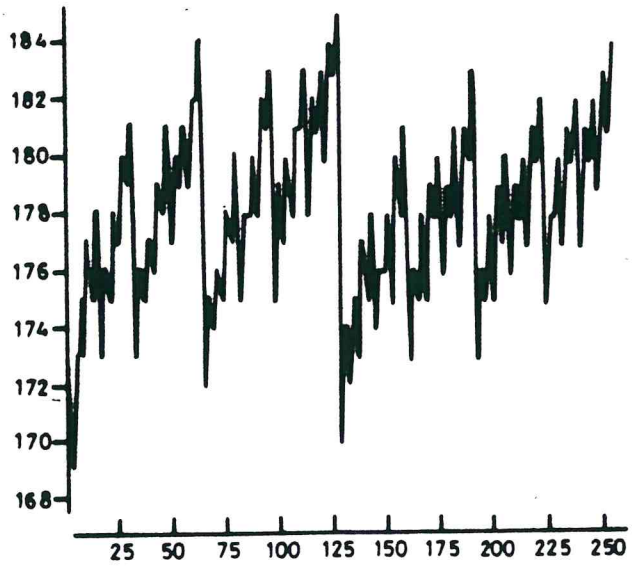
The strobed delay is fixed in order to recover all possible addresses.

The maximum frequency is quite strongly influenced by the address chosen. So that, while most of the addresses allow a maximum working frequency as high as 100 MHz and higher, few addresses, mainly the ones characterized by many inputs present in coincidence, are much slower.

The given figure of 65 MHz as maximum frequency, is the absolute measured minimum, measured over several series of memories.

PROPAGATION DELAY - OVERLAP MODE





POSSIBILITY OF CASCADING MODULES

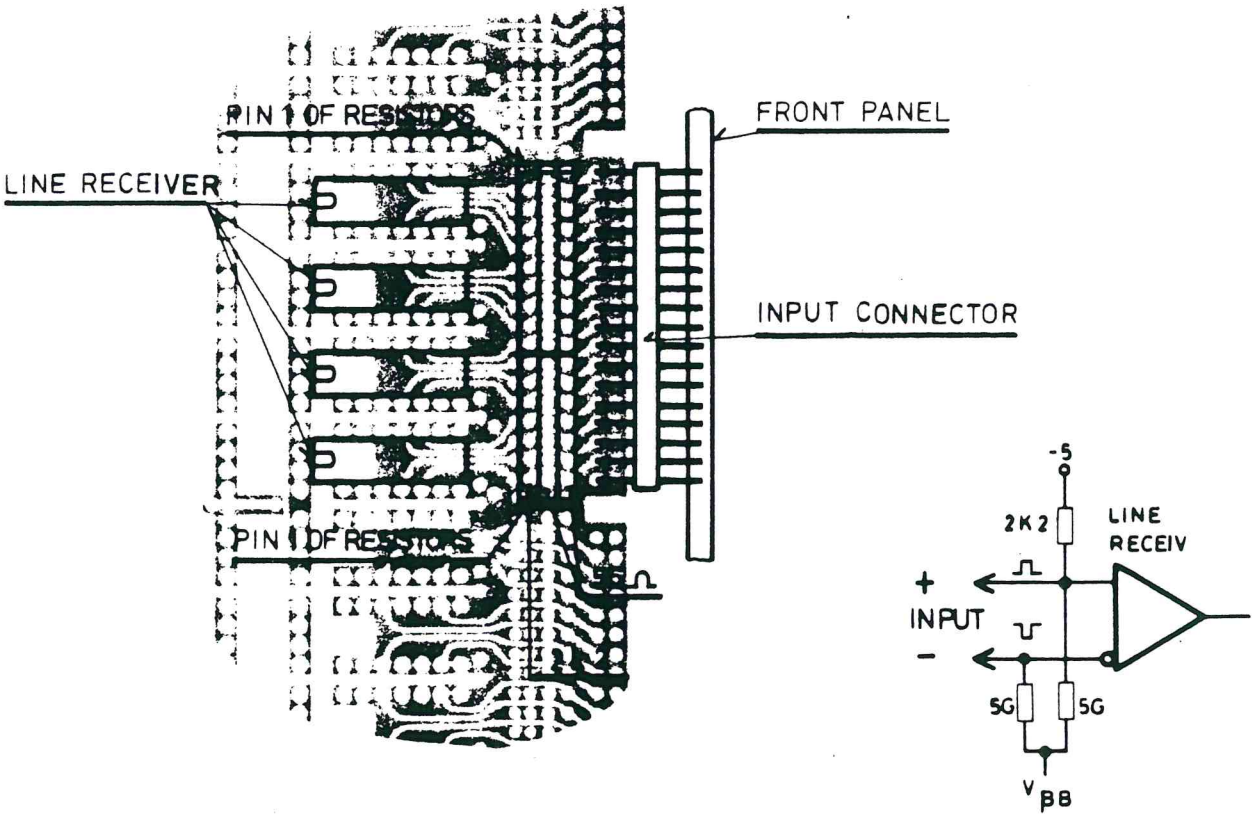
All differential ECL inputs, in ECLine modules, are terminated inside the module by two 56 ohms resistors to VBB, realizing a differential matching impedance of 112 ohms.

The input terminations are included in socket mounted, single in line resistor arrays, which can be removed if more than one unit have to be cascaded on the same driving cable. In this case, only the last unit in the daisy chain must be terminated for proper operation. (For more details see also the ECLine Application Note).

Figures below show the standard input stage of an ECLine module and the lay-out on the board.

WARNING : The resistor arrays are not symmetrical and they must be mounted in the proper way.

LOCATION OF INPUT TERMINATOR



ECL CABLES

Interconnections between different ECLine modules, for transmission of different ECL pulse pairs, can be made either by multiwire cables or by single twisted pair cables for one to one connections.

Such interconnecting cables can be purchased by LeCROY and in particular, as multiwire cables, two types are available, one for short connections using just flat cable, the second one for long interconnections using twisted and flat ribbon cable.

The denomination of such cables is as follows :

- STC-DC/34-LL Multiwire cable for short interconnections
- LTC-DC/34-LL Multiwire cable for long interconnections
- STP-DC/02-LL Single twisted pair cable.

Where LL is the cable length in feet which should be specified by the customer.