CAMAC ECLine
MODEL 4532
32 INPUT MAJORITY
LOGIC UNIT
USER'S MANUAL

October 1982

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration,

and use of LeCroy equipment are available from the Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499 (914) 578-6059, or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support service. For example, Blue Ribbon service provides guaranteed three-day turn around on repairs, a direct access number for product application assistance, yearly calibration and the addition of engineering improvements. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.

- Modify the software and/or merge it into another program for your use on a single machine.

- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LIST ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

GENERAL DESCRIPTION

The LeCroy Model 4532, Majority Logic Unit, has two basic modes of operation depending on the position of the MEMORY ENABLE switch.

If the MEMORY ENABLE switch is OFF, the 4532 is completely transparent with respect to inputs and outputs.The information present at all outputs will be a function of the instantaneous signals at the inputs during the gate time. The CAMAC functions become clearely meaningless, and will not be executed. No Q response will be generated.

If the MEMORY ENABLE switch is ON, pulses arriving at the input having their leading edges falling during the GATE pulse widths, will be stored.

Consequently, at the end of the GATE pulse, all the outputs will be stable and a LAM signal can eventually be generated. The information at the outputs will remain stable until a reset is applied either by CAMAC or by the input RTI (Reset Input).

It should be noted that the RTI input does not clear the LAM. This avoids problems during the CAMAC search for LAM sources.

On the other hand, the RTI input cleares the data memory. Therefore care should be taken to synchronisation the CAMAC activity with with the RTI signals.

FUNCTIONAL DESCRIPTION

The following description refers to the bloc diagram and schematics included with this manual. Depending on the operation mode, the input pulses can either set bits in a memory or go through an AND gate enabled by the GATE input.

After this initial stage, the signals coming either from the memory or from the AND gate, follow same path. These signals are termed "internal data", and pass through the following consecutive logic stages.

1. OR outputs

   The module provides a general logical OR of the 32 internal data on the output connector ORO (OR Output). In addition, the logical OR of the internal data taken 2 by 2 (IN1.OR.IN2 on OUT1, IN3.OR.IN4 on OUT2, and so on) is generated on the OUTs 1 to 16.

2. Cluster logic

   If the CLUSTER ENABLE switch is OFF, the 32 channels of internal data go directly to the Digital to Analog Converter (DAC) which sets the multiplicity analog level at the output. If the CLUSTER ENABLE switch is ON, each internal data vetoes the adjacent higher one. Consequently only the first bit in a set of consecutive bits (cluster) will be active into the DAC.

   In order to cascade several 4532's, channel 1 can be vetoed by the Cluster Carry Input (CCI). The internal data present on channel 32 is provided for the next 4532 module on the Cluster Carry Output (CCO).

3. Analog Majority Input-Output (AMIO)

   After the cluster logic the data is converted to a current by the DAC.

   The presence of a bit in the data coming into the DAC generates a 1.6 mA current source (adjustable by changing the Voltage-VD) in circuitry which at the same time adds these currents.

   The sum of the currents is performed by the common base mounted transistors T1 and T2.

The collectors of T1 and T2 are connected together to finally give the total sum of the currents. This total current is carried to the base of transistor T12 and the collector of transistor T3.

The current flowing through T4 and T12 will be the image of the one flowing through T3. This fact permits the transfer of the current to T5, T13 and T6, mounted in the same configuration as T3, T4, T12.

The resistance on the T6 emitter is one half of the one on the T5 emitter. This means that the current finally procided by T3 at the output, will be of 3.2 mA/hit. In order to compensate the different offset currents that can be present, the transistor T7 produces a constant current, adjustable by the internal potentiometer OADJ (offset adjustement), permitting a zero quiescient current on AMIO.

The circuitry is protected against missing 50 Ω terminations at the AMIO outputs, by the 39 Ω resistor between T12 and T5.

4. Majority Discriminated Output (MDO)

The AMIO signal is directly connected to a comparator input. The comparator threshold can be adjusted between O V and -1.5 V by the front panel potentiometer MATHR (Majority Threshold). It should be noted that the status of MDO output will be conditioned not only by the DAC output, but also by signals connected to the AMIO from other units.

5. Delayed Majority Output (DMO)

The output DMO is internally connected to a delay circuit based on the principle of a comparator connected to a capacitor being charged by a constant current. The comparator threshold, and resulting delay, can be adjusted by the front panel potentiometer DM DEL. The digital output of comparator MDO regulates the charge and discharge of this capacitor. When the MDO is off the transistor T8 discharges and holds the capacitor at a high reference voltage. When the MDO comparator provides a signal, T8 goes off and the capacitor charges with constant current and the amplitude of this charge is limited by T9.

The DM DEL switch selects two capacitor values to permit two different delay ranges.

6. Strobe Output (STO)

The width of the strobe output is determined by the charge at constant current of the variable capacitor ST WIDTH. When a gate signal GAI is applied, it closes the gate B1 and charges the variable capacitor. The amount of the charge is limited by T10 and T11. At the end of the gate pulse, B1 opens again and the variable capacitor discharges. The strobe output STD will be present as long as the voltage on the variable capacitor is greater than the threshold of B1.

It should be noted that STO is cleared by GAI and starts again from the end of GAI.

7. LAM circuit

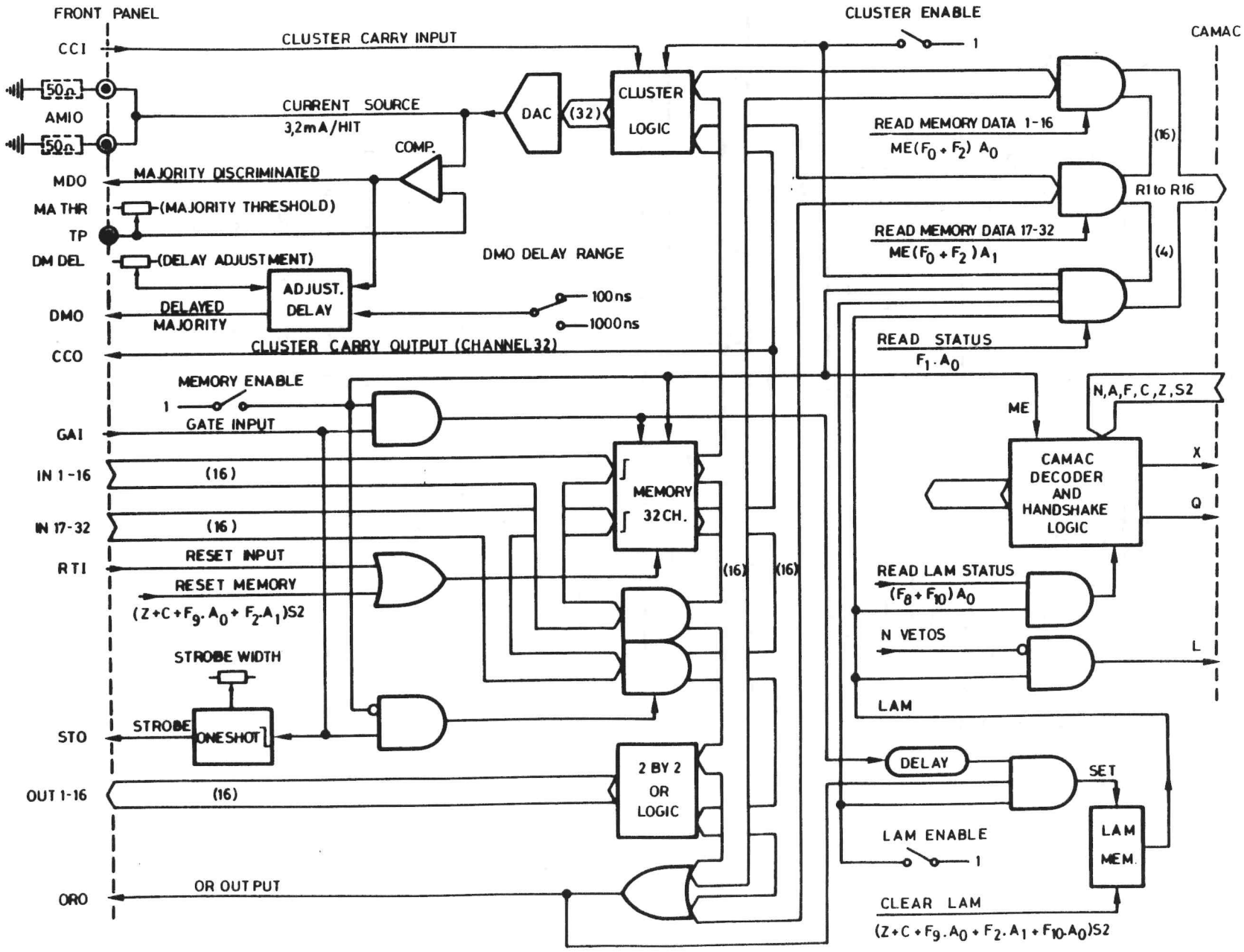
LAM circuit is composed of the two flip-flops I1. The first one memorizes a LAM request and acts on the L line. Its setting is dependent on switches LAM ENABLE and MEMORY ENABLE being ON. The first flip-flop is set by the leading edge of the signal provided by gate B1, pin 14, and translated by transistor T12.

Gate B1 has the function of halting the OR signal during GAI which would have generated a LAM.

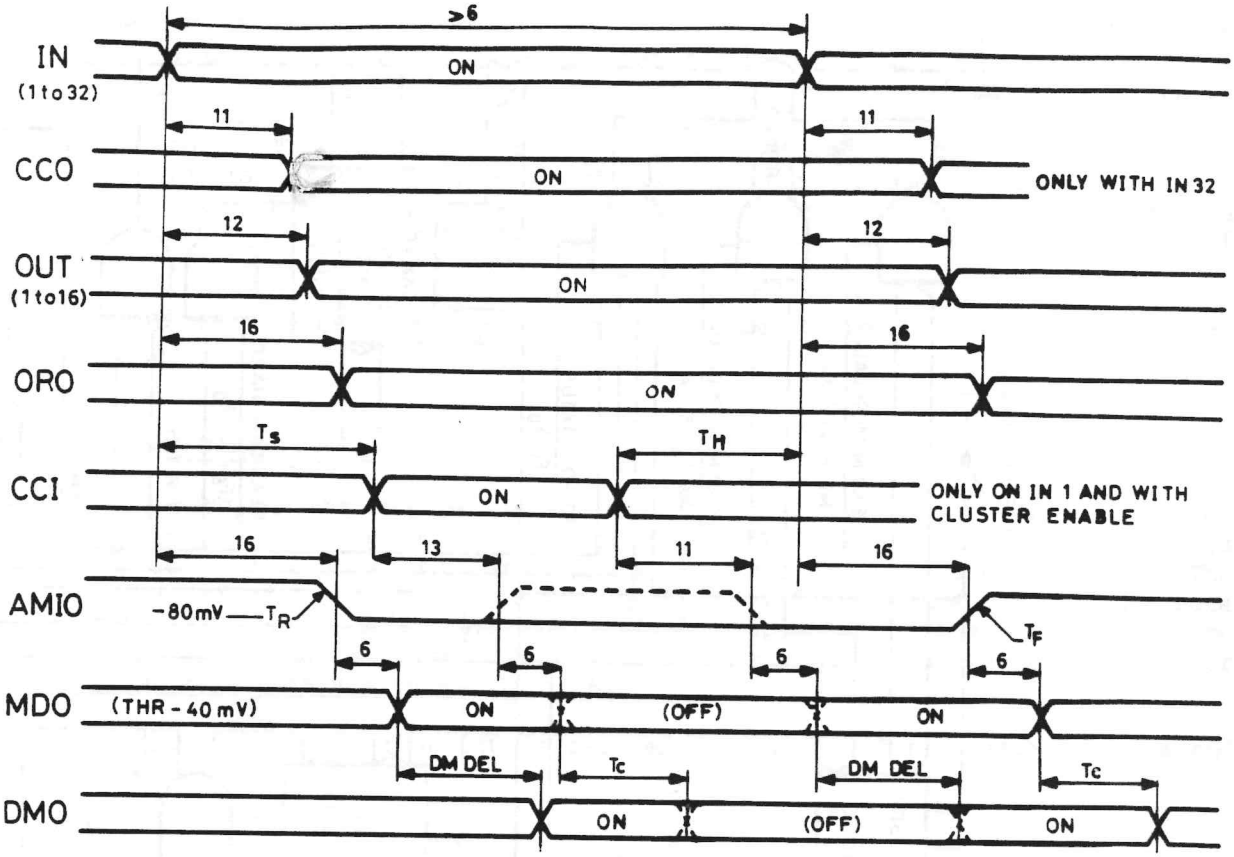
The second flip-flop, which is coupled to the first one, is set at the beginning of a CAMAC cycle if the L line is ON. It generates the Q response in recognition of F(8) and F(10).

In order to avoid loss of a LAM request coming during F(10), the reset by F(10) is halted if a Q response has not been delivered.

MODEL 4532 BLOCK DIAGRAM



MEMORY DISABLE TIMING (with GAI open)



All times in ns

T_s : Cluster disable set-up time, min. -2 nsec

T_h : Cluster disable hold time, min. 6 nsec

T_r : AMIO rise time < 6 nsec with amplitude of 1280 mV

T_f : AMIO fall time < 7 nsec with amplitude of 1280 mV

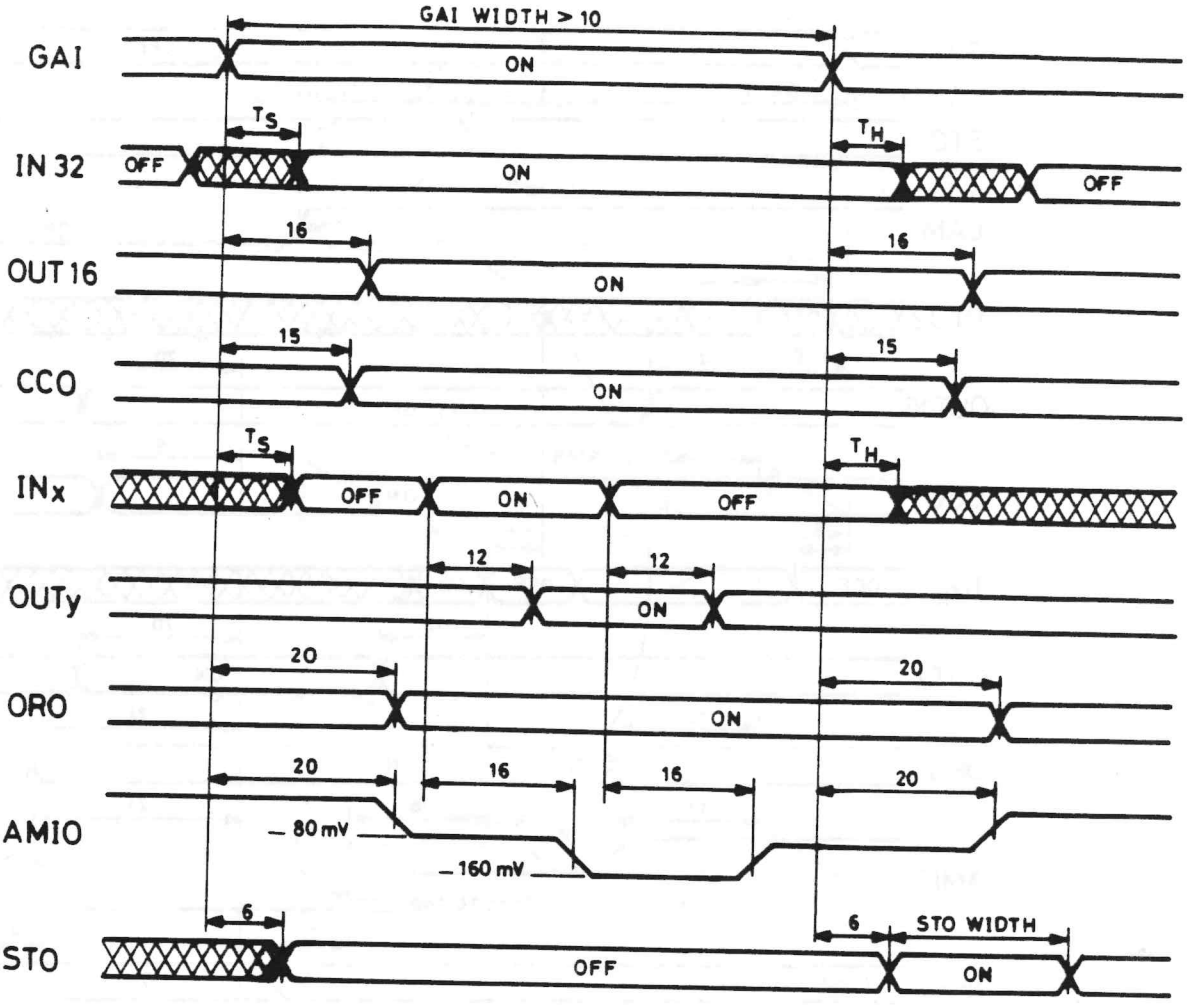
DMDEL : Adjustable from < 10 nsec to > 100 nsec

or from < 50 nsec to > 1 µ sec

T_c : DMO clear time: on range 100 nsec < 8 nsec

on range 1 µ sec < 16 nsec

MEMORY DISABLE TIMING



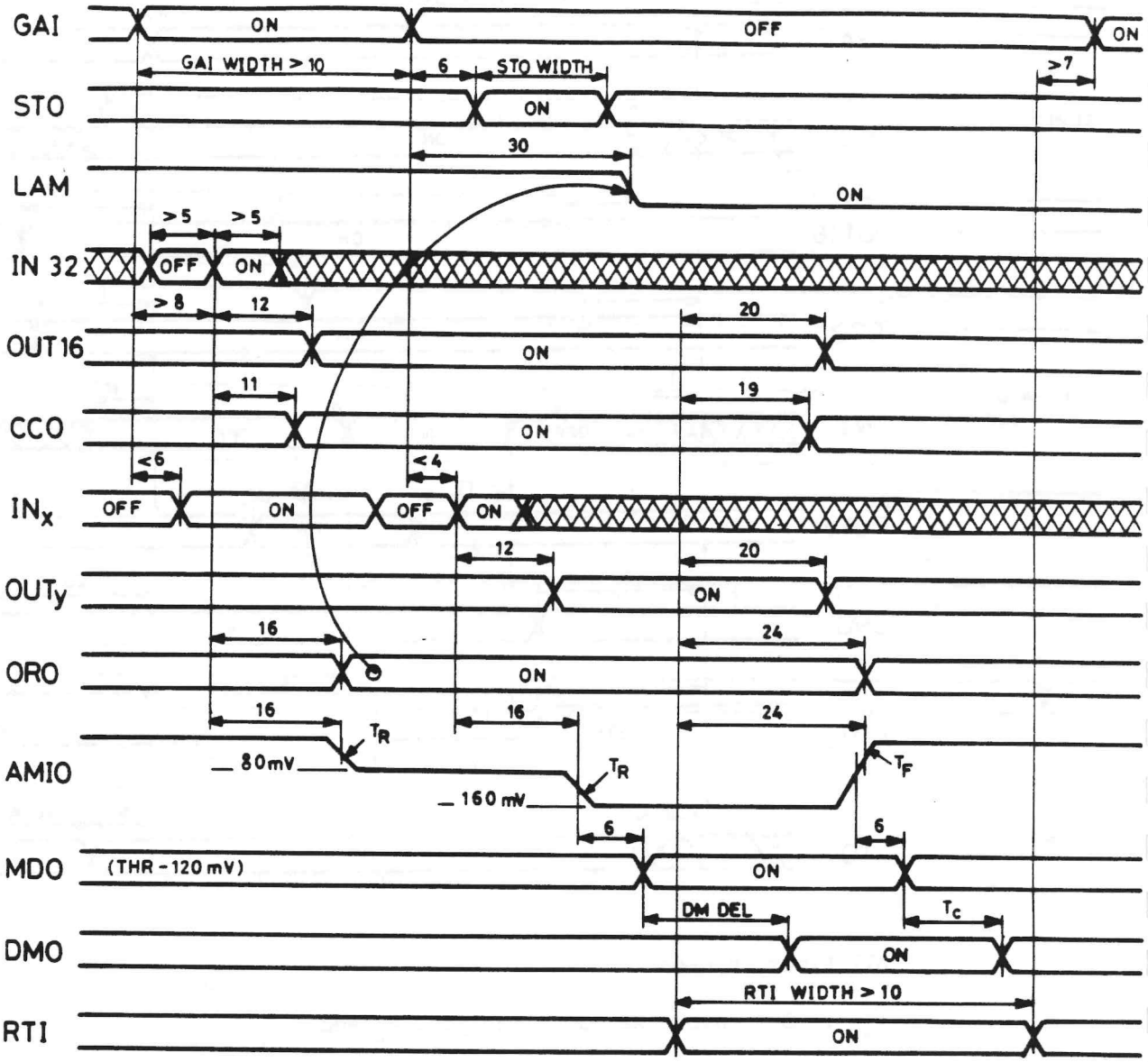
All times in nsec

T_s : GAI enable set-up time, min. 4 nsec

T_h : GAI disable hold time, min. 4 nsec

STO WIDTH : ADJUSTABLE FROM < 10 nsec to > 25 nsec

MEMORY ENABLE TIMING



All times in nsec

STO WIDTH : Adjustable from < 10 nsec to > 25 nsec

DM DEL : Adjustable from < 10 nsec to > 1 µsec

T_r : AMIO rise time < 6 nsec

T_f : AMIO fall time < 7 nsec with amplitude of 1280 mV

T_c : DMO clear time : on range 100 nsec < 8 nsec
on range 1 µsec < 16 nsec

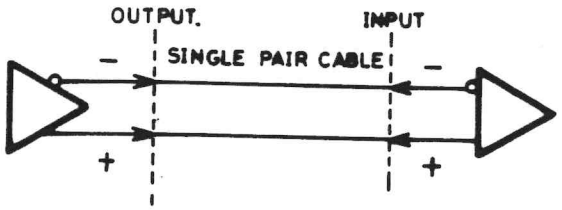
APPLICATION NOTE

In MEMORY ENABLE mode, several self triggering operations are possible by connecting the outputs ORO, STO, MDO, DMO with the inputs GAI and RTI.

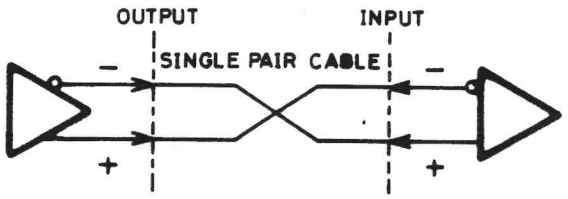
It should be noted that the RTI input can also be used as a gate. However the output signals are reset during the width of the signal applied on RTI.

Self Triggering can be done in two ways:

- Direct (example: RTI = MDO)

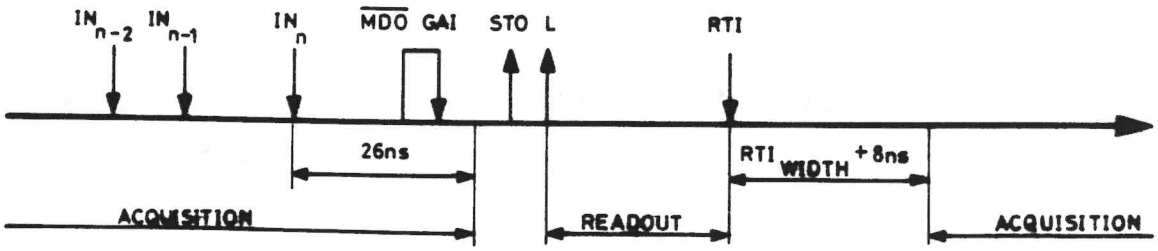


- Inverted (example: GAI = MDO)



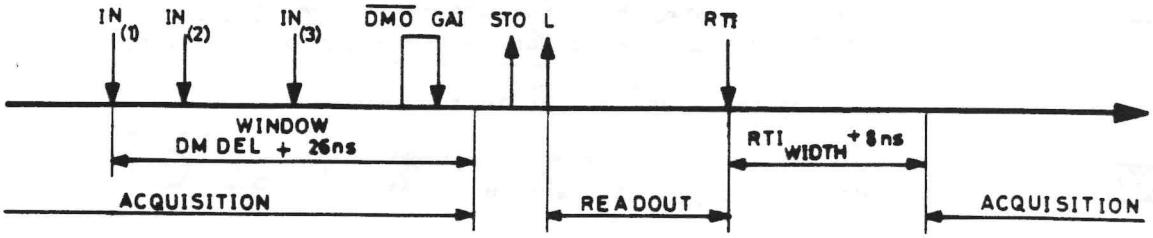
Application examples:

a) Start a CAMAC readout after reception of a given number n of inputs.
The number n can be set from 1 to 16 adjusting the MATHR potentiometer. The GAI = MDO self triggering technique should be used, while RTI can be used as gate.

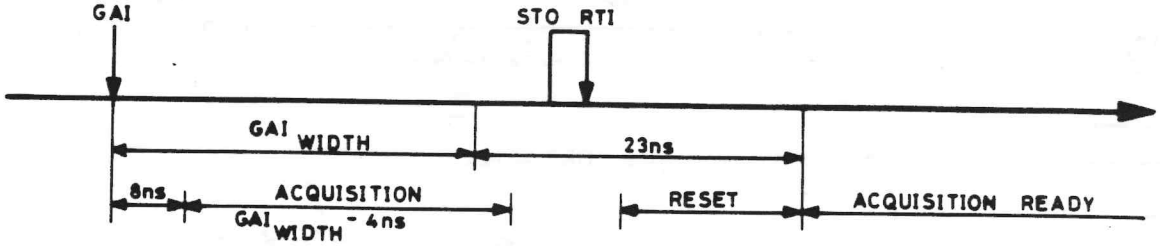


b) Start a CAMAC readout after a given time window of acceptance, where the time window is started by the first arriving input.

GAI = DMO should be used and the majority threshold (MA THR) set for n = 1. The first IN arriving will start the time window, while the width is established by DM DEL. RTI can again be used as gate.

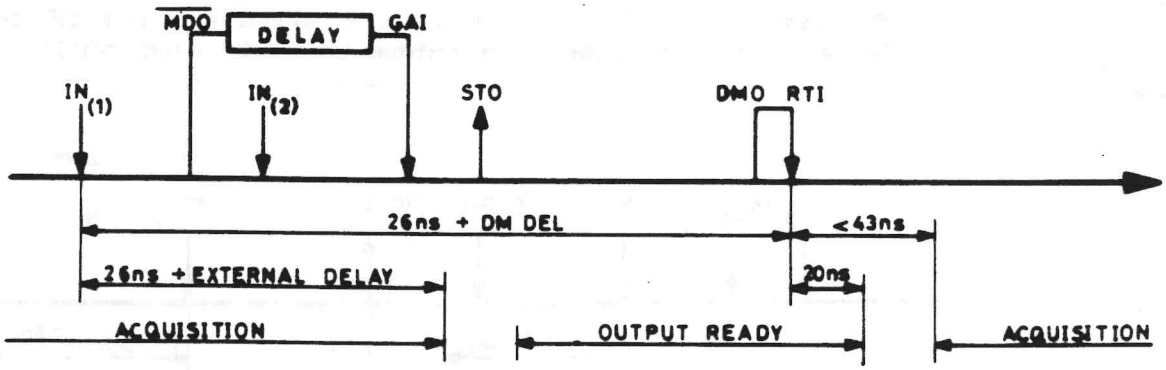


c) Automatic reset after a gate.
Let RTI = STO and adjust the STO width to 10 nsec.



d) Start a time window of acceptance by the first input signal; automatic reset after the time window.

MA THR should be set for n = 1 and GAI = MDO (or GAI = ORO) through a delay line. The reset will be executed by RTI = DMO with a delay adjustable by DM DEL.



OPTIONAL ACCESSORIES

ECL CABLES

Interconnections between different ECLine modules, for transmission of different ECL pulse pairs, can be made either by multiwire cables or by single twisted pair cables for one to one connections.

Such interconnecting cables may be purchased from LeCROY and in particular, as multiwire cables, two types are available; one for short connections using just flat cable, the second one for long interconnections using twisted and flat ribbon cable.

The notation for ordering these cables is as follows:

- STC-DC/34-LL Multiwire cable for short interconnections
- LTC-DC/34-LL Multiwire cable for long interconnections
- STP-DC/02-LL Single twisted pair cable

where LL is the cable length in feet which should be specified by the customer.