OPERATOR'S MANUAL

NIM MODEL 465

TRIPLE 4 - FOLD
COINCIDENCE UNIT

Revised
May , 1989

(ECO 1015)

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instructions regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other material that apply to the specific version of the instrument as identified by its ECO number.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental or consequential damages, whether in contract or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration and use of LeCroy equipment are available from the Research Systems Division Customer Services Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499 (914) 578-6030 or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support service. For example, Blue Ribbon service provides guaranteed three-day turn around on repairs, a direct access number for product application assistance, yearly calibration and the addition of engineering improvements. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purpose of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates in the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

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- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

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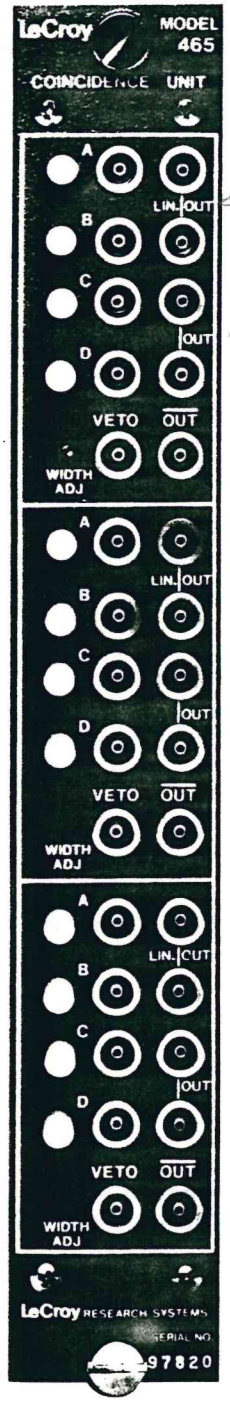
NIM STANDARD LOGIC MODULE
THREE SECTION, 4 INPUTS

LeCroy



Model 465

3-Channel, 4-Fold Logic Unit With Veto

The Model 465 contains three independent high-speed general purpose coincidence units in a single-width NIM module. Each channel has four coincidence inputs and a separate veto which accept standard negative NIM logic levels. The logic inputs may be individually enabled or disabled without altering input cabling or termination by means of front-panel pushbutton switches. With all inputs enabled, four inputs are required. Disabling the logic inputs is equivalent to reducing the number of simultaneous negative inputs required for an output. Thus, each channel may be programmed for 4-fold, 3-fold, or 2-fold logic decisions. With only one input enabled, each channel of the Model 465 operates as a logic fan-out.

Once triggered by signals satisfying the input coincidence requirements, the Model 465 generates five NIM fast logic outputs: one pair of – 32 mA negative preset outputs, one – 16 mA preset complementary output, and one pair of – 32 mA overlap outputs. The preset outputs are continuously adjustable from less than 5 nsec to greater than 500 nsec by means of a front-panel multiturn potentiometer and are independent of input overlap time, amplitude, and rate. Because it is updating, it may be retriggered even before the end of an output pulse that is already present. The overlap outputs are equal in duration to the coincidence overlap and produce outputs up to the maximum input rate capability.

The front-panel fast veto input accepts standard negative NIM-level pulses. To veto the linear outputs, the veto signal must completely overlap any input coincidence; to veto the preset outputs, a prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition is required. A rear-panel bin-gate switch permits a slower (50 nsec response time) inhibiting of the Model 465 by a clamp to ground from + 4 V through the bin gate pin of the rear power connector.

The Model 465 is packaged in a standard AEC/NIM #1 module (AEC Report TID-20893) and uses exclusively Lemo front-panel connectors.

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Innovators in Instrumentation

SPECIFICATIONS
NIM Model 465
TRIPLE 4-FOLD LOGIC UNIT

INPUT CHARACTERISTICS

Logic Inputs:	4; Lemo connectors; 50 Ω impedance; negative NIM-level input requirements; each input can be separately enabled or disabled by front-panel pushbuttons.
Veto Input:	Standard negative NIM-level signal, 3.5 nsec minimum width. Requires complete overlap of input coincidence for linear outputs and prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition for the preset outputs. (Veto should precede this leading edge by approximately 5 nsec in this case.)
Bin Gate:	Via rear connector; clamp to ground from +4 V inhibits; risetimes and falltimes <50 nsec.

OUTPUT CHARACTERISTICS

Preset Outputs:	3; one dual negative; quiescently 0 mA, −32 mA during output; one positive; quiescently −16 mA, 0 mA during output. Updating.
Overlap Outputs:	One dual negative; quiescently 0 V, −32 mA during output; duration equal to coincidence overlap. Non-updating.
Fan-Out:	5-fold, if each output drives a 50 Ω load.
Duration:	Continuously adjustable from less than 5 nsec to greater than 500 nsec by means of front-panel, screwdriver-adjustable potentiometer. Width stability: better than ±0.2%/°C.
Output Risetimes:*	$\overline{\text{OUT}}$: 2.0 nsec typical (max. 2.5 nsec). OUT: 2.2 nsec typical (max. 2.5 nsec; 3.0 nsec with negative output unterminated).
Output Falltimes:*	$\overline{\text{OUT}}$: 2.0 nsec typical (max. 2.5 nsec). Slightly longer on wide output durations. OUT: 2.2 nsec typical (max. 2.5 nsec). Slightly longer on wide output durations.

GENERAL

Logic:	2-fold, 3-fold, or 4-fold coincidences plus fan-out determined by selectively disabling logic input.
Coincidence Width:	⩾1 nsec, determined by input pulse durations.
Rate:	0 to >120 MHz.
Input-Output Delay:	13 nsec for preset outputs; 8.5 nsec for overlap outputs.
Multiple-Pulsing:	None; one and only one output pulse of preset duration is produced each time the input conditions are satisfied regardless of the duration of the input pulses or their overlap.
Double-Pulse Resolution:	8 nsec.
Packaging:	Single-width AEC/NIM module; in conformance with AEC standard; Lemo connectors used for all inputs and outputs.
Power Requirements:	65 mA at +12 V; 125 mA at +6 V; 5 mA at −24 V 135 mA at −12 V; 640 mA at −6 V

* −10 to 90%

SPECIFICATIONS SUBJECT TO CHANGE

SECTION 2

OPERATION

2.1 Logic Inputs

The Model 465 has direct-coupled, 50 ohm impedance, inputs which accept NIM logic signals. These inputs, typically driven from a discriminator or other logic unit, are protected both for transient and DC signals up to ±5 V. Since the input reflections are less than 7% for signals of as little as 2 nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e. -1.8 V) will reflect only approximately 125 mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

2.2 Veto Input (for preset outputs only)

The veto inputs of the Model 465 require NIM logical one input signals (i.e. <-600 mV into 50 Ω). In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the leading edge of the input signal that would otherwise cause the coincidence condition. See Figure 2.1.

2.3 Veto Input (for linear outputs only)

The veto inputs of the Model 465 require NIM logical one input signals as described above. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the entire coincidence condition as shown in the diagram below. This requirement is necessary since this linear output is determined only by the output of the front end of the logic unit, as opposed to the preset outputs where the leading edge of the front end output triggers a preset width stage. In the latter case, if the leading edge is vetoed, the entire preset width output stage never sees it, thereby preventing any preset output. In the case of the linear outputs, any portion of the front end output that is not specifically overlapped by the veto pulse will appear at the linear output connectors. See Figure 2.2.

2.4 Input Select Switches

Any input will be removed from the coincidence requirement without removing its cable if the adjacent "Input Select Button" is in the OUT position.

2.5 Usage of 465 as a Triple 5-Fold Coincidence

In order to use the 465 as a 5-fold coincidence unit, a complimentary fast NIM signal may be applied to the veto input. This signal will quiescently, then, hold the 465 in an off condition. When a pulse is applied to this input, it permits the 465 to give an output if the other selected inputs are in coincidence. Such application of the 465 is possible only by sacrificing usage of the veto input as a true inhibiting function.

2.6 Output Characteristics

Bridged Negative Outputs

The Model 465 has two pairs of current source 50 ohm outputs, delivering -32 mA of current during the output and 0 mA quiescently. These outputs are fully differential type current source outputs. They maintain a risetime of approximately 2.0 nsec and a reasonably clean shape, as long as care is taken to terminate at least one half of the other bridged output in that channel.

The actual shape of typical outputs from a 465 is shown in Figure 2.3

Using the typical output pulse shape as a visual reference, outputs on the 465 are set up to adhere to the restrictions in Figure 2.4, with the adjacent output pair terminated into 50 ohm:

Complementary Output:

The single complementary output is actually the output from the collector on the other half of the differential pair supplying current to one pair of preset outputs. Although it is internally a double amplitude signal, it is subsequently internally back-terminated into 50 ohm, thereby maintaining a quiescent level of -16 mA, and logical 1 of 0 mA. Risetime and other characteristics are similar to that of the normal outputs.

Usage of Bridged Negative Outputs Driving a Single Cable:

In applications where it is necessary to drive very long cable lengths from a logic unit output, it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively sends all 32 mA into one cable, giving nearly a double amplitude output. It is important to know that the 465 has clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 V. It cannot be assumed, therefore, that the -32 mA into one 50 ohm cable will give a -1.6 V output signal.

2.7 Coincidence Characteristics

Minimum Coincidence Overlap (Coincidence Resolving Time):

The required coincidence overlap time of two input signals on the 465 is approximately 3.5 nsec. This measurement could be made using two pulses of zero risetime. In practice, no discriminator or other logic unit exists which can perform this function. Therefore LeCroy uses the two methods discussed below where inputs have rise and fall times of approximately 1.5 nsec.

One method used at LRS is to measure the overlap time as follows. Two 10 nsec FWHM pulses from a single source all initially separated in time and fed into two of the inputs of the Model 465. The output of the 465 is displayed on an oscilloscope which is being externally triggered by the source (see Figure 2.5). Initially, no output will appear from the 465 (see waveforms in Figure 2.6). At some duration of overlap, output pulses will always appear. The minimum coincidence overlap is defined in LRS terminology as that amount of overlap which produces one output on the average for every two sets of inputs (i.e., 50% point). The 50% point can be quite accurately estimated on the oscilloscope (externally triggered) by adjusting the second pulse delay for equal intensity of trace (of the output states) for the duration of the output pulse.

Coincidence Curve Method of Measuring Resolving Time:

An alternative method used at LRS to measure the resolving time and time jitter involves making a coincidence curve and the measuring its "risetime" and "falltime". Two pulses from a single source are initially separated in time and fed into the inputs of the 465, at the same time being collectively counted in a scaler (see Figure 2.7). The 465 output is also counted into another scaler channel.

As one pulse is delayed more and more, the two pulses become more and more coincident; by comparing the counts in the two scaler channels at different delay amounts, a curve can be made representing Rate Out/Rate In vs. Time Delay where the time delay is measured from the trailing edge of Pulse A to the leading edge of Pulse B. (The previous waveform diagram is valid for this measurement also, except Pulse A delay should be continued until its leading edge is past the trailing edge of Pulse B.)

The resultant coincidence curve for this measurement would appear as shown in Figure 2.8.

The minimum coincidence overlap or minimum resolving time of the logic unit is defined as one-half the difference between the sum of the input pulse widths and the coincidence width measured above. Alternatively (but with more difficulty), if t_0 represents the time at which pulse A trailing edge and Pulse B leading edge are exactly coincident in time, then the minimum resolving time is equal to t_2-t_0.

If both input pulses A and B are identical in shape, and if the

inputs to the coincidence unit are identical, the trailing edge side of the coincidence curve should be symmetrical to the leading edge side. If they differ, the larger one (either 0% to 100% or 100% to 0%) is specified as the resolving time jitter.

It is important to note that the major contribution toward resolving time jitter in typical logic units is the instability of the "threshold" level of the differential amplifier following the input "AND" stage, particularly for inputs with slow inherent risetimes (i.e., <2 nsec). In the 465, a true high sensitivity discriminator is used which has a very stable and jitter-free threshold (the LD601C hybrid used in all LRS multichannel NIM discriminators). For this reason, the resolving time jitter of the 465 is quite small.

2.8 Maximum Rate

Maximum CW rate capability of the 465 is guaranteed at 110 MHz. Typically, the maximum rate is 120 MHz, with some units being capable of operation beyond 130 MHz for small bursts of input pulses. The measurement for maximum rate is made by applying pulses to one of the inputs, with the other three inputs either disconnected or set in the OFF position (i.e., internally always enabled at a DC logical 1).

The double pulse resolution (DPR), as opposed to CW rate capability actually defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur whereas a CW input pulse train would be unlikely. For a coincidence unit like the 465, the coincidence width of the input pulses would limit the double pulse resolution of the unit. Each input itself is capable of responding to input pulses spaced 8 nsec apart, measured at the FWHM points of the leading edge (i.e., -375 mV point for -750 mV input pulses). Since the minimum coincidence width of the 465 is approximately 3.5 nsec the 465 can actually function, resolving coincidences spaced as norrow as 8 nsec apart.

Packaging:

The 465 Triple Coincidence Unit is packaged in a #1 NIM module with Lemo-type connectors. Due to front panel space limitation, the 465 is not offered with BNC's.

Current Requirements:

The current usage of the 465 will permit the use of seven modules per standard NIM bin offering 5 A of ±6 V, 2 A of ±12 V, and 1 A of ±24 V. Power calculation works out to 7.1 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot. It is recommended that additional -6 V current be supplied to permit maximum usage of NIM Bin space or that the 465's are powered in the same NIM bin with other modules not requiring -6 V. Higher power NIM supplies (Model 1002A provides 10 amps of ±6 V) are available from LeCroy. This power supply is also incorporated as part of the Model 1403 heavy duty NIM bin.

Recommended Use of the NIM Power Bins:

It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.

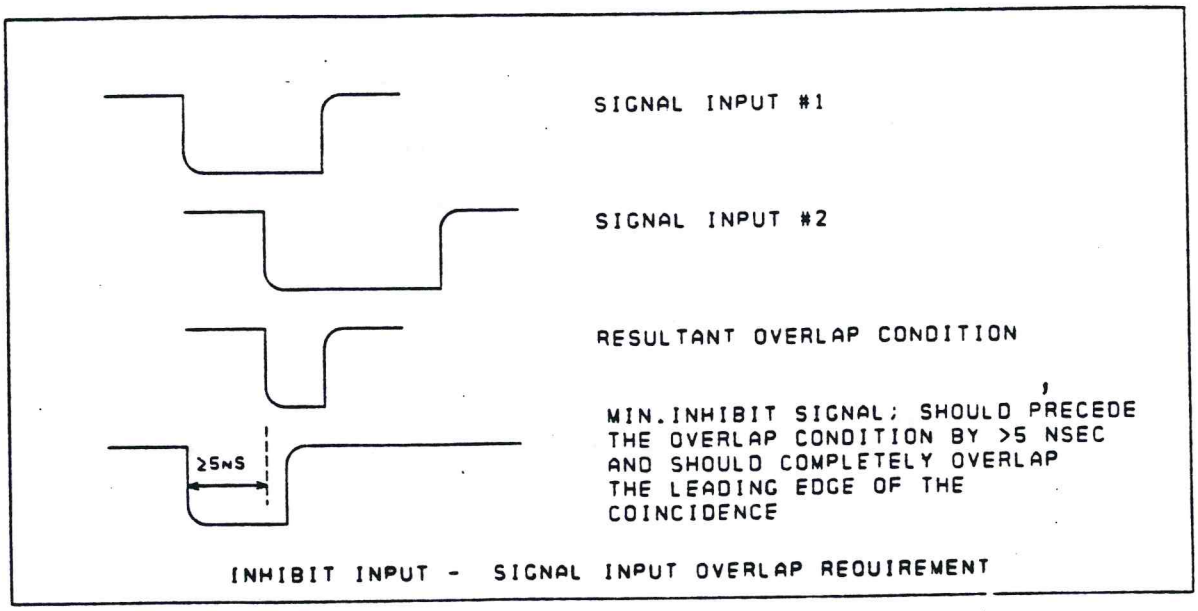
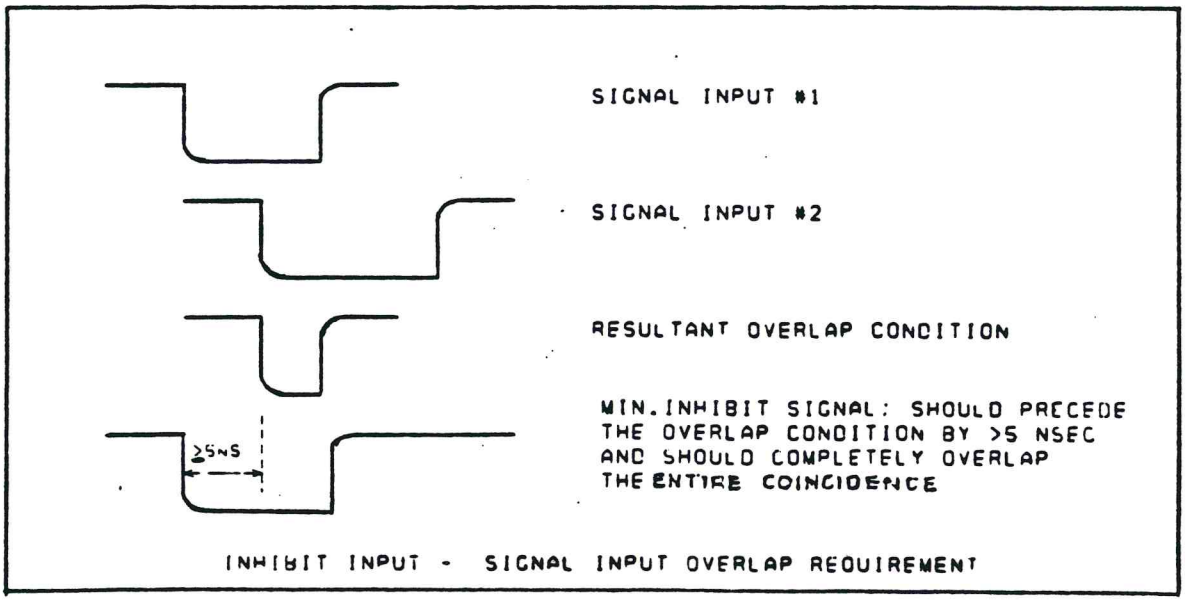
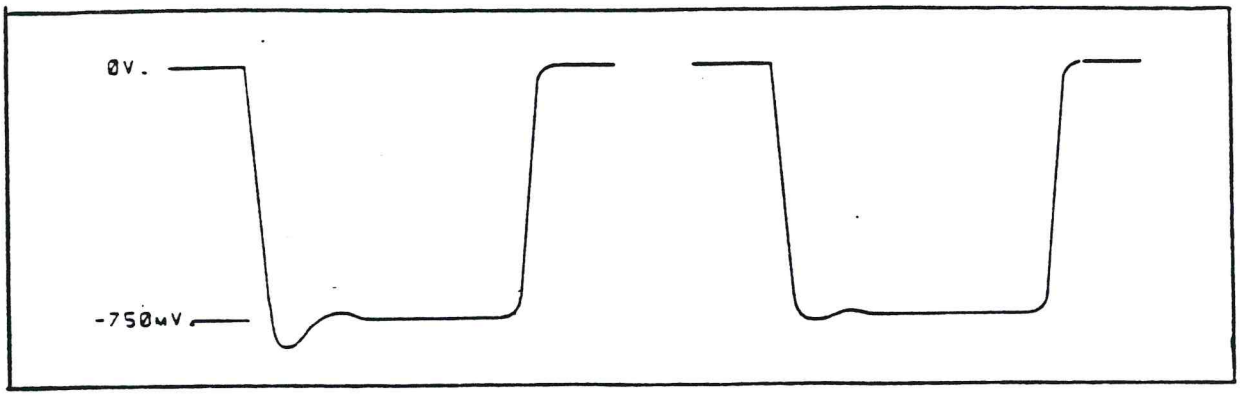

SIGNAL INPUT #1
SIGNAL INPUT #2
RESULTANT OVERLAP CONDITION
≥5nS
MIN. INHIBIT SIGNAL; SHOULD PRECEDE THE OVERLAP CONDITION BY >5 NSEC AND SHOULD COMPLETELY OVERLAP THE LEADING EDGE OF THE COINCIDENCE
INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

Figure 2.1

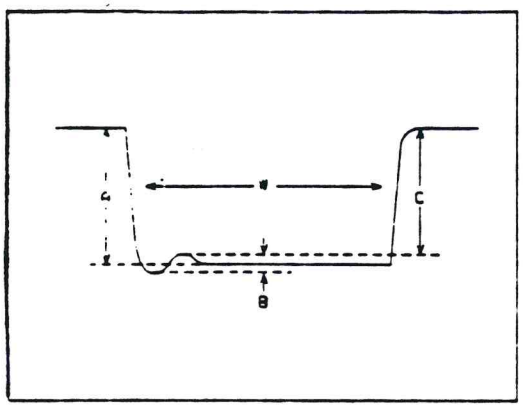

SIGNAL INPUT #1
SIGNAL INPUT #2
RESULTANT OVERLAP CONDITION
≥5nS
MIN. INHIBIT SIGNAL: SHOULD PRECEDE THE OVERLAP CONDITION BY >5 NSEC AND SHOULD COMPLETELY OVERLAP THE ENTIRE COINCIDENCE
INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT



Fully differential type current source output, adjacent output pair unterminated; tr ≈ 2.5 nsec; overshoot <15%.

Fully differential type current source output, output pair terminated; tr tr ≈ 2.0 nsec; overshoot <10%.

Figure 2.3



AMPLITUDE -700mV<A<-850mV.

OVERSHOOT: B<10% OF A. C DOES NOT REACH -600mV

RISETIME <2.5 NSEC.

FALLTIME <2.5 NSEC. AT MINIMUM WIDTH.

MINIMUM WIDTH. WMIN (FWHM) <5.0 NSEC.

MAXIMUM WIDTH. WMAX (FWHM) = 1 USEC.

Figure 2.4

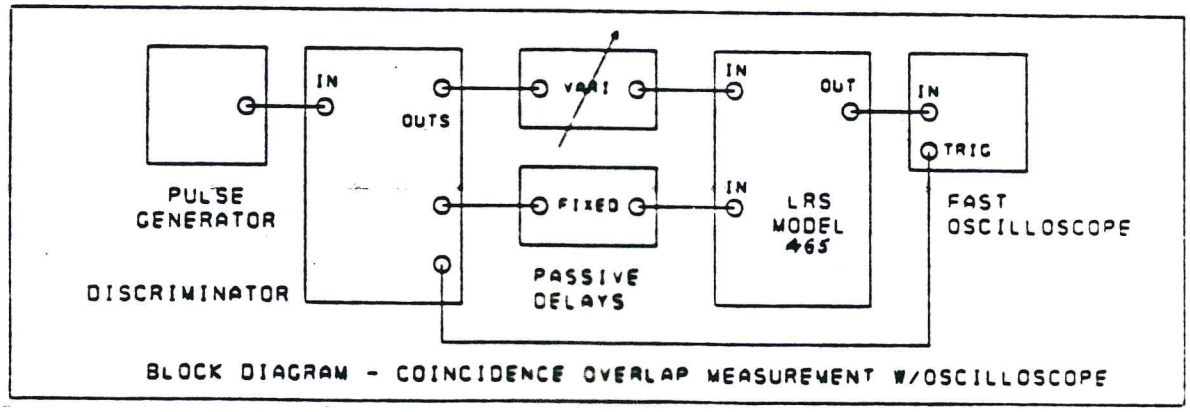


Figure 2.5

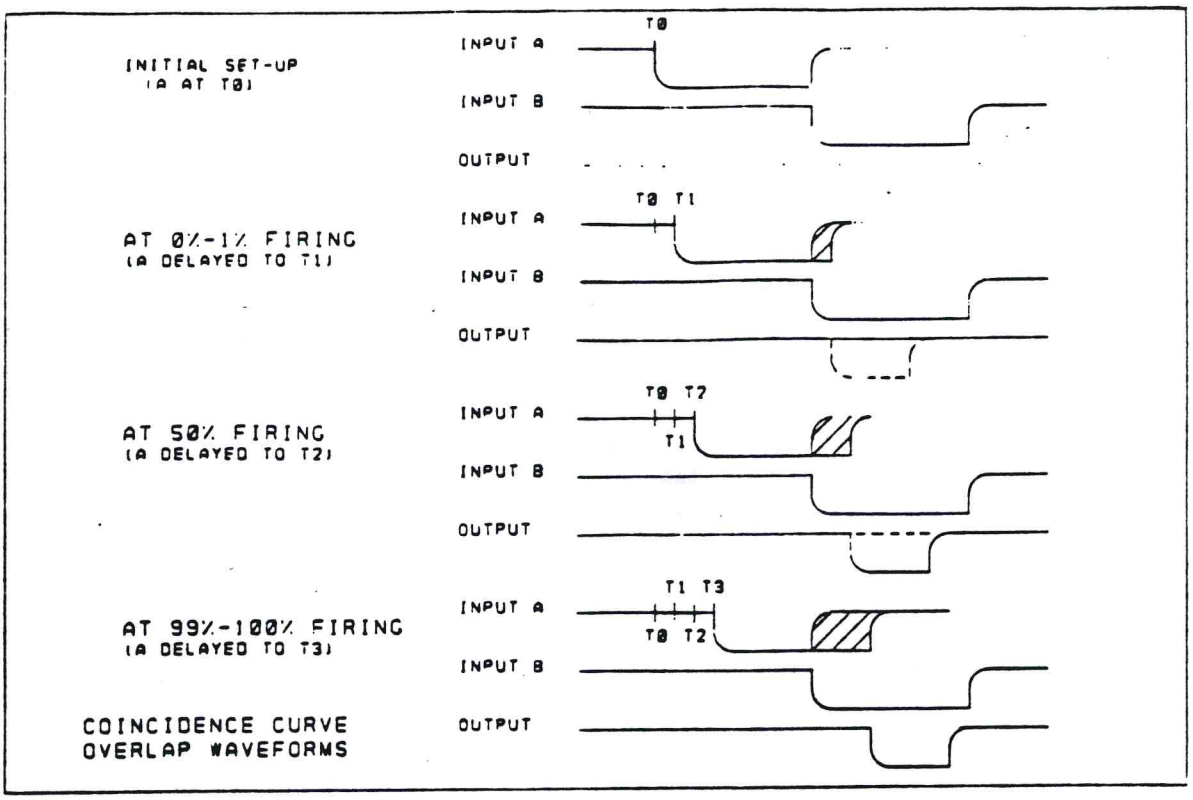


Figure 2.6

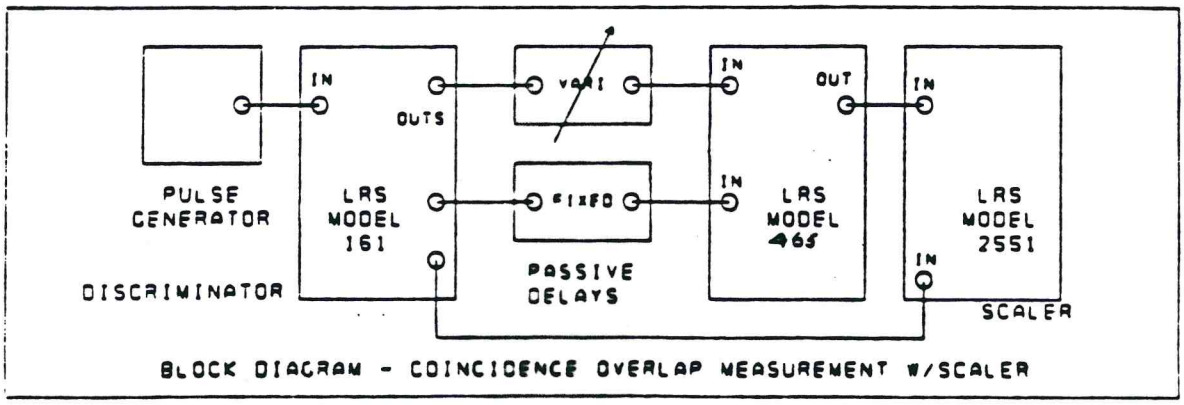


Figure 2.7

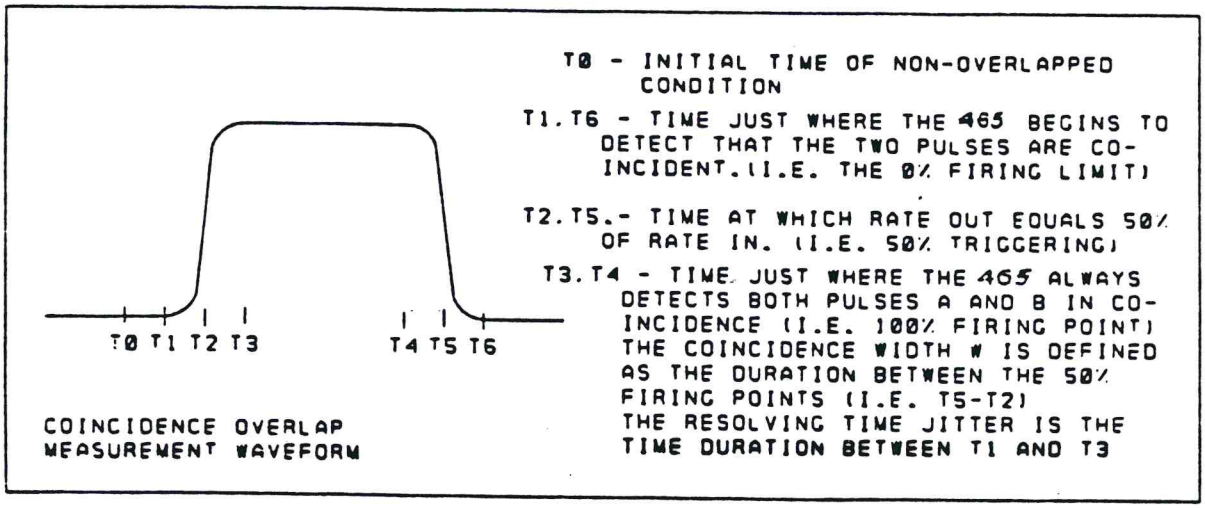

T0 T1 T2 T3
T4 T5 T6
COINCIDENCE OVERLAP
MEASUREMENT WAVEFORM
T0 - INITIAL TIME OF NON-OVERLAPPED CONDITION
T1.T6 - TIME JUST WHERE THE 465 BEGINS TO DETECT THAT THE TWO PULSES ARE CO-INCIDENT.(I.E. THE 0% FIRING LIMIT)
T2.T5.- TIME AT WHICH RATE OUT EQUALS 50% OF RATE IN. (I.E. 50% TRIGGERING)
T3.T4 - TIME JUST WHERE THE 465 ALWAYS DETECTS BOTH PULSES A AND B IN CO-INCIDENCE (I.E. 100% FIRING POINT)
THE COINCIDENCE WIDTH W IS DEFINED AS THE DURATION BETWEEN THE 50% FIRING POINTS (I.E. T5-T2)
THE RESOLVING TIME JITTER IS THE TIME DURATION BETWEEN T1 AND T3

Figure 2.8

SECTION 3

FUNCTIONAL DESCRIPTION

3.1 General

Each of the three channels of the Model 465 is composed of four basic sections: the Input Coincidence Stage, the Discriminator and Pulse-Standardizer Stage, the Timing or Pulse-Former Stage, and the Output Stage. A block diagram of the Model 465 can be seen in Figure 3.1, and a complete schematic can be found in the rear pocket of this manual.

3.2 Input Coincidence Stage

The input stage accepts up to four inputs, each of which can be switched such that the input is disconnected from the internal logic AND gate and a DC logic "1" continuously enables the internal input. The result is the equivalent of a switch-selectable 1-input, 2-input, 3-input, or 4-input AND. This is accomplished with four emitter-OR'd followers driving a discriminator stage which is biased at a negative voltage to compensate for the base-emitter drop of the transistors while sensing the NIM outputs at the full-width-half-amplitude point when a coincidence overlap occurs. In the special case where all four inputs are switch-disabled, to prevent the LINEAR (Overlap) output of the Model 465 from going high, a diode OR senses the condition and disables the input.

3.3 Discriminator and Pulse Standardizer

The discriminator stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator. The LD601C is functionally presented in Figure 3.2. The threshold level is set by the voltage bias on a fast differential amplifier which has positive feedback to provide regeneration at threshold. In actual operation the V_T input is tied to -0.8 V and the threshold level is determined primarily by the 19:1 voltage divider composed of the external 1.8 K resistor to -6 V (the 1N4448 diode is not conducting unless a veto bin gate is present) and the internal 100 Ω resistor. When an input signal applied to -IN from the Input is equal to the threshold voltage at +IN, the saturating amplifier output will begin to go positive. This will force +IN closer to 0 V, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (pin 6). The quiescent level should be nominally -2.4 V going to -1.6 V during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate and veto) must be off. (See following paragraph). Once the latch is set, a latch OUTPUT is available to start the Model 465 timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to

the AMPL. OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external selection of RC time constant and voltage levels at Pins 3 and/or 4. It is set approximately 3 nsec in the Model 465.

Each channel of the Model 465 has an independent front panel NIM-level veto input and a common rear connector bin gate input. The bin gate driver output is used to disable the three veto input stages, accomplishing the equivalent to a veto pulse causing the veto input circuit to current-switch. In either case, the normally off diode connecting this circuit to +IN of the LD601C will now conduct, pulling the +IN below the level of the -IN. This type inhibit is required for the Model 465 LINEAR (overlap) output, and it is important that the veto input completely overlap the coincidence overlap input to completely block the LINEAR output. The veto circuit is also connected to Pin 16 of the LD601C to accomplish a leading edge inhibit (requiring only an overlap of the leading edge of the coincidence overlap input) for the PRESET outputs of the 465.

Older Model 465 units use the LD601B hybrid, while more recent units use LD601C's. These two hybrids are identical and interchangeable.

3.4 Timing Stage

The timing or pulse-forming stage of the Model 465 utilizes three stages of MECL MC1692 receiver for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601 (via one MC1692 stage and the differential stage, composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front panel width potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604-ohm emitter resistor. The actual current is varied from near zero (for the 1 μsec maximum width) to about 10 mA for the 5 nsec minimum width. Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, T_W, sets the minimum width to 5 μsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The MC1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601 to the timing stage, as well as driving the preset output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601 output, independent of the delay encountered in initializing the timing stage. Before the 601 output is over, the timing capacitor is charged, causing the third amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing) until the

timing capacitor subsequently discharges to a sufficiently low level (approximately -2.0 V). At this point, (because of regeneration, the third amplifier promptly switches back to its quiescent off condition, termina

The Model 465 has one set of bridged outputs which completely bypass the timing stage, receiving their timing and drive directly from the AMPL. OUT of the LD601C. Thus, the output duration is just equal to the FWHM of the overlap of the input pulses.

3.5 Output Stage

One output stage of the Model 465 utilizes a conventional differential stage. This requires a continuous 32 mA of current of which 16 mA is quiescently available at the complementary back-terminated output connector. During an output pulse, the MC1692 will switch from the quiescent level of -2.4 V to a higher level of -1.6 V, causing the differential stage to switch the 32 mA current from the complementary half of the stage to the normal output connectors for the duration of the pulse. All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages. In all cases, the dual bridged outputs should both be terminated in 50 Ω for normal output amplitudes and shape.

The other output stage of the 465 is connected directly to the AMPL. OUT of the LD601. The voltage levels of the LD601 are the same as the MC1692, so the operation is as above.

3.6 Internal Power Supplies

Three internal power supplies are used to generate the -0.8, and -2.2, and -11.5 V which are special bias voltages used by the three channels. These stages provide voltage regulation and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but operating in a normal bin environment these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is DC sequenced on before the +6 voltage, the LD601C may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 V DC until the relay coil, operating from the +6 V DC is energized. This insures that

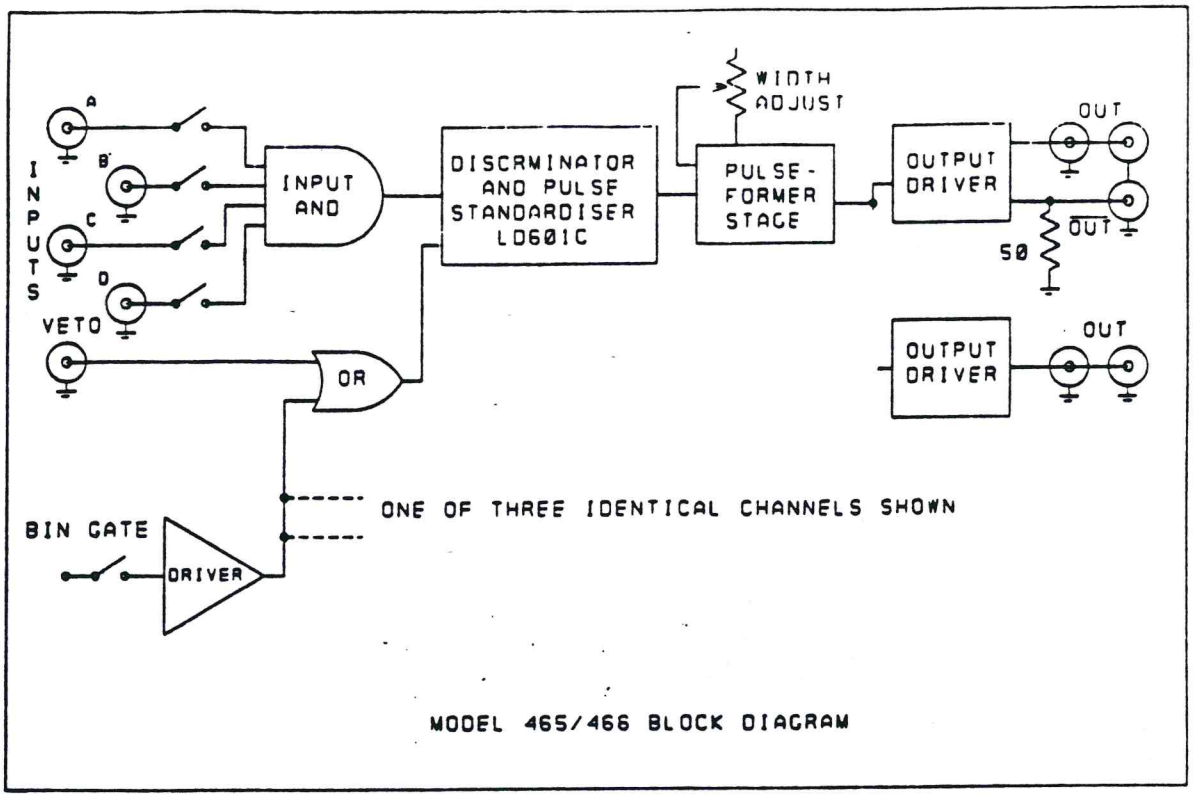


Figure 3.1

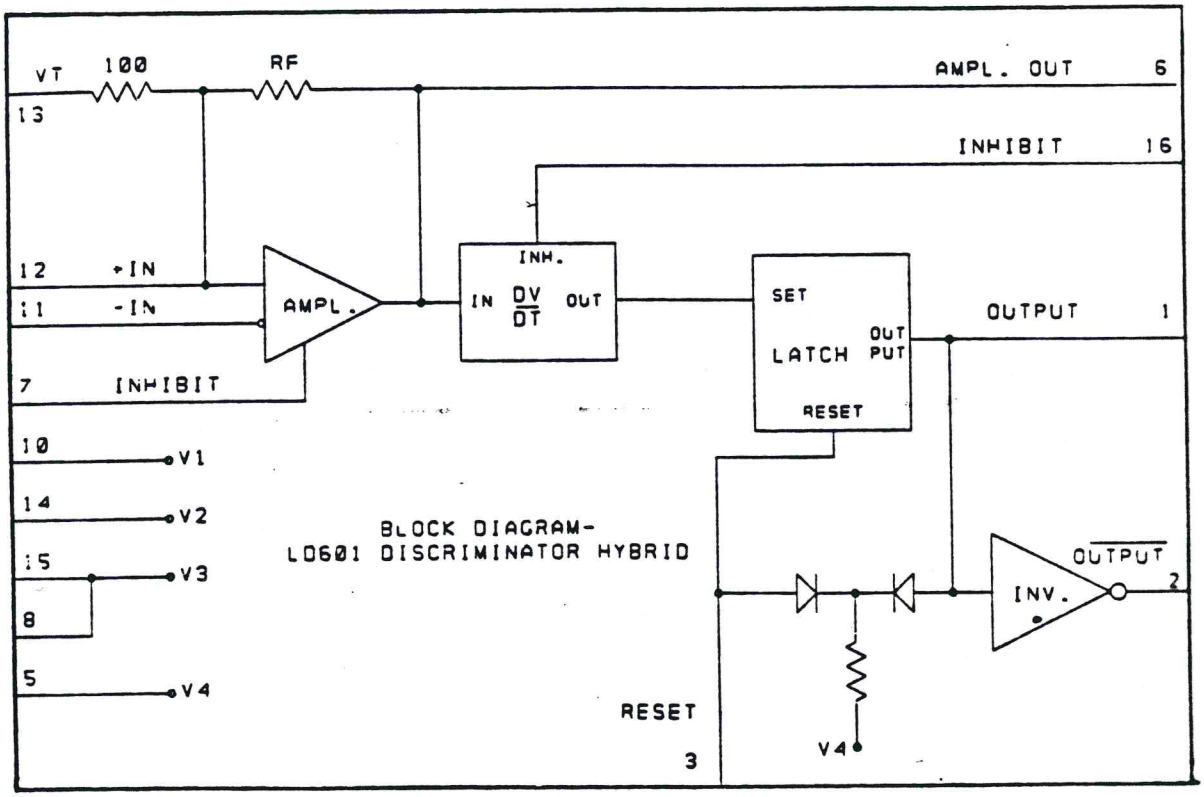


Figure 3.2

TECHNICAL INFORMATION

(PARTS LIST, SCHEMATICS)

PART NUMBER	DESCRIPTION REMARK	QTY PER
102245103	CAP CERA DISC 25V .01 UF	41
102444220	CAP CERA DISC 100V 22 PF	6
102944075	CAP CERA DISC 1KV 7.5 PF	12
102944150	CAP CERA DISC 1KV 15 PF	3
103276103	CAP CERA MONO X7R .01 UF	6
116515150	CAP DIP MICA DM10 15 PF	3
116515330	CAP DIP MICA DM10 33 PF	3
142824685	CAP TANT DIP CASE 6.8 UF	19
147147090	CAP ALUM METAL CAN 90 UF	1
158819001	CAP VARI CERA 3.5 - 18 PF QUANTITY 6 WILL BE CHARGED TO SEQ 300	9
161335027	RES CARBON FILM 2.7 OHMS	3
161335100	RES CARBON FILM 10 OHMS	1
161335101	RES CARBON FILM 100 OHMS	9
161335102	RES CARBON FILM 1 K	12
161335103	RES CARBON FILM 10 K	3
161335104	RES CARBON FILM 100 K	3
161335111	RES CARBON FILM 110 OHMS	6
161335123	RES CARBON FILM 12 K	3
161335151	RES CARBON FILM 150 OHMS	6
161335152	RES CARBON FILM 1.5 K	1
161335200	RES CARBON FILM 20 OHMS	3
161335201	RES CARBON FILM 200 OHMS	3
161335205	RES CARBON FILM 2 MEG	3
161335221	RES CARBON FILM 220 OHMS	3
161335222	RES CARBON FILM 2.2 K	3
161335301	RES CARBON FILM 300 OHMS	4
161335302	RES CARBON FILM 3 K	3
161335391	RES CARBON FILM 390 OHMS	9
161335392	RES CARBON FILM 3.9 K	3
161335470	RES CARBON FILM 47 OHMS	24
161335510	RES CARBON FILM 51 OHMS	6
161335511	RES CARBON FILM 510 OHMS	8
161335512	RES CARBON FILM 5.1 K	1
161335561	RES CARBON FILM 560 OHMS	4
161335621	RES CARBON FILM 620 OHMS	3
161335681	RES CARBON FILM 680 OHMS	3
161335682	RES CARBON FILM 6.8 K	1
161335751	RES CARBON FILM 750 OHMS	1
161335752	RES CARBON FILM 7.5 K	3
161335822	RES CARBON FILM 8.2 K	3
168531373	RES PREC RN55D 619 OHMS	3
168531389	RES PREC RN55D 909 OHMS	1
168531405	RES PREC RN55D 1.33 K	1
168531473	RES PREC RN55D 6.81 K	1
168531497	RES PREC RN55D 12.1 K	1
168531609	RES PREC RN55D 178 K	3
168531621	RES PREC RN55D 237 K	3
181457102	RES VARI CERMET 1 K	1
182537103	RES VARI CERMET 10 K	3
204021004	IC LINE RECEIVER MC1692L	3

PART NUMBER	DESCRIPTION REMARK	QTY PER
208011003	IC SINGLE OP AMP LM301AN	3
208034001	IC DUAL OP AMP UA747	3
230110003	DIODE SWITCHING FD 777	3
230110005	DIODE SWITCHING 1N4448	22
230110700	DIODE SWITCHING FD700	3
240225703	DIODE ZENER 3.6V 1N5989A	1
240225705	DIODE ZENER 4.7V 1N5992A SEND 3 PIECES FOR EACH UNIT TO RSD PRODUCTION FOR MATCHING.	4
253010811	DIODE SCHOTTKY HP2811	6
253010835	DIODE SCHOTTKY HP2835	31
270130002	TRANSISTOR NPN A 430 SEND TO RSD PROD. FOR MATCHING.	6
270130401	TRANSISTOR NPN A401	12
270170001	TRANSISTOR NPN 2N5770	13
270170002	TRANSISTOR NPN 2N5962	3
270190001	TRANSISTOR NPN PWR 2N3054	1
275150003	TRANSISTOR PNP 40319	1
275170002	TRANSISTOR PNP 2N5771	16
275190001	TRANSISTOR PNP PWR 2N3740	1
300010001	BEAD SHIELDING FERRITE	52
300050001	CHOKE FERRITE SINGLE LEAD	5
400010008	SOCKET IC SOLD TAIL DIP-8	3
400020014	SOCKET IC SOLD TAIL DIP-14	3
400030016	SOCKET IC SOLD TAIL DIP-16	6
402030000	CONN CO-AX LEMO	30
402030002	SPANNER NUT SMALL OD LEMO	30
402030003	GROUND LUG NONLOCK LEMO	21
405112001	CONNECTOR BLOCK (PIN)	1
405212002	GUIDE PIN (MALE)	1
405213001	GUIDE PIN (MALE)	1
405312001	GUIDE PIN (FEMALE)	2
405410016	CONNECTOR PIN (MALE)	7
405613001	CONNECTOR HOOD	1
412000801	SPACER CERAMIC 1/8" LONG	12
418000301	RETAINING CLIP	12
418000508	SHAFT NYLON	12
418000509	COUPLER	12
418241002	SWITCH SLIDE PB-10 4 STA	3
420212001	SWITCH SLIDE DPDT	1
500120002	TRANSIPAD "LARGE"	1
519350001	BUSHING NYLON	21
520000510	STANDOFF GLASS 8MM	82
521400018	SPACER ROUND #4 9/16	2
523400020	ROLL PIN SIZE #4 5/8 LONG	3
540103102	SIDE COVER NIM LEFT	1
540103103	SIDE COVER NIM RIGHT	1
540105001	BRACKET NIM WRAP SIZE #1	2
555611001	CAPTIVE SCREW 6-32	2

PART NUMBER	DESCRIPTION REMARK	QTY PER
555621002	CAPTIVE SCREW RETAINER	2
560440005	SCREW PHILIPS 4-40X5/16	8
560440012	SCREW PHILIPS 4-40X3/4	2
567256004	SCREW FLAT PHIL 2-56X1/4	4
568440003	SCREW FLAT PHIL 4-40X3/16	10
577400001	WASHER SHAKEPROOF SIZE 4	8
580440001	NUT HEX STANDARD 4-40	4
585141237	RIVET "POP" ALU 1/8X.237	2
590001022	WIRE TEFLON 7/30 BLK 22	1
590111022	WIRE TEFLON 7/30 BRN 22	1
590331022	WIRE TEFLON 7/30 ORA 22	1
590551022	WIRE TEFLON 7/30 GRN 22	1
590661022	WIRE TEFLON 7/30 BLU 22	1
590881022	WIRE TEFLON 7/30 GRAY 22	1
591101022	WIRE BUS TIN-COPP AWG 22	3
593910001	CABLE CO-AXIAL RG178B/U	10
710465013	PC BD PREASS'Y 465-466	1
720465013	FRONT PNL PREASS'Y 465	1
740000002	WRAPAROUND NIM 1 BIN GATE	1
LD601C	HYBRID DISC	3

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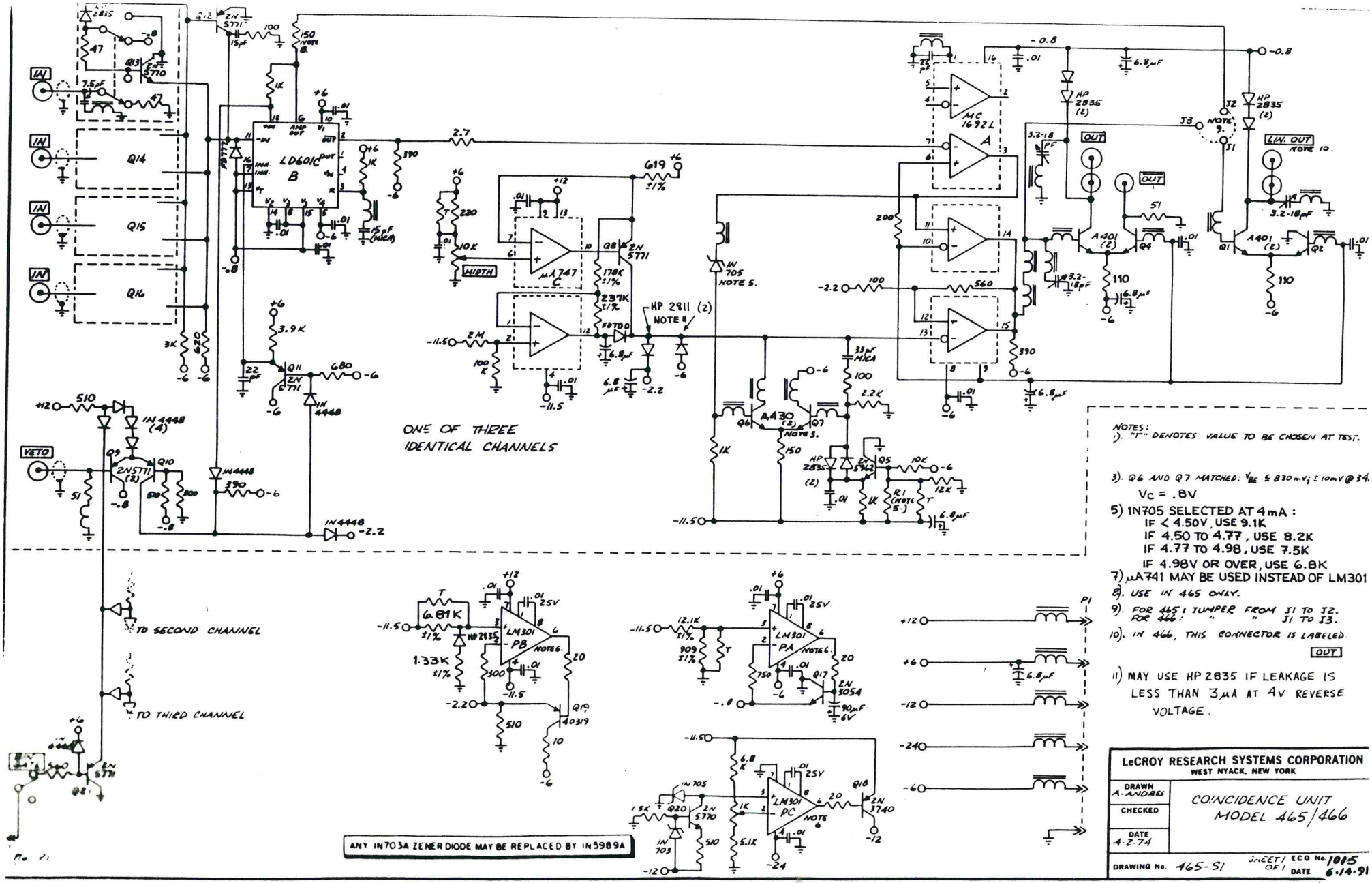

NOTES:
1). "T" DENOTES VALUE TO BE CHOSEN AT TEST.

3). Q6 AND Q7 MATCHED: V_{BE} ≤ 830 mV; ± 10mV @ 34 Vc = .8V

5) 1N705 SELECTED AT 4 mA :
IF < 4.50V, USE 9.1K
IF 4.50 TO 4.77, USE 8.2K
IF 4.77 TO 4.98, USE 7.5K
IF 4.98V OR OVER, USE 6.8K

7) μA741 MAY BE USED INSTEAD OF LM301

8). USE IN 465 ONLY.

9). FOR 465: JUMPER FROM J1 TO J2.
FOR 466: " " J1 TO J3.

10). IN 466, THIS CONNECTOR IS LABELED OUT

11) MAY USE HP 2835 IF LEAKAGE IS LESS THAN 3μA AT 4V REVERSE VOLTAGE.

ANY IN703A ZENER DIODE MAY BE REPLACED BY IN5989A

LeCROY RESEARCH SYSTEMS CORPORATION
WEST NYACK, NEW YORK

DRAWN A. ANDRES	COINCIDENCE UNIT MODEL 465/466
CHECKED	
DATE 4.2.74	
DRAWING No. 465-S1	SHEET 1 OF 1 ECO No. 1015 DATE 6.14.91