OPERATOR'S MANUAL

NIM MODEL 821

QUAD DISCRIMINATOR

CE

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(ECO 1018)

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GENERATION OF LOGIC PULSES FROM ANALOG SIGNALS

A discriminator generates precise logic pulses in response to its input exceeding a given threshold. Output pulses are of standard amplitude and of preset duration or proportional to the input rate. The threshold is a specific voltage of interest to the user (which can be set above some critical noise level or correspond to a physical quantity such as energy). In other applications, the threshold level can correspond to a certain level of integrated rates (coincidence events).

The output of a discriminator can be used to trigger or gate associated portions of the data collection system or to generate pulses which are to be counted. It may also be integrated into a complex logic system allowing sophisticated decisions to be made in real time.

LeCroy's family of NIM discriminators offers flexibility and versatility with features such as at least three outputs per channel, adjustable output width and variable threshold level settings. The low minimum threshold levels permit the use of lower gain photomultipliers, long input cables and often avoid the need for preamplifiers.

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LeCroy's NIM discriminators offer versatility, high speed, multiple input and high performance packaged in single-width NIM modules. All models have small double pulse resolution times and have updating capabilities to reduce dead time. Input signal threshold levels as well as output pulse widths are fully adjustable over a wide range for each channel. Each module offers at least three outputs per channel for added convenience and has a maximum counting rate exceeding 100 MHz. In addition, a common Veto or Inhibit is provided.

Each module offers a variable threshold from -30 mV (-15 mV for the Model 4608C) to -1 V via a front-panel screwdriver adjustment for each channel. The low threshold level is useful when working with signals directly from photomultipliers and other detectors. A monitor point is provided to permit measurement of the threshold level with a voltmeter, assuring accurate results even in varied operating environments. Threshold stability is 0.3%/°C or better. Low input reflections make these units less sensitive to multiple pulsing.

The Model 623B and the Model 821 operate at maximum rates of 100 MHz while the Model 4608C operates up to 150 MHz. All modules have updating capability which permits retriggering while an output from a previous input is still present. A second pulse, which exceeds threshold while an output is already occurring extends the present output by the preset width. However, if the second threshold crossing occurs within the double pulse resolution time, the module will not respond. This configuration is useful when the discriminators are used in DC coincidence logic.

The 821 and 4608C have a selectable Burst Guard operation. In this mode, the output is extended until the falling edge of the last pulse of the burst when input pulses are separated by less than the resolving time. This feature is particularly important when the module is used in Veto applications.

Although the actual width depends on the rate of input and the mode of operation, outputs of the modules are NIM Standard (see Application Note AN-34) level signals with minimum widths set by the front-panel controls. There are a minimum of three standard negative NIM outputs per channel. In addition, the 821 and the 4608C both have one complementary output per channel.

The 4608C includes a built-in test feature which simulates an input signal for each channel. The test feature is enabled with the receipt of a NIM level applied to the front-panel Lemo connector and permits rapid simultaneous testing of all channels.

In addition, the 821 and the 4608C can be used as single channel analyzers. See LeCroy Application Note AN-2 for further details.

SPECIFICATIONS

Model 623B

INPUT

Signal Inputs: Eight inputs via Lemo front-panel connectors, 50 Ω ±5%, protected to ±5 A for 0.5 μsec clamping at +1 and -7 V. Reflections: < 4% for input pulses of 2 nsec rise time. Threshold: -30 mV to approximately -1.0 V; front-panel screwdriver adjustable. Stability: < 0.2%/°C, 20°C to 60°C operating range. Threshold Monitor: 10:1 ratio of monitor voltage to actual threshold voltage. Hysteresis: 15 mV.
Inhibit: One input via a Lemo front-panel connector, 50 Ω ±5%, permits simultaneous fast inhibiting of all channels; requires a NIM level signal (< -600 mV). Must precede input by 6 nsec to inhibit. Minimum width 8 nsec. Effective width 5 nsec less than NIM input pulse.
Bin Gate: Slow gate via rear connector and rear-panel ON-OFF switch; rise times and fall times approximately 50 nsec; clamp to ground from +5 V inhibits; direct-coupled.

OUTPUT

Negative Outputs: Three NIM level outputs, 0 V quiescently, -800 mV during output. Duration is 6 nsec to > 150 nsec, continuously variable via front-panel screwdriver control. Rise time is typically 2.1 nsec; maximum 2.5 nsec. Fall time is approximately 4 nsec at minimum width, increasing with width setting up to 10 nsec maximum. At least two outputs should be terminated in 50 Ω for optimum pulse shape. Width stability maximum ±(50 psec +0.3%)/°C for temperature variation and ±0.1% per percent variation of supply voltage. Amplitude stability is better than ±0.1%/°C.

GENERAL

Maximum Rate: > 100 MHz, input and output.
Double Pulse Resolution: Better than 9 nsec.
Input-Output Delay: 11 nsec.
Multiple Pulsing: None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.

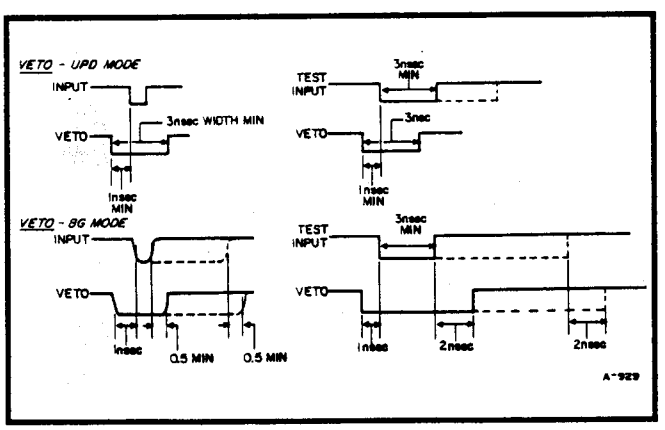
Model 821

INPUT

Signal Inputs: Four inputs via Lemo connectors, 50 Ω ±5% protected to ±5 A for 0.5 µsec, clamping at +1 and -7 V. Reflections: < 1% for input pulses of 3 nsec rise time. Offset 0 ±2 mV.
Threshold: -30 mV to -1.0 V; front-panel screwdriver adjustment. Stability: ≤ 0.2%/°C over 20°C to 60°C operating range. Threshold Monitor has 10:1 ratio of monitor voltage to actual voltage, ±5%. Hysteresis: 15 mV.
Veto: Front-panel connector permits simultaneous inhibiting of all channels; 50 Ω; requires NIM-level signal; direct-coupled, must overlap leading edge of input signal. Must precede input by approximately 5 nsec to inhibit. Minimum width 5 nsec.
Bin Gate: Slow gate via rear connector and rear-panel ON-OFF switch; rise times and fall times approximately 50 nsec; clamp to ground from +5 inhibits; direct-coupled.

OUTPUT

Negative Outputs: Two bridged pairs (0 mA quiescently, -32 mA during output). Amplitude limit of -1.2 V. Rise time < 2.0 nsec, fall time < 2.5 nsec typical but slightly longer on wider output durations. Width Stability is < ±0.2%/°C maximum. Duration of output depends on mode of operation selected by front panel switch.
Update Only Mode: 5 nsec to 1 µsec, continuously variable up to 600 nsec with a setting for 1 µsec via front-panel screwdriver control. (Narrower widths possible at slight expense of amplitude.)
Burst Guard Mode: Output duration is either equal to the time-over-threshold of the input signal or equal to the preset duration, whichever is greater. For input burst rates greater than the DPR of the unit, the output is equal to the duration of the burst.



Veto Input to 4608C with Updating and Burst Guard Operations.

Fast Negative Timing Output: Differential type current source (0 mA quiescently, -16 mA in 50 Ω during output). Rise time is typically 1.5 nsec.
Complementary Output: As above except levels opposite.

GENERAL

Maximum Rate: 110 MHz typical, input and output.
Double Pulse Resolution: < 9 nsec.
Time Slewing: < 1 nsec for input amplitudes 110% of threshold and above.
Input-Output Delay: 9.5 nsec, typical.
Multiple Pulsing: None; one and only one output pulse of preset duration is produced for each input pulse regardless of input pulse amplitude or duration.
Rate LED: One per channel. Indicates discriminator output; 10 msec stretching.

Model 4608C

INPUT

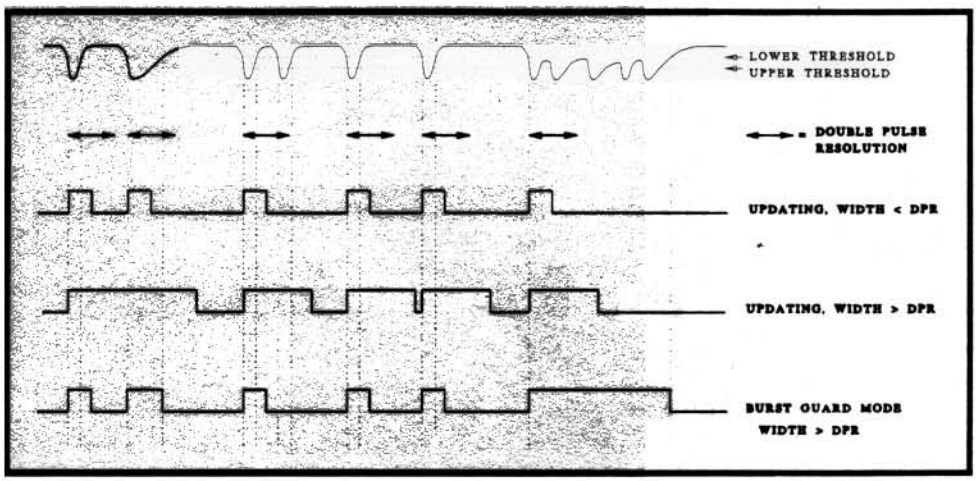
Signal Inputs: Eight inputs via Lemo front-panel connectors, 50 Ω ±5% protected to ±5 A for 0.5 µsec clamping at ±5 V. Reflections: < 4% for input pulses of 2 nsec rise time.
Threshold: -15 mV to -1 V ±2.5 mV or ±5%, whichever is greater. Stability: better than 0.3%/°C to 60°C operating range. Offset ±3 mV. Threshold Monitor: front-panel test point has 10:1 ratio of monitor voltage to actual voltage ±5%. Hysteresis: Typical 3.5 mV.
Test Input: One NIM input via a Lemo connector on the front-panel, 50 Ω ±5%, triggers all channels. Minimum width: 3 nsec. Maximum rate: 150 MHz.
Veto Input: One NIM input via a Lemo front-panel connector, 50 Ω ±5%, permits simultaneous fast inhibiting of all channels. Must precede input signal by approximately 1 nsec and overlap its leading edge in Update Mode or completely overlap input signal in Burst Guard Mode. Minimum duration: 3 nsec.

OUTPUT

Negative Outputs: Three outputs, NIM (0 mA quiescently, -50 mA ±6 mA during output, -800 mV into three 50 Ω loads). Amplitude limited to -1.2 V. Duration 4.5 nsec to > 100 nsec. Rise times and fall times less than 2 nsec. Width stability better than 0.3%/°C, 821, 4608C max.
Complementary Output: One output, NIM (16 mA ±2 mA quiescently, 0 mA during output). Duration, rise times, fall times, and width stability specifications are identical to those of negative outputs.

GENERAL

Maximum Rate: 150 MHz.
Double Pulse Resolution: Typical, 5 nsec.
Time Slewing: 500 psec for input amplitudes from 2x to 20x over threshold.
Input-Output Delay: < 18 nsec.
Test-Output Delay: < 18 nsec.
Multiple Pulsing: None, one and only one output pulse is produced for each input pulse regardless of input pulse amplitude and duration.
Burst Guard: A front-panel switch enables the Burst Guard or Updating operation for all channels.



Comparison of Updating and Burst Guard Modes with various fast input signals. DPR is the Double Pulse Resolution Interval set to minimum in this example.

NIM DISCRIMINATORS SELECTION CHART

	623B	821	4608C
INPUT			
No. of Inputs	8	4	8
Threshold	-30 mV to -1 V	-30 mV to -1 V	-15 mV to -1 V
GENERAL			
Packaging	Single-width NIM	Single-width NIM	Single-width NIM
Max. Rate	> 100 MHz	> 100 MHz	> 150 MHz
D.P.R.	9 nsec	9 nsec	5 nsec
Burst Guard	N/A	Selectable	Selectable
OUTPUT			
No. of Outputs	3 NIM	5 NIM, 1 $\overline{\text{NIM}}$	3 NIM, 1 $\overline{\text{NIM}}$
Width	6 nsec to 150 nsec	5 nsec to 600 nsec	4.5 nsec to 100 nsec
POWER			
-24 V	80 mA	85 mA	—
-12 V	195 mA	170 mA	—
-6 V	490 mA	690 mA	2.1 A
+6 V	240 mA	230 mA	0.6 A
+12 V	160 mA	15 mA	—
+24 V	—	—	0.01 A

1.3 Input Threshold Characteristics

1.3.1 Threshold Range

The threshold range of the 821 Quad Discriminator is -30 mV to -1 V. Because the front-panel screwdriver-adjustable potentiometer becomes increasingly sensitive as the threshold is increased, it eventually reaches a point (approximately -600 mV) beyond which it becomes difficult to set. Thus, beyond the -600 mV level it should be assumed that the discriminator will attain its maximum threshold setting of -1 V with negligible additional turning of the pot.

The low minimum threshold of the 821 makes it possible to use lower gain photomultipliers, lower phototubes and to drive PM signals over longer cable lengths than would be possible with higher thresholds. Compared with a -50 mV discriminator, for instance, utilizing RG-58 cable, the -30 mV discriminator would permit cable runs 66.7 feet longer than those permitted by a -50 mV discriminator for equal amplitude pulses. In addition, the low minimum threshold helps make it possible for one to back-terminate at the photomultiplier to absorb reflections and high amplitude noise. (In this case, the PM drives 25 Ω, the tube current is shared, and the amplitude is half that of the unterminated system).

1.3.2 Threshold Uncertainty

Often the threshold of a discriminator is assumed to be strictly that value which is written on a spec sheet or determined by a front-panel potentiometer. The actual value can be a strong function of environmental conditions. The external factors with the strongest effect upon the threshold value are temperature and power supply voltage.

Figure 1.1 indicates the threshold uncertainty due to these factors for Model 821 Discriminators.

1.3.3 Threshold Memory

In order for a user to be assured of a well defined threshold value, this value must remain constant for typical conditions encountered. If a discriminator's threshold is affected by previous events, it is said to have threshold memory. To the user this is an additional threshold uncertainty, since the discriminator's threshold for any given event depends upon the elapsed time from the preceding threshold crossing. In most discriminators, threshold memory (or second pulse sensitivity) becomes must larger as the pulse separation is reduced. The effect can be further aggravated by the amplitude of the initial signal. In some circuits a very large input can effectively paralyze the discriminator for a long period following the overload.

Figure 1.2 shows the threshold memory of the 821 Discriminator for a signal 20 dB over threshold and when the first input is just slightly above threshold.

Note that in both cases the threshold memory effect for the second pulse is within 6% of nominal for all spacing wider than 9 nsec. The second graph (i.e., the one more favorable to be discriminator) shows exceptionally clear response with virtually no effect in evidence above 10.5 nsec.

1.3.4 Threshold Calibration

Determination of the input threshold set by the front panel control has typically required the user to calibrate each change in setting with an external pulse source and oscilloscope. Newer discriminators offer a front panel test point whose DC level is proportional to the actual discriminator threshold. Not only does this allow rapid and simple determination of threshold, but it also allows the user to easily return the threshold level to a previously recorded setting. The convenience, and therefore the usefulness, of this feature is strongly dependent upon the characteristics of this monitor voltage, particularly its linear proportionality with the threshold setting. Figure 1.3 indicates the characteristic curve for the LRS 821 Discriminator.

1.3.5 821 Series Threshold Hysteresis

In 821 Discriminators, hysteresis is built into the front end, such that every threshold crossing will not trigger the discriminator unless the previous signal has returned to below approximately -15 mV. This avoids multiple pulsing due to, for example, fine structure riding on a flat-topped pulse. Note the examples in Figure 1.4.

In Example A of Figure 1.4, the pulse shape variations of the input pulse will not retrigger the discriminator even though they cross the threshold level at a time exceeding the double pulse resolution of the unit. In Example B, since the input signal does go back through -15 mV and then once again rises to exceed the -30 mV threshold level, two discriminator outputs would result.

1.3.6 -10 mV Minimum Threshold Option: By special request and at added cost, LRS can provide the 821 Discriminator (or 620 Series Octal Discriminator) with its minimum threshold set at -10 mV instead of -30 mV. Extreme care must be taken in the use of these modified units. The hysteresis level (described above) is only 5 mV for the -10 mV unit, such that any pulse entering with variation on it exceeding 5 mV may cause the discriminator to retrigger. Care should be taken that the discriminator is not fed by a circuit with any small DC level on it, and the less noisy the environment, the better. It is recommended that AC coupling be used if the input rates are low enough to permit it.

1.4 Input Reflections

Input reflections account for the majority of multiple-pulsing problems encountered by users. As discriminator thresholds have become lower, the amount of reflected signal required to retrigger the unit has decreased accordingly. Unless the percentage of input reflections is reduced along with the minimum threshold value, the user finds himself in the situation where multiple-pulsing negates the usefulness of a lower threshold. The input reflections of a discriminator effectively determine the allowable dynamic range of event or noise input signals.

A limited dynamic range may mean that minimum threshold values will have to be set higher to prevent multiple pulsing on noise or large (shower) event signals. In addition, high input reflections also limit the ability of a discriminator to be used to restandardize logic signals which have been degraded by long cables.

Figure 1.5 shows the maximum input voltage and allowable dynamic range as a function of discriminator input reflections.

As is evident, the Model 821 Discriminators offers a dramatic improvement in input reflection suppression over previously available discriminators. Because of the extremely low reflection coefficient (i.e., <2% for inputs of risetime ≥2 nsec), maximum input signal is more than a volt larger than it would be for a unit exhibiting the typical 10% reflections, offering five times increase in the discriminators' dynamic range.

1.5 Input Protection

The inputs of 821 Discriminator is protection to 5 A for 0.5 μsec, clamping at +1 and -7 V.

The DC protection is limited by the 0.25 watt dissipation limit of the input resistor, which can be assumed to offer protection against DC signals between -5 V and +5 V.

1.6 Bridged High Impedance Input Option (821Z)

The Model 821Z module is offered with a bridged high impedance input. The bridged high impedance inputs permit a user to drive only one cable from the photomultiplier to the discriminator to permit subsequent fast logic decision and pattern recognition to be performed. A popular method in the absence of this discriminator input option is to run two cables, one of which is from the dynode, which then must be inverted before the ADC or discriminator could accept it.

For this bridged input option, one output connector of an output pair is generally sacrificed. The wire normally feeding this output is tied to 50 Ω to permit normal operation of the other half of the output. A silver-colored ring is placed around this connector (as well as around the original input connector) when the unit is modified for this option to signify the fact that there are now two

input connectors. In standard usage, the silver-colored ring usually specifies complementary output.

1.7 Output Characteristics

1.7.1 Bridged Negative Outputs

The Model 821 Discriminator has two pairs of current source 50 Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. The 821, 821Z and 821BLP all have switched current outputs, requiring no quiescent current and permitting extremely low power dissipation in the total circuit. The switched current outputs maintain a risetime of <2.5 nsec and a reasonably clean shape, as long as care is taken to terminate at least one half of the other bridged output in that channel.

The actual shape of typical outputs from the 821 Series Discriminators is approximated in Figure 1.6.

Using the typical output pulse shape shown in Figure 1.7 as a visual reference, LRS output shapes for switched current outputs are set to adhere to the restrictions shown in that figure when one output from the adjacent pair is terminated.

1.7.2 Fast Negative Timing Output

The fast negative timing output on all 821 Series Discriminators is a full differential type current source output. Its name originates from the contrast in risetime (1.3 nsec vs. 2.5 nsec) between it and the other 4 negative outputs. Because the risetime is much faster, there is less timing inaccuracy that would be created by the normal "threshold" levels of subsequent time measuring circuits.

1.7.3 Complementary Output

The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to the fast negative timing output. It is a 50 Ω output with quiescent level at -16 mA, and logical 1 at 0 mA. Risetime and other characteristics are similar to that of the fast negative timing output.

1.7.4 Output Width

The output range of LRS Series 821 Discriminators in standard updating mode is 5.0 nsec to 1 μsec, continuously adjustable via a front panel potentiometer. The effect of the Burst Guard mode on output width is described in Section 1.7.7.

Because the potentiometer is very sensitive beyond 600 nsec, it is actually almost impossible to set the width between 600 nsec and 1 μsec. As a result, the specifications indicate continuous adjustment up to 600 nsec, with a 1 μsec setting at the far end of the pot.

1.7.5 Output Width Uncertainty

The output width of most discriminators is a nominal value determined by the front-panel potentiometer. Dispersion caused by variation in the discriminator input amplitude (jitter) results in a broadening of the skirts on the timing curve. In the LRS 821 Series Discriminators, this contribution is virtually non-existent as indicated in figure 1.8.

The other main contributions to output width uncertainty are a function of external conditions in a manner similar to threshold uncertainty. Variations in both temperature and voltage can cause significant changes in output width with undesirable consequences identical to dispersion caused by input amplitude.

Figure 1.9 indicates the uncertainty in output width of the 821 Series Discriminators as a function of reasonable variations in temperature and supply voltage.

1.7.6 Updating

The LRS 821 Series Discriminators all have the choice of Updating or Burst Guard modes. In an updating discriminator the output is extended if a second pulse comes in before the first output returns to zero, as long as the second pulse arrives at a time later than the double-pulse resolution of the unit. Thus, the second pulse will be seen by the front end even though an output is still present from the first signal, and that second pulse will cause a new output to be generated and added (in time) to the portion of the original output that already occurred.

1.7.7 Burst Guard

In the Burst Guard mode, the output of the front end is OR'd with the conventional mode output. Thus, for input pulses arriving at a rate which exceeds the double-pulse resolution of the unit, the discriminator output duration will be equal to the time interval between the first leading edge threshold crossing and the last trailing edge threshold recrossing, or the preset output width, whichever is greater. This feature is especially important in veto applications, where it is desired to keep the discriminator output on when the detector is being hit by unwanted and unmeasurable high rates. A discriminator without Burst Guard would see the first pulse and generate the preset output width, but would return to the quiescent level or trigger only randomly for subsequent pulses separated by less time than the DPR of the unit. Burst Guard assures a logical 1 output level during these high rate bursts.

It is important to note that propagation delay through the discriminator is approximately 1 nsec less in the Burst Guard mode. The output width in this mode will be then correspondingly longer, since the output leading edge appears sooner.

1.7.8 Usage of Bridged Negative Outputs Driving a Single Cable

In applications where it is necessary to drive very long cable lengths from a discriminator output, it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively channels all 32 mA into the one cable, giving a double amplitude output. It is important to know that 821 Series Discriminators all have clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 V. It cannot be assumed, therefore, that the -32 mA into one 50 Ω cable will give a -1.6 V output signal.

1.8 Timing Characteristics

1.8.1 Maximum Rate

Maximum continuous pulse train (CW from RF terminology) rate capability of the 821 Series Discriminators is guaranteed at 100 MHz. Typically, the maximum rate is 110 MHz, with some units being capable of operation up to 120 MHz for small bursts of input pulses.

1.8.2 Double-Pulse Resolution

The speed of a discriminator is practically defined by its double-pulse resolution or the time between the leading edges of the most closely spaced pulse pair for which the discriminator produces two distinct output pulses. Although simple in concept, this specification can be misleading unless the input conditions are precisely defined and performance fully specified. Characteristic curves which describe double-pulse resolution for the 821 series are in Figure 1.10 - 1.12 (discussed below).

Double-Pulse Resolution vs Input Amplitude:

The double-pulse resolution of some discriminators is a strong function of the amount of overdrive. Typical anomalies include substantial increases in amplitude to achieve minimum pulse pair resolution (which is an effective threshold increase as a function of rate) and/or limited input dynamic range over which the discriminator adheres to specifications. A third effect is equivalent to tracking error. Does a discriminator have 8 nsec DPR if it never produces output pulses spaced more closely than 10 nsec apart? In some cases, this effective timing error can be much larger than time shift due to intrinsic slewing or risetime dependent slewing. The figure below shows the minimum double-pulse resolution of the LRS821 Series Discriminators as a function of input amplitude from threshold to 10X threshold.

It is worth noting that the 821's maintain a DPR of under 9 nsec for all inputs over the 10:1 dynamic range. Although not featured as part of the general specifications, the double-pulse resolution is much better than specified over most of the measured dynamic range. Also significant is the absence of tracking error at the limit of the discriminator's input performance. Throughout the measured range, the time shift of the output averages 2.54% or approximately 200 ps.

Double-Pulse Resolution vs Input Width:

The DPR of a discriminator is a strong function of the duration of the first pulse in an input pair, since this width affects the recovery time allowed the discriminator input stage between the two pulses. If the double-pulse resolution is not linear with input width, it may mean that the discriminator will not respond to the second pulse following an overload photomultiplier signal. The double-pulse resolution vs input width of the 821 Series Discriminators is shown in figure 1.11. This figure demonstrates that the discriminator's response is linear with input width and has a fixed recovery time of 4 nsec following an input of any duration.

1.8.3 Tracking Error

The ability of a discriminator to be used for precise timing (coincidence or TOF) in an environment which encounters narrow pulse pair separations is demonstrated by considering the time shift (or tracking error) introduced as the time interval between successive inputs is reduced. In an experiment, tracking error is equivalent to time dispersion as a function of input rate. For many experiments, this can be critical, since it is often in high rate situations that the best timing resolution is required. Tracking error of the 821 Series Discriminators as a function of input pulse spacing is indicated in figure 1.12.

1.8.4 Slewing

For input rates which do not tax the double-pulse resolution of the discriminator the most important characteristic which defines the fidelity of the discriminator output to the time information in the input signal is slewing. This is defined as variation in the input-to-output time delay of a discriminator with input amplitude. The net measured slewing yielded by a discriminator has two components, one contributed by the discriminator itself (intrinsic slewing) and the other dependent upon the input risetime.

Intrinsic slewing might be defined as the slewing measured with a delta function input. Risetime dependent slewing arises from the fact that the discriminator fires earlier on the leading edge of a large pulse of finite risetime than on one of smaller amplitude with the same risetime. For an extreme range of pulse heights, the maximum contribution is equal to the 0 to 100% risetime of the pulse

With most discriminators the largest portion of the slewing occurs in the amplitude region just above threshold. Threshold being defined as the input amplitude that produces 50% triggering. Slewing specifications are frequently given over an input amplitude range from threshold to a specified overload factor (such as 10X threshold).

No commonly accepted standard exists for measuring the slewing characteristics of discriminators. One technique which LRS considers relevant to describing a discriminator's timing characteristics is to

obtain a time spectrum of shift in input-output delay when a uniform spectrum of pulse heights from below threshold to many times threshold is used to drive the discriminator. Such an input spectrum constitutes a relatively severe test of the discriminator's timing performance for it contains a relatively higher proportion of near threshold pulses than does a usual beam-derived photomultiplier spectrum. It takes into account all aspects of discriminator slewing performance and presents their combined effect in terms of a time dispersion curve as indicated in figure 1.13.

From figure 1.13, an integral curve such as shown in figure 1.14 may be plotted indicating the percentage of the linearly distributed input events with time shift <S.

Figures 1.13 and 1.14 were plotted from computer-generated runs on several Model 821 channels using a linear input amplitude distribution from 0 to -240 mV. System time resolution was <25 ps. Data in both curves was not corrected for input risetime of 500 ps. The FWHM of the time dispersion curve under these conditions is 125 ps.

1.9 General

1.9.1 Packaging

The 821 Series Discriminators are all packaged in a #1 NIM module with Lemo-type connectors. Due to front panel space limitations, the 821's are not offered with BNC.

1.9.2 Current Requirements

The -6 V current usage of the 821 permits the use of only 7 modules per standard 96-watt NIM bin offering 5 A of ±6 V. In applications requiring the use of many 821's, the user may find it advantageous to have a higher power NIM bin (such as the LeCroy Model 1002 which can provide up to 10 A for each 6 V supply).

Power dissipated by the 821 is approximately 10 watts, so it is highly recommended to use a NIM bin with higher power dissipation limits than the standard 8 watts per NIM slot or to take care to carefully choose low power modules for the remaining slots in the bin, or to perhaps leave some NIM slots blank.

1.9.3 Recommended Use of the NIM Power Bins

It is highly recommended that any NIM bin be kept at as constant a temperature as possible, using air conditioning and fans to assure air flow through all modules in every bin. Elimination of large temperature variations removes the possibility of temperature drift effects upon modules and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for

days under power between initial test and final test, it is recommended that subjecting any modules to adverse operating conditions be avoided when possible.

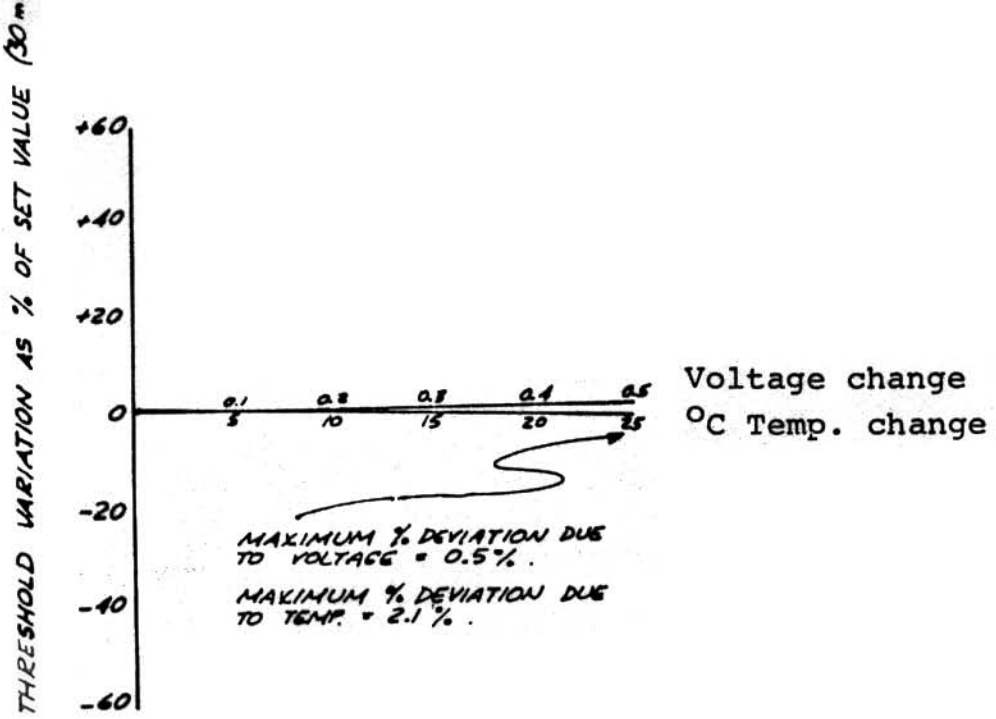


Figure 1.1

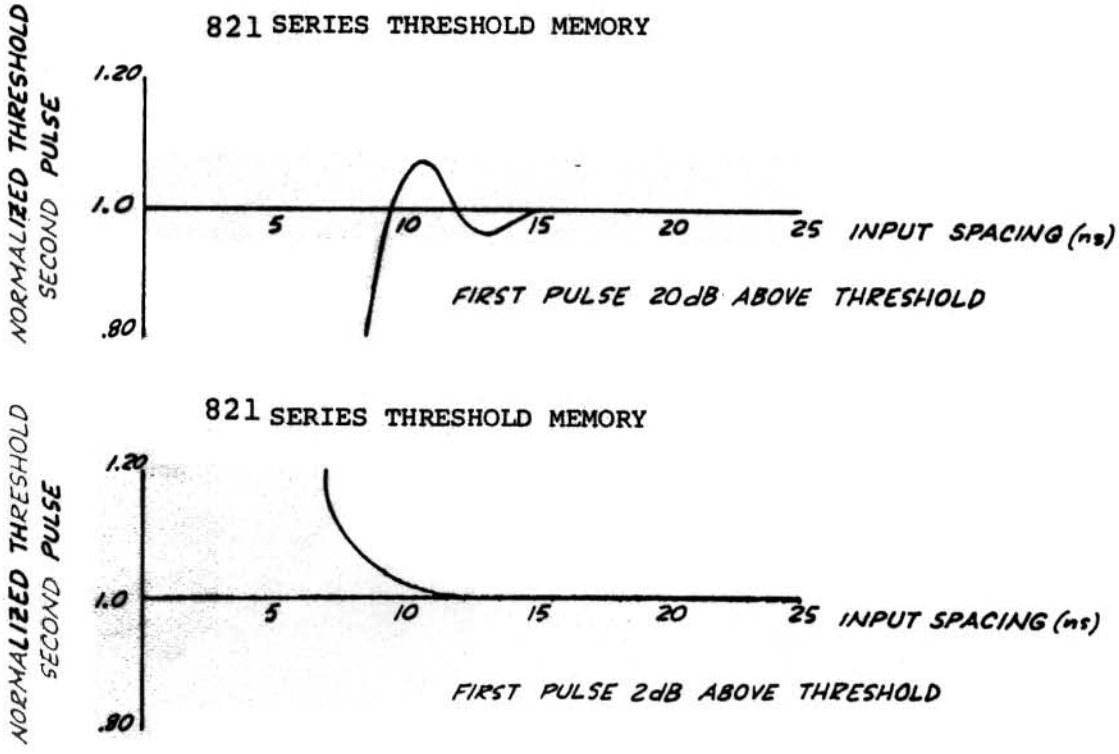


Figure 1.2

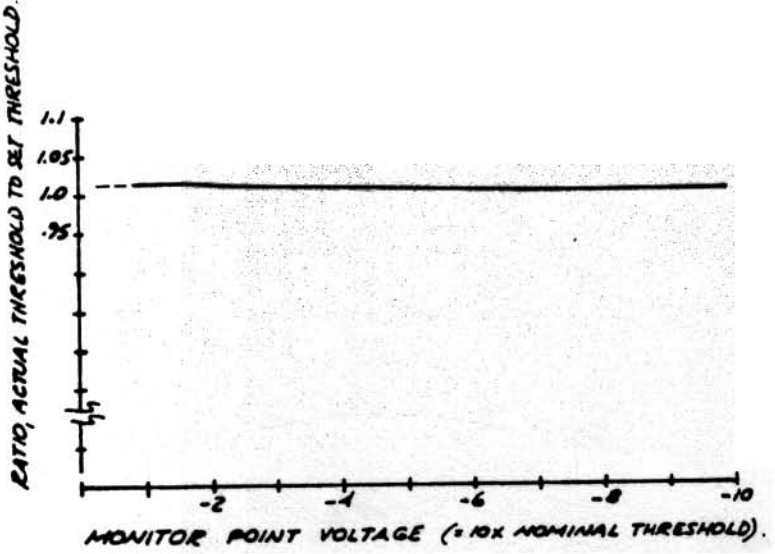


Figure 1.3

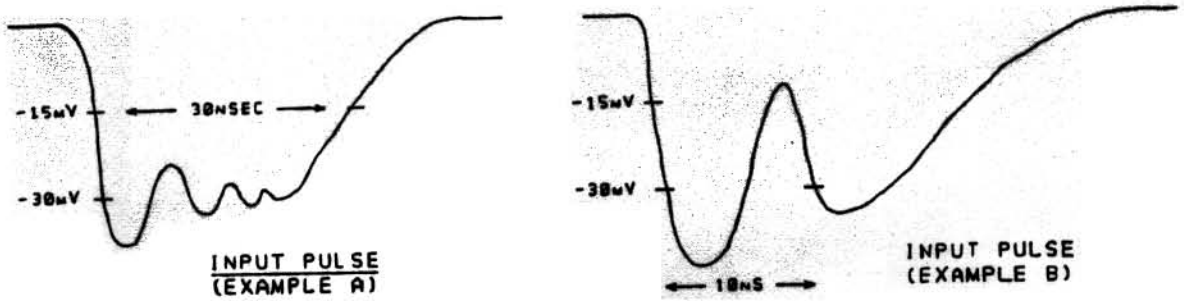


Figure 1.4

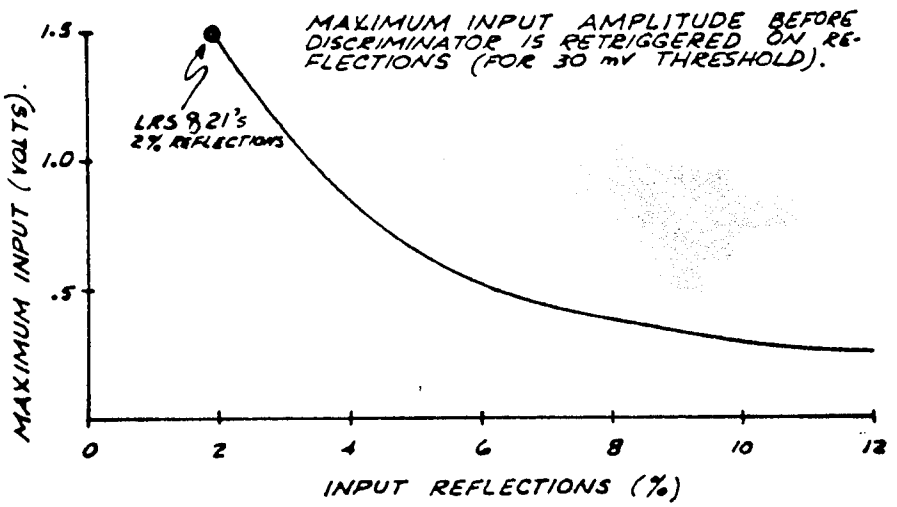


Figure 1.5

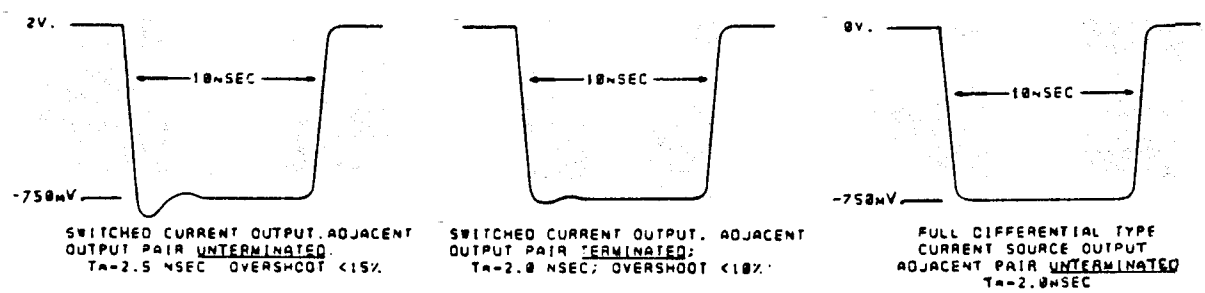
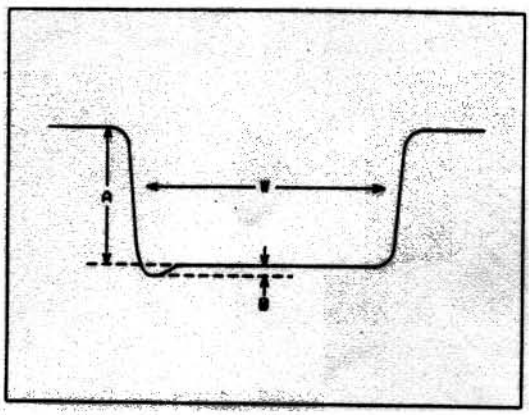


Figure 1.6



AMPLITUDE -700mV≤A≤-800mV

OVERSHOOT B≤10% OF A

RISETIME: TYPICALLY ≤2.0 NSEC.

FALLTIME: TYPICALLY ≤2.5 NSEC. AT MINIMUM WIDTH.

MINIMUM WIDTH: WMIN (FWHM) ≤5.0 NSEC

MAXIMUM WIDTH: WMAX (FWHM) = 1 USEC

Figure 1.7

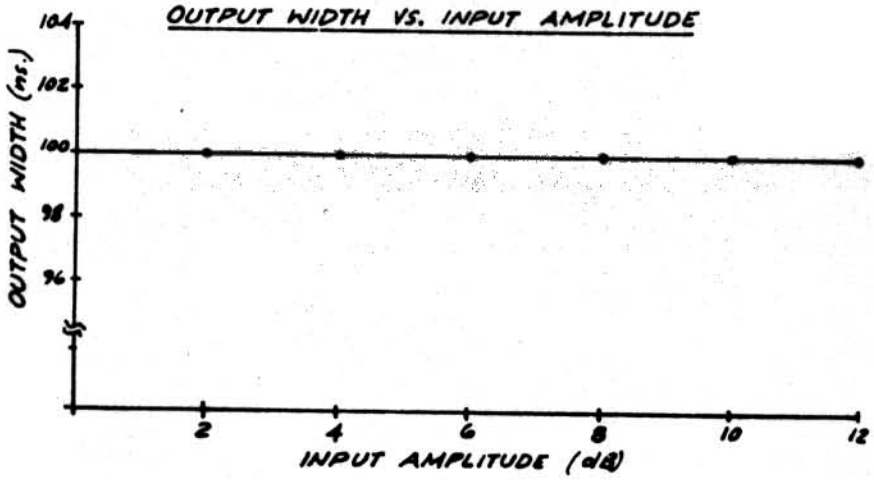


Figure 1.8

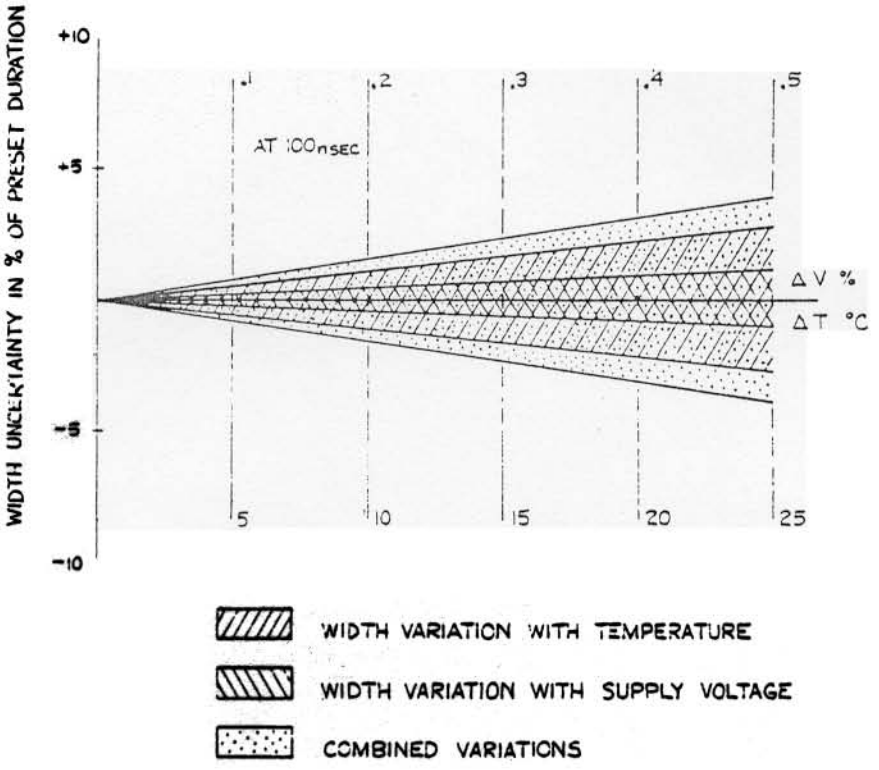


Figure 1.9

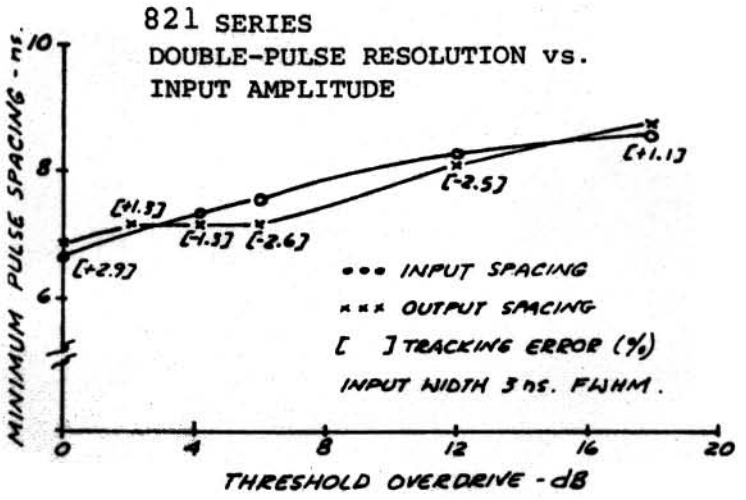


Figure 1.10

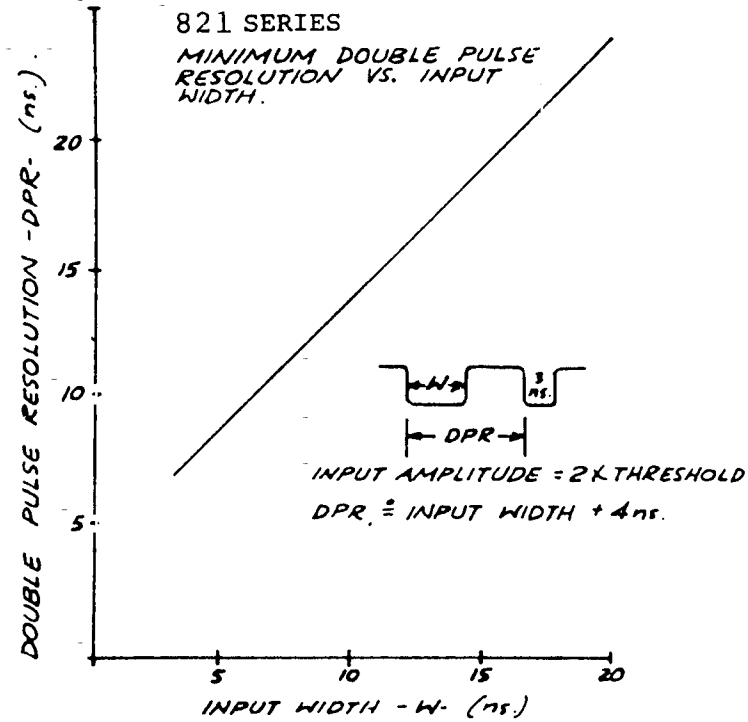


Figure 1.11

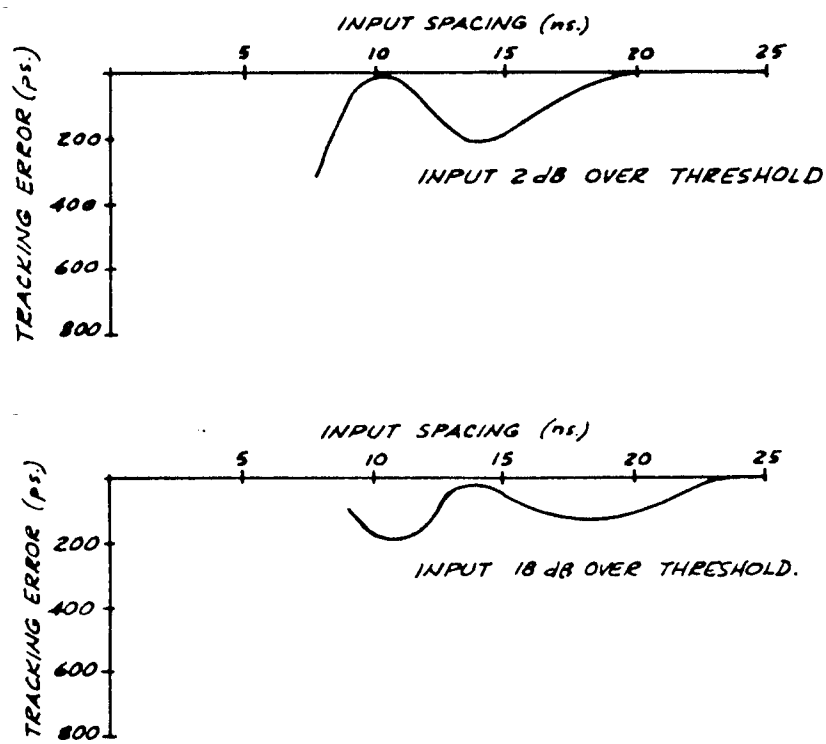


Figure 1.12

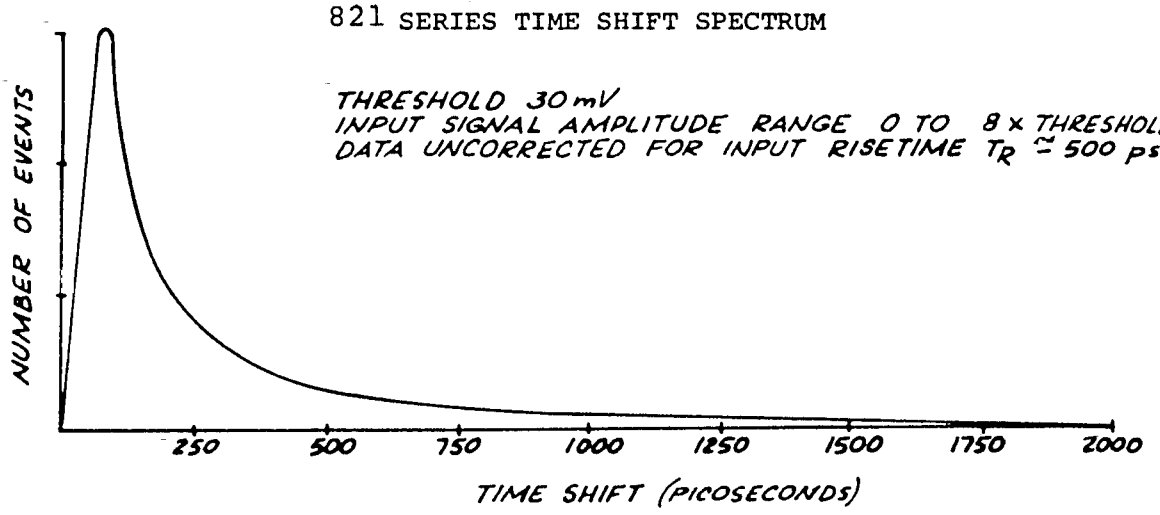


Figure 1.13

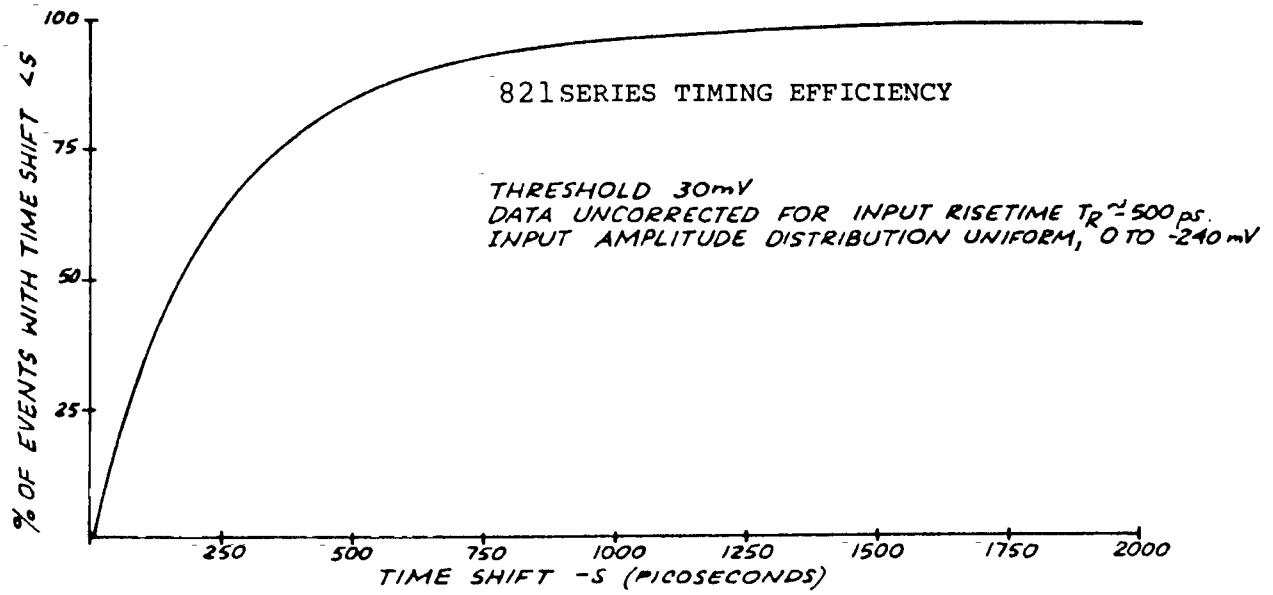


Figure 1.14

FUNCTIONAL DESCRIPTION

2.1 General

Each of the four channels of the 821 Series models is composed of three basic sections: the input and discriminator stage, the timing or pulse-former stage, and the output stage. A block diagram of the 821 Series is in Figure 2.1 and a complete schematic of a specific model can be found in the rear pocket of this manual.

2.2 Input and Discriminator

The input and discriminator stage is based on the LRS Model LD601 hybrid. This unit contains all of the circuitry of the discriminator with the exception of the input termination and input protection. The LD601 is functionally presented in Figure 2.2. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small amount of positive feedback to provide regeneration at threshold. In actual operation the V_T input is grounded, and the threshold level is determined by the 10:1 voltage divider (composed of the external 909 Ω and internal 100 Ω resistors) operating from a voltage which is set by a front-panel potentiometer and monitored at the front panel test point.

The measured voltage will be 10 times the actual threshold voltage. When an input signal applied to -IN is equal to the threshold voltage at +IN, the amplifier output will begin to go positive. This will force +IN closer to 0 V, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (Pin 6) and is used to do the Burst Guard mode. The quiescent level should be nominally -2.4 V going to -1.6 V during the pulse. The leading edge of this output sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate) must be off. The required level at Pins 7 and 16 of the LD601 must be 0 to -1.6 V to enable, and -2.5 to -6.0 to disable. The purpose of the first inhibit is to avoid generating a low level transient at the output associated with the leading edge of an amplified input pulse inhibited at the dV/dt stage only. (The common bin gate driver shifts this so that 0 V at the Bin Gate input will inhibit, greater that +3 V will enable). Once the latch is set, a latch OUTPUT is available to start the 821 Series timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external selection of RC time constant and voltage levels at Pins 3 and/or 4. It is set at approximately 3 nsec in the 821 Series models.

Two trim resistors T1 and T2 are associated with this stage. (See enclosed schematic). T1 sets the minimum threshold. T2 calibrates the LD601C threshold to the test point voltage at its respective channel. If the LD 601C is changed, T2 will probably require trimming.

2.3 Timing Stage

The timing or pulse-forming stage of the 821 Series utilizes three stages of MC1692 MECL receivers for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601C (via one MC1692 stage and the differential stage, composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604 Ω emitter resistor. The actual current is varied from near zero (for the 1 μsec maximum width) to about 10 mA (for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, Tw, sets the minimum width to 5 nsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the timing capacitor. The 1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601C to the timing stage, as well as driving the output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the LD601C output, independent of the delay encountered in initializing the timing stage. Before the LD601C output is over, the timing capacitor is charged, causing the third 1692 amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing) until the timing capacitor subsequently discharges to a sufficiently low level (approximately -2.0 V). At this point (because of regeneration) the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

The Model 821 has an optional Burst Guard mode. This mode is activated by a front-panel switch which enables a fourth stage of the 1692. When enabled, it receives its input from the AMPL OUT of the LD601C. When the input rate exceeds the DPR capability of the LD601, this point begins to "pump up" such that it does not fall below the ON level of the 1692. Its output level is wire-OR'd with the feedback input of the 1692 which is driven from the timing stage to appear finally to the output stage as an "ON" level for the duration of the "Burst" at the front panel input.

2.4 Output Stage

The output stage utilizes two different types of circuits. The single normal and complementary outputs use a conventional differential stage. This stage requires a continuous 16 mA of current which is quiescently available at the complementary output connector. During an output pulse, the MC1692 will switch from the quiescent level of -2.4 V to a higher level of -1.6 V, causing the differential stage to switch the 16 mA current from the complementary to the normal output connector for the duration of the pulse. The other two pairs of outputs each supply 32 mA of current during the pulse, because at this time the bases of the two A430 transistors are at -1.6 V. The emitters are therefore at about -2.4 V. This places about 600 mV across each 18 Ω emitter resistor, and the resulting 32 mA will be available at each output connector pair for the duration of the pulse. Quiescently, the bases of these transistors are at -2.4 V; therefore, there is only -600 mV drop available for V_{BE} so the transistors are off, resulting in a substantial power saving. All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, even on a single output stage, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages.

2.5 Internal Power Supplies

Four internal power supplies are used to generate the -0.8, -2.2, -3.0, and -11.5 V which are special bias voltages used by the four channels. These stages provide voltage regulation and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but during operation in a normal bin environment these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is sequenced on before the +6 voltage, the LD601 may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC is energized. This insures that the +6 is up before the -6 in any power-on sequence.

2.6 Programming the 821BLP

The Model 821BLP is a standard 821 which has the critical threshold and width control voltages brought directly out to an added rear panel 20-pin connector. Internal high frequency filtering is provided (i.e., T_{RC} + 0.01 seconds) on each input.

The remote programming voltage source must be low impedance (ideally less than 100 Ω). When using the front panel potentiometers, the rear panel programming should be removed.

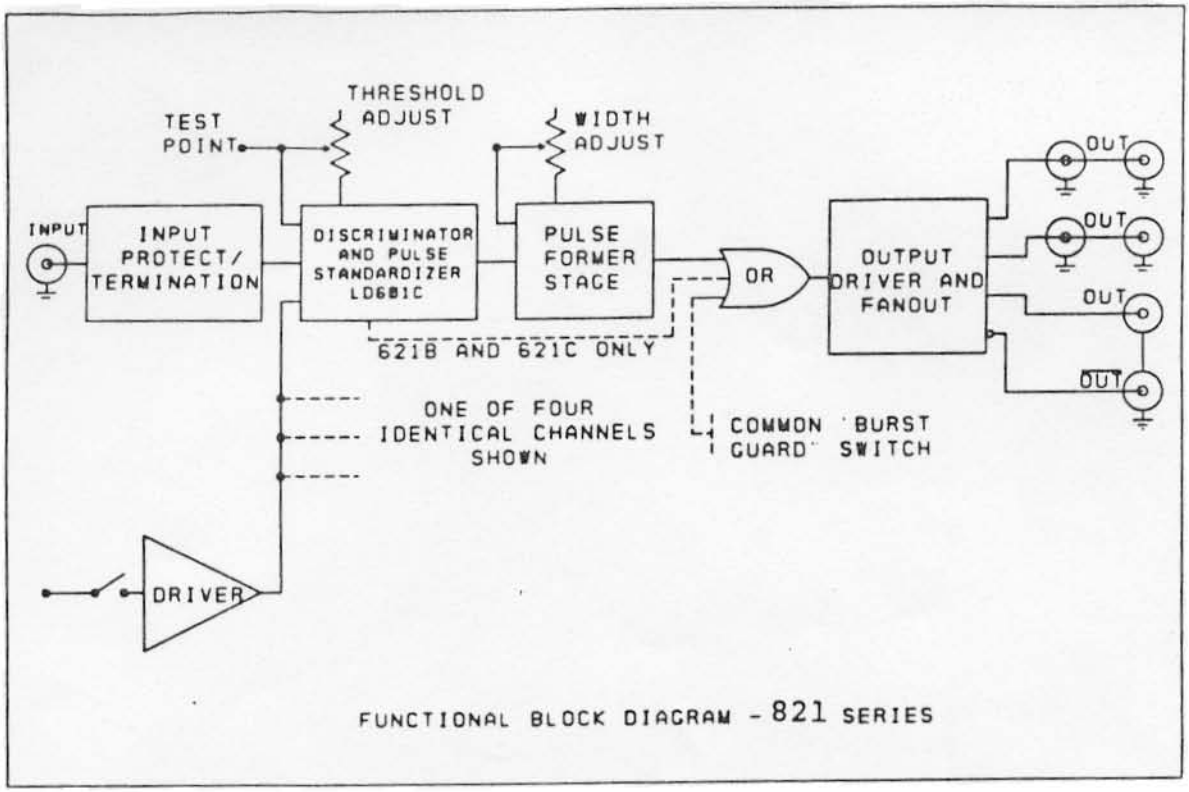

THRESHOLD ADJUST
TEST POINT
WIDTH ADJUST
INPUT
INPUT PROTECT/ TERMINATION
DISCRIMINATOR AND PULSE STANDARDIZER LD681C
PULSE FORMER STAGE
OR
OUTPUT DRIVER AND FANOUT
OUT
OUT
OUT
OUT
621B AND 621C ONLY
ONE OF FOUR IDENTICAL CHANNELS SHOWN
COMMON BURST GUARD SWITCH
DRIVER
FUNCTIONAL BLOCK DIAGRAM - 821 SERIES

Figure 2.1

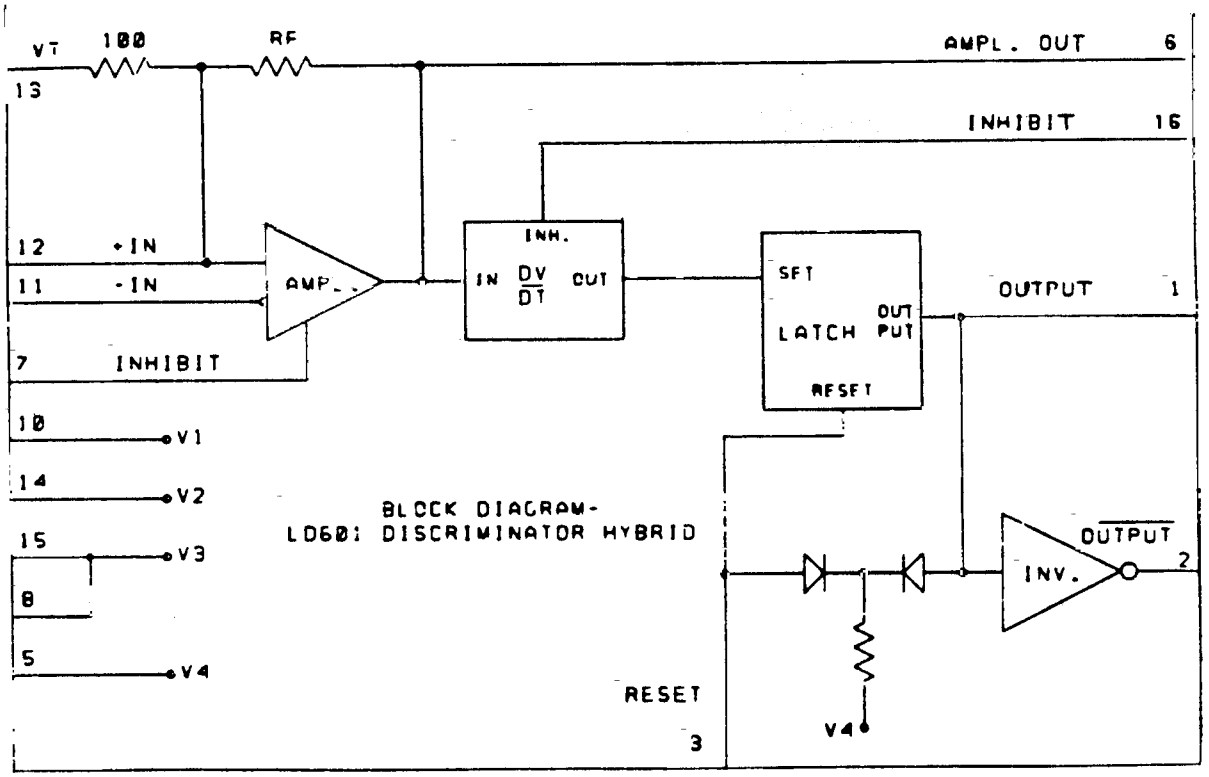

VT
100
RF
AMPL. OUT
6
13
INHIBIT
16
12
+IN
11
-IN
AMP
INH.
IN
DV/DT
OUT
SET
LATCH
OUTPUT
RESET
OUTPUT
1
7
INHIBIT
10
V1
14
V2
15
V3
8
5
V4
BLOCK DIAGRAM-
LD601 DISCRIMINATOR HYBRID
INV.
OUTPUT
2
RESET
3
V4

Figure 2.2

SECTION 3

TEST AND CALIBRATION

For the 621 and 821

This Test and Calibration Section has been included to familiarize the service technician with the areas that should be checked when searching for sources of failures and after replacing components, especially front end hybrids (LD601's). The trouble-shooting section is by no means exhaustive, but it does provide insight into some of the problems that have occurred at LRS during the initial testing of the 821's. The technician should follow the "Trouble-Shooting Guide" for ease in determining the defective component. Replacement of critical components will require some recalibration.

3.1 Trouble-Shooting

Equipment Required:

1. Digital voltmeter.

2. Sampling scope; 50 Ω input impedance.

3. High impedance real time scope with bandwidth of 150 MHz or greater (Tektronix 454, 475, or equivalent).

4. Pulse generator or signal source capable of producing 10 nsec -50 mV pulse into 50 Ω .

Initial Setup:

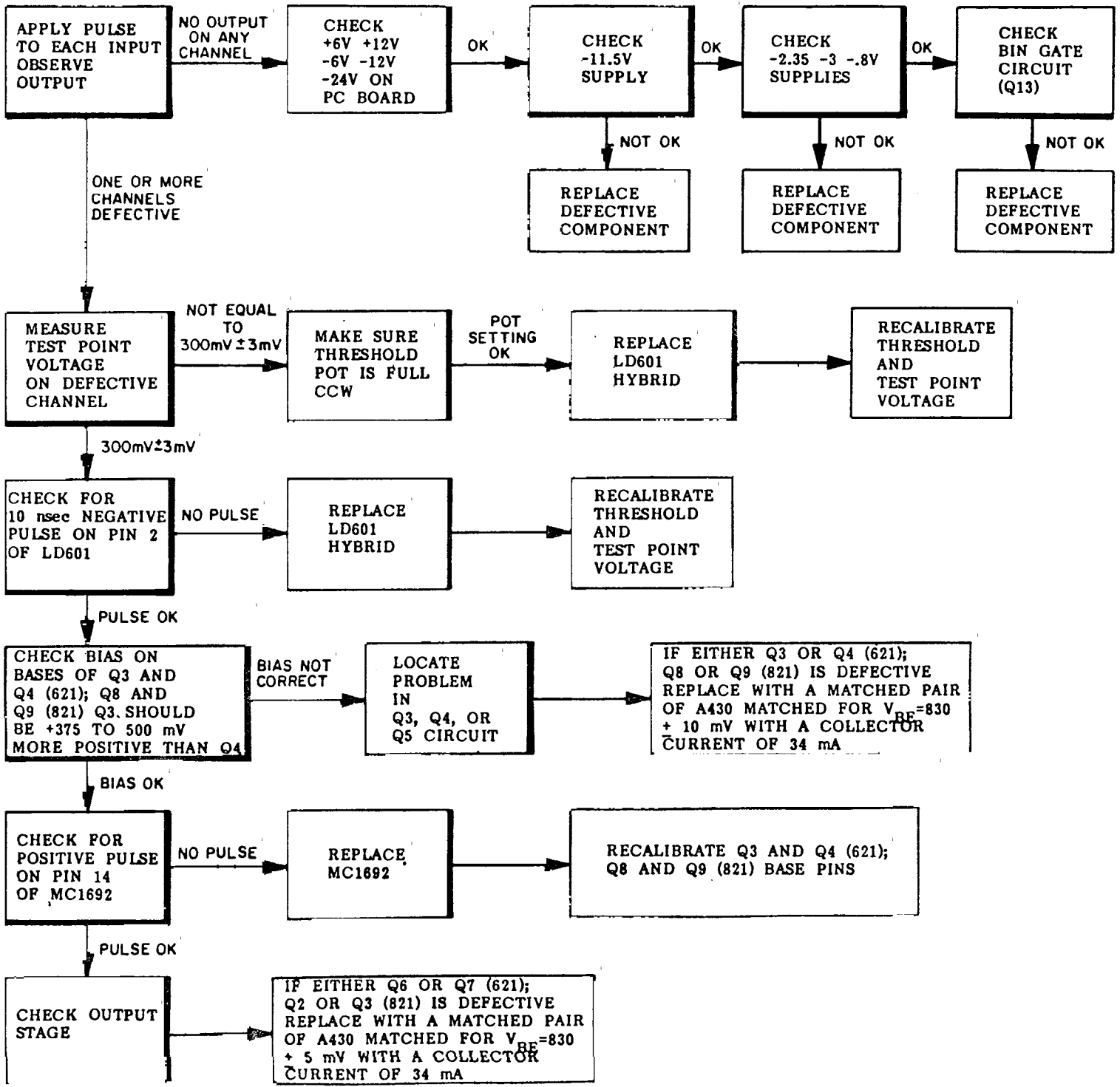
1. Use NIM power extender cable to power the 821 under test

2. Set all threshold and width pots to their full counterclockwise position (threshold equal to -30 mV and width equal to less than 5 nsec).

3. Apply a 10 nsec negative pulse (approximately equal to -50 mV) in turn to each input. Check output on sampling scope.

4. Follow the "Trouble-Shooting Guide", next page

TROUBLE-SHOOTING FOR 821 AND 621



3.2 821 Calibration

Required recalibration if LD601, MC1692, or timing stage components were replaced for the 821 series discriminators.

Replacement of LD601

If any LD601 was found to be defective and required replacement, the Threshold and Test Point voltage should be recalibrated.

Procedure:

1. Set front panel Threshold pot to minimum (counter-clockwise).

2. Measure Test Point voltage. If not equal to -300 ±5 mV, replace existing trim resistor T_1 (across 5 K Ω pot) with proper resistance to bring Test Point voltage into required range.

3. Check Threshold level with a 5 nsec wide pulse; if it is not -30 mV, replace existing trim resistor T_2 with proper resistance.

Replacement of MC1692 IC "C" - 621, IC "A" - 821.

If the MC1692 was found to be defective and required replacement, the base bias of Q3 and Q4 on the 621, and the base bias of Q8 and Q9 on the 821 should be recalibrated.

Procedure:

1. A) 621 - measure the base voltage of Q4 with respect to the base voltage of Q3. This voltage should be between +375 and +500 mV.

   B) 821 - measure the base volt of Q8 with respect to Q9 trim for 300 mV ± 25 mV.

2. Select proper trim resistor to obtain above voltage. (This trim resistor is connected from the base of Q5 on the 621 and Q10 on the 821 to the -11.5 V supply across the 8.2K or 7.5K resistor).

3. Observe output width. If less than 1 μsec with front panel width pot set to its full clockwise position, retrimming will be required. (See Calibration (9) Maximum Width).

4. Output Amplitude Adjustment: With one output terminated, the output amplitude of the bridged outputs should be greater than -750 mV. If less than 750 mV, the -3 V supply should be readjusted. Wide channel-to-channel variation of output amplitude indicates poorly matched MC1692 and/or output A430's. In order to reduce the channel-to-channel output amplitude variation without replacing any active devices, the emitter resistor of Q6 or Q7 (16 Ω) can be changed on the 621 and Q2 or Q3 on the 821. (To increase the output amplitude, the value of this resistor should be decreased).

Replacement of Q3 and Q4 (621) or Q8 and Q9 (821):

1. Observe output width. If less than 1 µsec with front panel width pot set to its full clockwise position, retrimming will be required. (See Section 3.4 Calibration (9) Maximum Width).

Calibration:

The following is a detailed step-by-step calibration procedure for the 621L (and 621AL) Discriminator. The sequence should be followed to avoid extraneous labor.

Important Notes:

a. When actual trim and calibration adjustments are performed, be sure the unit had at least 5 minutes of warmup time. (Calibration may be off if warmup time is too short.

b. If for any reason long periods of time between trimming occur, be sure to double-check periodically the bin voltages (Step 3). (Power supply voltage may change and calibration may be off when performed to the new changed voltage).

c. If at any check or calibration step problems occur, refer to the Trouble-Shooting Guide.

3.3 Procedure

1. Check (on board) the presence and verify the following correct voltages: -12.00 V, -6.00 V, and +6.00 V, and -24.00 V. These voltage points are clearly marked on the rear of the PC board.

2. -11.5 V regulator (new units only) - measure the voltage on the -11.5 V bus. Readjust pot (wiper connected to Pin 2 IC "G") if voltage is not -11.5 V ±50 mV.

3. -2.35 V regulator - measure voltage on the -2.35 V bus (or 2.2 V bus for 621AL). If voltage is not -2.35 V ±2% (or -2.2 V ± 2% for 621AL), retrimming will be necessary. The existing trim resistor across the 6.2 K Ω resistor (from Pin 3 of IC "D" to the -11.5 V supply), should be removed and replaced by one of proper value.

4 -0.8 V regulator - measure voltage on the -0.8 V bus. If voltage is not -0.8 ±2%, retrimming will be necessary. The existing trim resistor across the 909 Ω resistor (from Pin 3 or IC "F" to ground) should be removed and replaced by one of proper value.

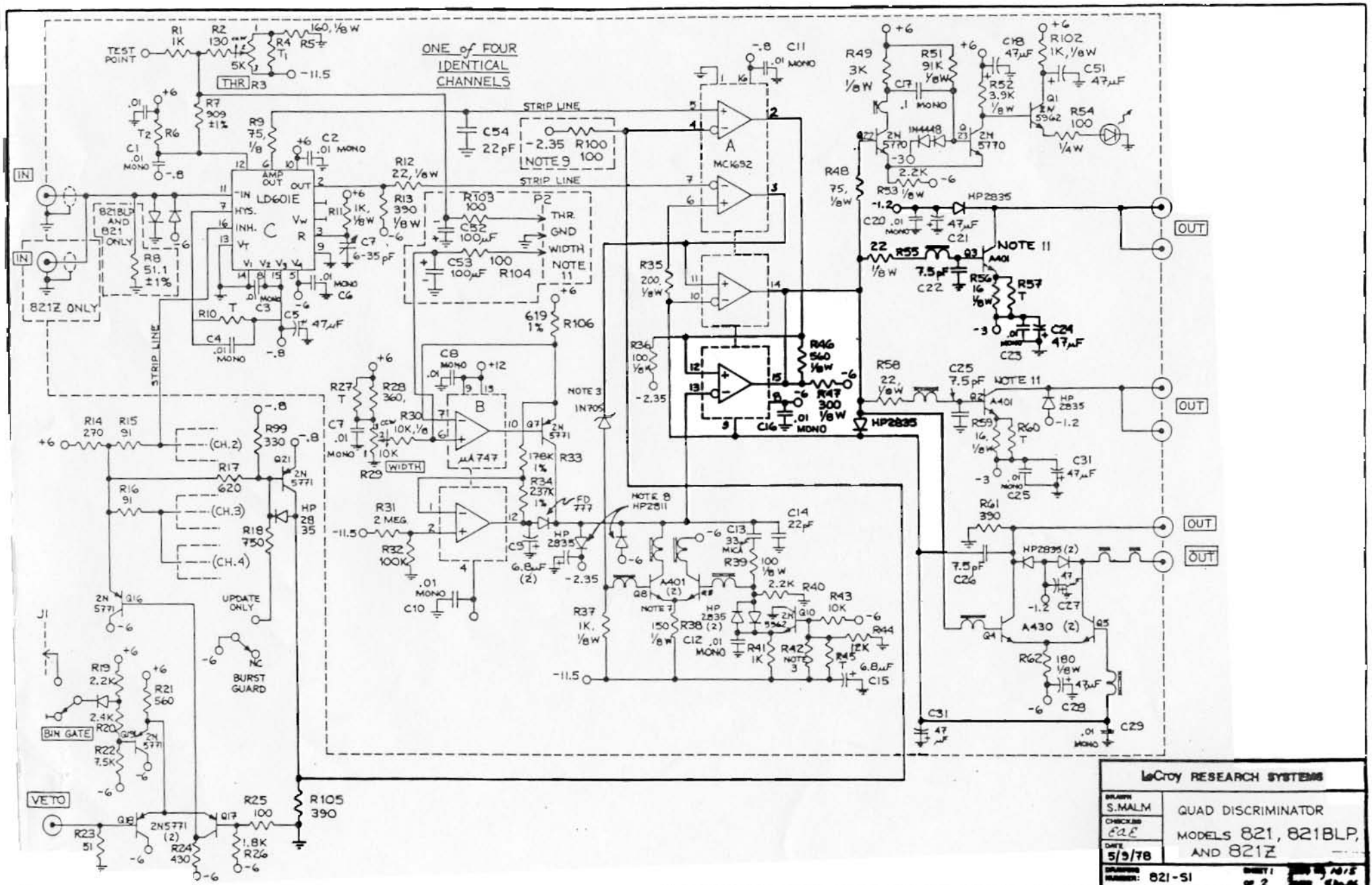
5. -3 V regulator - the -3 V regulator should only be adjusted if the output amplitudes of the bridged outputs are less than -750 mV when driving a total load impedance of 25 Ω . An adjustment pot (R 91) is provided to adjust the -3 V regulator.

6. Q3 and Q4 bias - measure the voltage on the base of Q4 with respect to Q3 base. If voltage is not between 270 mV and 330 mV, retrimming will be necessary. The existing trim resistor across the 8.2 K Ω or 7.5 K Ω resistor (from the base of Q5 to the -11.5 V supply) should be removed and replaced by one of proper value.

7. Test point voltage - turn front panel Threshold pot to its full counter-clockwise position (30 mV threshold. Measure voltage at front panel test point with respect to ground. If voltage is not equal to -300 ±5 mV (10 times threshold), retrimming will be required. The existing trim resistor T_1 (across the 5 K Ω pot) should be removed and replaced by one of proper value.

8. Threshold - make sure front panel Threshold pot is turned to its full counterclockwise position (-30 mV threshold). Apply a 5 nsec wide -30 mV pulse to the input. The output should be present approximately 50% of the time. If it does not trigger at all, or if it always triggers, remove the existing trim resistor T_2 and replace it with one of the proper value to insure 50% triggering level.

9. Maximum width - turn front width pot to its full clockwise position. Apply input with amplitude large enough to trigger 621. Check output width. If it is less than 1 μsec, retrimming will be required. The existing trim resistor across the 360 Ω resistor (from one end of the width pot to the +6 supply) should be removed and replaced by one of proper value.


ONE of FOUR IDENTICAL CHANNELS
TEST POINT
THR
STRIP LINE
IN
821BLP AND 821 ONLY
821Z ONLY
LD601E
MC1692
μA747
2N 5771
HP 2835
HP2835
A401
A430 (2)
2N 5770
2N 5362
IN4448
HP 2811
FD 777
IN705
(CH.2)
(CH.3)
(CH.4)
UPDATE ONLY
BURST GUARD
BIN GATE
VETO
WIDTH
NOTE 3
NOTE 7
NOTE 8
NOTE 11
OUT
LeCroy RESEARCH SYSTEMS
S.MALM
5/9/78
QUAD DISCRIMINATOR
MODELS 821, 821BLP, AND 821Z
821-S1