

ORTEC

Model 467

Time to Pulse Height

Converter and SCA

Operating and Service Manual

This manual applies to instruments
"Rev. 02" (on rear panel)

ORTEC 467 TIME TO PULSE HEIGHT CONVERTER AND SCA

Manual Change Sheet

REV 467-03

Feb. 10, 1975

On schematic 467-0101-S1, make the following changes:

Change the value of R45 from 4.3K to 4.7K.

For transistor Q24, exchange the identification of emitter and collector. The emitter of this NPN transistor should be shown connected to C13 and its collector connected to C14.

CONTENTS

	Page
WARRANTY	v
PHOTOGRAPHS	vi
1. DESCRIPTION	1
1.1. Purpose and Features	1
1.2. Operation	1
1.3. Logic	1
2. SPECIFICATIONS	2
2.1. Performance	2
2.2. Controls	3
2.3. Inputs	3
2.4. Outputs	3
2.5. Electrical and Mechanical	4
3. INSTALLATION	4
3.1. General	4
3.2. Connection to Power	4
3.3. Connection into a System	4
3.4. Linear Output Signal Connections and Terminating Impedance	5
3.5. Logic Signal Connections	5
4. OPERATING INSTRUCTIONS	5
4.1. Time to Pulse Height Conversion	5
4.2. Single Channel Analysis	6
5. CIRCUIT DESCRIPTION	7
5.1. General	7
5.2. TPHC Circuit	7
5.3. Single Channel Analyzer Circuit	8
5.4. Auxiliary Logic	8
6. MAINTENANCE	9
6.1. Testing Performance	9
6.2. Corrective Maintenance	12
6.3. Troubleshooting	14
6.4. Typical DC Voltages	15
6.5. Modifications	15
6.6. Factory Repair	15
APPENDIX	16
Schematics and Block Diagram	
467-0201-S1	
467-0301-S1	
467-0101-B1	

ILLUSTRATIONS

Fig. 6.1. Test System for Checking Conversion	9
Fig. 6.2. Test System for Checking Converter Resolution	10
Fig. 6.3. Test System for Checking Count Rate	11
Fig. 6.4. Test System for Checking Differential Linearity	11
Fig. 6.5. Differential Linearity for the Indicated Ranges	11
Fig. 6.6. Test System for Checking External Strob ing Mode	12
Fig. 6.7. Using Internal Strobe with Stop After End of Conversion	13
Fig. 6.8. Using Internal Strobe with Stop Timed Normally	13
Fig. 6.9. Using External Strobe with Output Timed Normally	14
Fig. 6.10. Using External Strobe with Strobe Signal Arriving Before Conversion is Complete	14

STANDARD WARRANTY FOR ORTEC INSTRUMENTS

ORTEC warrants its instruments other than preamplifier FET input transistors, vacuum tubes, fuses, and batteries to be free from defects in workmanship and materials for a period of twelve months from date of shipment provided that the equipment has been used in a proper manner and not subjected to abuse. Repairs or replacement, at ORTEC option, will be made on in-warranty instruments, without charge, at the ORTEC factory. Shipping expense will be to the account of the customer except in cases of defects discovered upon initial operation. Warranties of vacuum tubes and semiconductors made by their manufacturers will be extended to ORTEC customers only to the extent of the manufacturers' liability to ORTEC. Specially selected vacuum tubes or semiconductors cannot be warranted. ORTEC reserves the right to modify the design of its products without incurring responsibility for modification of previously manufactured units. Since installation conditions are beyond the company's control, ORTEC does not assume any risks or liabilities associated with methods of installation or with installation results.

QUALITY CONTROL

Before being approved for shipment, each ORTEC instrument must pass a stringent set of quality control tests designed to expose any flaws in materials or workmanship. Permanent records of these tests are maintained for use in warranty repair and as a source of statistical information for design improvements.

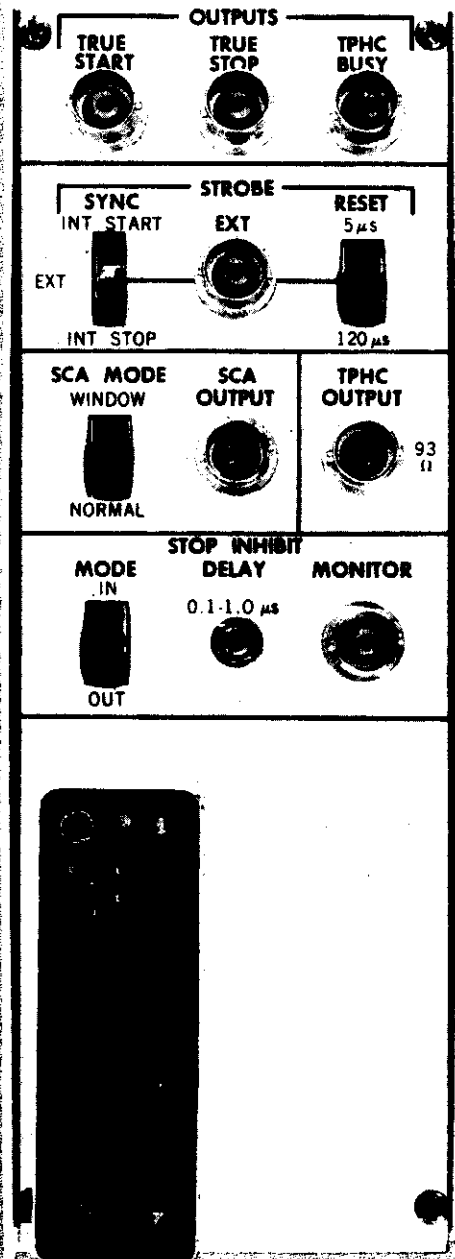
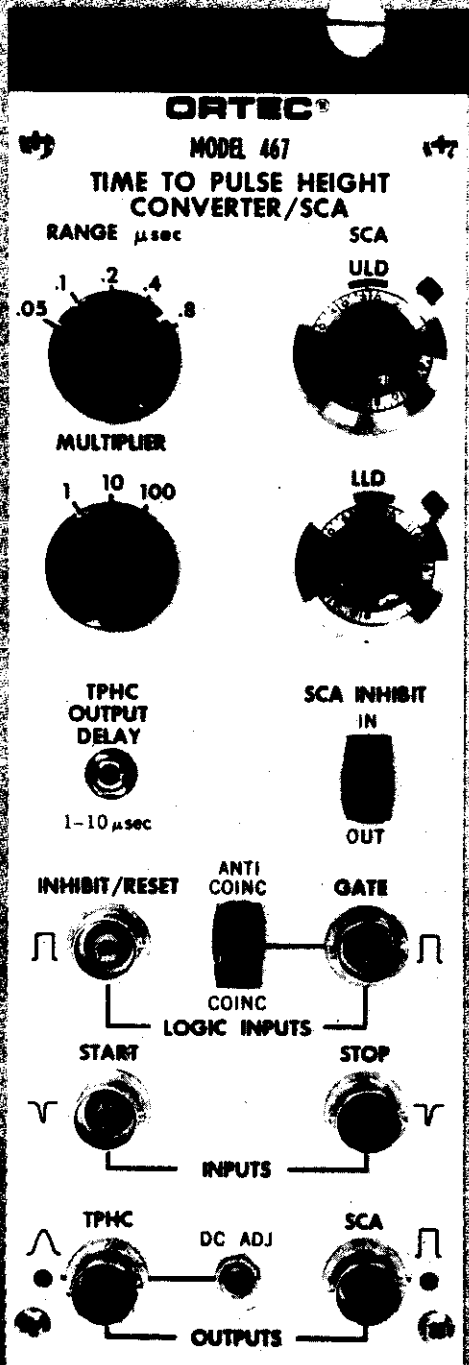
REPAIR SERVICE

If it becomes necessary to return this instrument for repair, it is essential that Customer Services be contacted in advance of its return so that a Return Authorization

Number can be assigned to the unit. Also, ORTEC must be informed, either in writing or by telephone [(615) 482-4411], of the nature of the fault of the instrument being returned and of the model, serial, and revision ("Rev" on rear panel) numbers. Failure to do so may cause unnecessary delays in getting the unit repaired. The ORTEC standard procedure requires that instruments returned for repair pass the same quality control tests that are used for new-production instruments. Instruments that are returned should be packed so that they will withstand normal transit handling and must be shipped **PREPAID** via Air Parcel Post or United Parcel Service to the nearest ORTEC repair center. The address label and the package should include the Return Authorization Number assigned. Instruments being returned that are damaged in transit due to inadequate packing will be repaired at the sender's expense, and it will be the sender's responsibility to make claim with the shipper. Instruments not in warranty will be repaired at the standard charge unless they have been grossly misused or mishandled, in which case the user will be notified prior to the repair being done. A quotation will be sent with the notification.

DAMAGE IN TRANSIT

Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify ORTEC of the circumstances so that assistance can be provided in making damage claims and in providing replacement equipment if necessary.



ORTEC 467

TIME TO PULSE HEIGHT CONVERTER AND SCA MANUAL

1. DESCRIPTION

1.1. PURPOSE AND FEATURES

The ORTEC 467 Time to Pulse Height Converter and Single Channel Analyzer (TPHC/SCA) measures the time interval between the leading edge of logic pulses furnished to its start and stop inputs and generates an analog output pulse that is proportional to the measured time through the TPHC output. The TPHC output pulses are appropriate for multichannel analysis to obtain timing spectra. They are also connected internally to the single channel analyzer to generate an SCA output logic pulse for each TPHC pulse with a peak amplitude within the adjusted single channel limits.

There are 15 full-scale time ranges that can be switch-selected with the 467, from 50 ns through 80 μ s. Each TPHC output pulse has a peak amplitude that is proportional to the ratio of the measured time interval to the selected full-scale interval, and the range of these pulses is 0 through +10 V.

The 467 is an extremely accurate and versatile instrument. It is composed of a very stable gated time to pulse height converter, a low-droop stretcher, a strobed TPHC output, and a single channel analyzer that can be operated in either a normal or window mode.

The integrated assembly, in a NIM-standard double-width module, combines excellent time resolution over a broad dynamic range with excellent temperature stability and linearity. It is dc-coupled throughout to prevent pileup and count-rate distortion.

1.2. OPERATION

Start-to-stop time conversion is accomplished only after a valid start has been identified and after a stop pulse has arrived within the selected time range. The start input is disabled during the busy interval to prohibit pileup; the stop input is disabled after the first accepted stop signal. Unwanted stop signals that occur immediately after a start input, such as those in linear accelerator applications, for example, can be rejected by a Stop Inhibit Mode switch and a circuit that is time-adjustable from 0.1 to 1.0 μ s. An inhibit/reset circuit also permits the operator to abort and cancel a measurement after a true start has been recognized. The input gate for the start circuit can be operated in either an anticoincidence or a coincidence mode.

Time ranges may be switch-selected for full-scale intervals from 50 ns to 80 μ s. Each time measurement is analog-stored in a low-loss stretcher amplifier until a linear gate is

opened by either an internal or an external strobe. The internal strobe can be obtained from either the start or the stop input pulse, and in either case occurs automatically at a selected delay following the reference. An external strobe can be used for a prompt output at the strobe time provided that a time measurement has been completed and reset has not occurred. A rear panel switch can select either 5 or 120 μ s after stop for an automatic reset if no strobe has been furnished. If reset occurs before a strobe, no TPHC output signal is available. There are two other sources for reset: one occurs if the start-to-stop time interval exceeds the range that is selected and the other occurs as a result of an input pulse through the Inhibit/Reset Logic Input connector on the front panel. The normal setting for the rear panel switch is 120 μ s; the 5- μ s setting should be used only if the stop-strobe mode is used and the delay is adjusted to minimum, or if the external-strobe mode is used and the strobe will be furnished within the selected interval.

The peak amplitude of the TPHC signal is sampled by the SCA at the time of a true-stop input. If the amplitude is within the adjusted acceptance range of the SCA, an SCA logic output is generated. The width of the SCA output is from the stop input until the subsequent reset. Since this output occurs before the TPHC signal is used to generate its analog output, the SCA output can be used to inhibit a TPHC output, unless the analog signal is within the SCA window, and to thus limit the range of a timing spectrum as it is stored in the multichannel analyzer.

The single channel analyzer has a lower level discriminator that can be adjusted through the full linear range of the TPHC signals from 0 through 10 V. The range for its upper-level discriminator is also 0 through 10 V, but the zero reference point for the ULD must be selected on the rear panel with the Window/Normal switch. When the switch is set at Window, the zero reference for the ULD is the adjusted setting of the LLD control. When the switch is set at Normal, the zero reference for the ULD is ground zero and is equal to the LLD zero point.

1.3. LOGIC

An input can be accepted through the Start Input connector on the front panel unless the 467 is busy processing a previous set of information or the response is inhibited by a gate input condition. The acceptance of a start input is essential in order to initiate a response in the 467. When a start input is accepted, a positive logic signal is available through the rear panel True Start Output connector and is continued until the leading edge of a subsequent reset. The

reset can be caused by a TPHC output, by the sensing of an overrange condition, or by an inhibit/reset signal through the front panel BNC. The true-start signal permits the internal circuits to start measuring a time interval and enables the stop input circuit.

The Stop Input BNC can accept an input signal after it has been enabled by the true-start condition. It may be enabled immediately at true start, or the rear panel Stop Inhibit Mode switch can be set at In and there will be a delay from true start before the stop signal can be accepted; the delay range is 0.1 through 1.0 μ s. When a stop input signal is accepted, this indicates that an interval has been measured and its analog equivalent is stored and available. A signal is furnished through the true-stop output that continues until the leading edge of a subsequent reset. If no stop input is accepted before an overrange condition is sensed or before an inhibit/reset input is furnished, the measurement will be aborted and no output signals for either SCA or TPHC will be generated.

At the true-stop time the SCA is enabled to sample the peak amplitude of the stored timing signal and to determine whether its peak amplitude is within the single-channel acceptance range. If the SCA responds, it generates an SCA output that goes high about 600 ns after the leading edge of the true stop and this signal continues until the trailing edge of the subsequent reset. If the SCA does not respond (because the amplitude is either less than the LLD or greater than the ULD), no SCA output is generated.

The front panel SCA Inhibit switch determines whether the SCA response is essential in order to generate a TPHC output. If the switch is set at In, a TPHC output is generated only if the SCA has responded. If the switch is set at Out, the generation of the TPHC output is independent of the SCA response.

The TPHC output must be strobed. The source of the strobe can be switch-selected from the true-start or true-stop signal or from an external signal. If true start is selected as the reference, the strobe occurs after a fixed delay that is selected by the Multiplier switch so that it will accommodate the maximum range time; if the switch is set at X1, the delay is 2 μ s; for the X10 setting, the delay is 10 μ s; and for the X100 setting, the delay is 100 μ s. If true stop is selected as the reference, the strobe occurs after a delay that has been adjusted with the front panel TPHC Output Delay control, 1 to 10 μ s after the leading edge of the true-stop signal. If the Strobe Sync switch is set at Ext, a signal must be furnished through the Strobe Ext BNC connector to strobe the output promptly.

The reset interval is 5 μ s and no output can be strobed after the leading edge of the reset pulse. There should be no interference if the Strobe Reset switch is set at 120 μ s unless external strobe is being used and the strobe input pulse does not arrive within the interval before reset. Reset can occur as the result of the completion of a read interval in which the TPHC signal is furnished as an output, or of an overrange indication where no significant peak amplitude is available, or of an inhibit/reset input that cancels the cycle at its leading edge and inhibits further response by the 467. The principal purpose for the automatic reset is to furnish this function if external strobe is being used and the input pulse is not furnished. If reset occurs for any reason before the TPHC output is completed, the TPHC output width is reduced by the reset.

A busy output starts at the leading edge of the true-start output and continues until the trailing edge of the subsequent reset. This can be used to control external equipment by indicating each interval during which no new start input can be accepted.

2. SPECIFICATIONS

2.1. PERFORMANCE

Time to Pulse Height Converter

Time Resolution <10 ps (10^{-11} s) FWHM on 50- and 100-ns ranges; <0.01% FWHM of full range for all other ranges.

Temperature Instability < ± 10 ps/ $^{\circ}$ C for 50-ns range; < $\pm 0.015\%$ / $^{\circ}$ C for higher ranges.

Differential Nonlinearity < $\pm 2\%$ from 10 ns through full range for 50-ns range; < $\pm 2\%$ from 5% range to full range for all higher ranges.

Integral Nonlinearity < $\pm 0.1\%$ from 10 ns through full range for 50-ns range; < $\pm 0.1\%$ from 5% range to full range for all higher ranges.

Single Channel Analyzer

Temperature Instability
ULD, < $\pm 0.01\%$ / $^{\circ}$ C. LLD, < $\pm 0.01\%$ / $^{\circ}$ C.

Nonlinearity Effectively determined by the 10-turn potentiometers. ULD, < $\pm 0.5\%$ over 10-V range. LLD, < $\pm 0.5\%$ over 10-V range.

2.2. CONTROLS

Range μsec Switch-selectable 15-range choices of .05, 0.1, 0.2, 0.4 or 0.8 μs multiplied by X1, X10, or X100; the X1 position can be internally modified to be X1000 to extend time range capability to 800 μs .

Multiplier Front panel 3-position selector switch; settings select multiple factors for the selected time ranges of X1, X10, and X100, resulting in 15 time ranges from 50 ns to 80 μs .

TPHC Output Delay Front panel 10-turn screwdriver potentiometer adjusts the output delay from the stop input to the internal stop strobe; range, $<1 \mu\text{s}$ to $>10 \mu\text{s}$.

Anti Coinc/Coinc Front panel slide switch selects either coincidence or anticoincidence logic for gating the start input circuit.

SCA ULD Front panel 10-turn potentiometer determines the window width or the upper-level discriminator setting; range, 0 to 10 V.

SCA LLD Front panel 10-turn potentiometer adjustable from 0 to 10 V.

SCA Inhibit Front panel slide switch.

In In this position the TPHC output pulse is available only if the output level falls within the SCA window.

Out In this position the switch has no effect on the TPHC output.

DC Adj 20-turn potentiometer to adjust the dc level over the range $\pm 0.5 \text{ V}$.

Strobe Sync Rear panel 3-position slide switch for selecting one of three modes:

Int Start In this position the information is strobed out $\sim 2 \mu\text{s}$ after the start pulse when the Multiplier switch is in the X1 position, $\sim 10 \mu\text{s}$ in the X10 position, and $\sim 100 \mu\text{s}$ in the X100 position.

Ext In this position a positive pulse fed into the Strobe Ext connector will strobe the information to the output if the strobe pulse has a magnitude of +3 V or larger.

Int Stop In this position the information is strobed out 1 to 10 μs (adjustable by the TPHC Output Delay control) after a true-stop pulse.

Strobe Reset Rear panel 2-position switch that allows the converter to be reset either 5 μs or 120 μs after a true-stop pulse if a strobe pulse has not been received.

SCA Mode Rear panel 2-position slide switch:

Normal Allows independent use of upper level discriminator and lower level discriminator.

Window ULD setting is added to LLD setting when switch is in this position.

Stop Inhibit Mode Rear panel 2-position slide switch:

In Rejects stop pulses that occur within 100 ns to within 1 μs (adjustable by the Stop Inhibit Delay control) after a true-start pulse.

Out In this position switch does not affect the operation of the instrument.

Stop Inhibit Delay A 20-turn trim potentiometer mounted on the rear panel allows the stop inhibit period to be adjusted from $\sim 100 \text{ ns}$ to $\sim 1 \mu\text{s}$ after a true-start pulse.

2.3. INPUTS

Start Input Front panel BNC connector.

Amplitude -250 mV minimum; protected to $\pm 100 \text{ V}$. $Z_{\text{in}} = 50 \Omega$, dc-coupled.

Rise Time No limit, but rise time should be as short as possible to provide maximum accuracy.

Pulse Width 3 ns at -250 mV ; maximum limit, $\sim 4 \mu\text{s}$.

Stop Input Specifications same as for the Start Input.

Gate Logic Input Front panel BNC connector. Logic 0, $< +2 \text{ V}$; logic 1, $> +2 \text{ V}$; input protected to $\pm 100 \text{ V}$. Gate signal must occur 10 ns before the start and must overlap the start input pulse. Impedance, $\sim 1 \text{ k}\Omega$, dc-coupled.

Inhibit/Reset Logic Input Front panel BNC connector. Amplitude of $> 4 \text{ V}$ resets circuit at any point in the cycle and inhibits start pulses for the duration of the pulse; input protected to +12 V.

Strobe Ext Rear panel BNC connector.

Amplitude $> +2 \text{ V}$; protected to $> \pm 25 \text{ V}$.

Rise Time No limit.

Pulse Width 10 ns minimum; $\sim 4 \mu\text{s}$ maximum.

Impedance 1 $\text{k}\Omega$ dc-coupled.

Control Outputs Prompt with strobe input.

2.4. OUTPUTS

TPHC Outputs Front and rear panel BNC connectors. 100% protected from short circuit and excessive duty cycle. **Unipolar** 0 to +10 V linear; $< 500 \text{ ns}$ rise time.

Width Internally adjustable from ~ 1.0 to 2.5 μs .

Output Timing Prompt with either internal or external strobe.

Impedance $< 1 \Omega$ on front panel and 93Ω on rear panel, dc-coupled.

Output dc Level Adjustable from 0 to $\pm 0.5 \text{ V}$ dc with front panel DC Adj screwdriver control.

SCA Outputs Front and rear panel BNC connectors. 100% protected from short circuit and excessive duty cycle.

Amplitude $\cong +4 \text{ V}$ on positive logic if TPHC pulse is in the LLD-ULD window and 0 V if TPHC is not in the window.

Output Timing Pulse begins $\sim 600 \text{ ns}$ after a valid stop pulse and continues until TPHC resets.

Impedance 10Ω , dc-coupled.

True Start Output Rear panel BNC connector provides a positive logic timing output to indicate the interval from an accepted start input signal until reset.

Rise Time <100 ns.

Output Width The interval from the start input until reset time, which can occur at strobe time, overrange, or 120 μ s after stop signal.

Impedance <10 Ω , dc-coupled.

True Stop Output Rear panel BNC connector provides a positive 4-V pulse to indicate valid stop and the interval from an accepted stop input signal until reset occurs.

Rise Time <100 ns.

Impedance \cong 10 Ω , dc-coupled.

Output Width The interval from the stop input until reset time.

TPHC Busy Output Via rear panel BNC connector to indicate the total time that the 467 is involved in a conversion; amplitude, +4 V; t_r , <100 ns; Z_o , 10 Ω , dc-coupled. Output width is equal to the interval from the start input to 5 μ s after reset.

Stop Inhibit Monitor Rear panel BNC connector provides a positive 3.5-V pulse to indicate the time period during which stop signals are inhibited.

Rise Time <100 ns.

Output Width Variable from 100 ns to >1.0 μ s with Stop Inhibit Delay trim potentiometer, beginning when a true-start pulse is received. Stop pulses are rejected until this pulse returns to the baseline if the Stop Inhibit Mode switch is in the In position.

Impedance \sim 10 Ω , dc-coupled.

2.5. ELECTRICAL AND MECHANICAL

Power Required

+24 V, 165 mA; -24 V, 120 mA;
+12 V, 320 mA; -12 V, 140 mA.

Dimensions NIM-standard double-width module (2.70 in. wide by 8.714 in. high) per TID-20893.

3. INSTALLATION

3.1. GENERAL

An ORTEC 401/402 Series Bin and Power Supply, or equal, in which the 467 will be installed, is intended for rack mounting. If vacuum tube equipment is operated in the same rack, there must be sufficient cool air circulating to prevent localized heating of the all-transistor circuits in the 467 and in the other modules in the Bin and Power Supply. Rack-mounted equipment subjected to the temperatures in vacuum tube equipment can exceed the maximum for which the transistorized circuits are designed unless this precaution is taken. The 467 should not be subjected to temperatures in excess of 120°F (50°C).

3.2. CONNECTION TO POWER

The 467 is designed per TID-20893 and accepts its operating power requirements through a mating power connector when it is installed in an ORTEC 401/402 Series Bin and Power Supply. As a safety precaution, always turn off the power for the Bin before inserting or removing any modules. If all the modules installed in the Bin are ORTEC 400 and/or 700 Series instruments, there will be no overload on any portion of the Power Supply. However, if any modules not designed by ORTEC are included in the Bin, this protection may not be effective; monitor the dc voltages at the test points on the control panel of the Bin after all modules have been installed and the power is turned on, in order to determine that none of the four power levels have been reduced by an overload.

3.3. CONNECTION INTO A SYSTEM

The 467 can accept both start and stop pulses from discriminators that furnish NIM-standard fast negative logic signals or from the timing output of a photomultiplier tube base. Typical ORTEC instruments that provide compatible signals are the 416A, 403A, 473, and 260 discriminators and the 265, 269, 270, and 271 Photomultiplier Tube Bases. The start and stop inputs will properly terminate 50 Ω cable, and this type is recommended to ensure proper termination of the signals.

No input or output connectors need be terminated when they are not in use.

In any experiment in which it is reasonable to assume that the count rates for start and stop will be equal or nearly so, use the signal furnished from the origin of events into the start input and the signal furnished from the response into the stop input. The 467 will then measure the time difference T from origin to response and furnish an output amplitude that is some fraction of the selected full-scale amplitude, proportional to the ratio of T to the selected full-scale time range.

In any experiment in which the two count rates differ noticeably, such as one in which fewer responses than event origins can be expected, use the lower count rate as the start input to the 467. This assures that the 467 dead time will be minimized, because it analyzes the time difference

only after a start signal is accepted. When the response is used as a start signal, furnish the signals from the origin of events through a delay line into the stop input, and adjust the delay to match the selected full-scale time of the 467. At each start input signal the 467 will analyze the time until its related origin signal is furnished to the stop input. The time measured is then delay time minus T , and produces a so-called inverted time spectrum. The purpose for this type of system connection is to reduce the number of conversions and the corresponding dead time during the experiment. For each signal accepted through the start input there must be a conversion, but for each signal through the stop input there need not be a conversion. For each start signal that is not followed by a stop signal within the selected time full range, the converter measures a time equal to the total range, even though no output pulse is generated.

3.4. LINEAR OUTPUT SIGNAL CONNECTIONS AND TERMINATING IMPEDANCE

The source impedance of the standard TPHC output, with the 0- to 10-V linear range, is about 1Ω through the connector on the front panel and 93Ω through the connector on the rear panel.

For the front panel circuit the interconnection to other modules does not usually require any special considerations, especially if the interconnecting cable is shorter than 4 ft in length. Paralleling several loads on a single output will still not reduce the 0- to 10-V signal span significantly unless the combined load is less than 100Ω .

The rear panel TPHC output circuit is designed for use of 93Ω cable to transfer the signals into a measuring circuit that has an input impedance of at least 1000Ω . With this series impedance-matched circuit connection, there will usually not be any interference with the signal. If oscillations should occur, it will be necessary to provide an additional shunt termination of 100Ω in parallel with the input circuit of the receiving instrument, but this will result in about a 50% loss of signal amplitude.

As with any analog instrument, oscillations may be observed occasionally when unterminated lengths of cable are used. Short cable lengths (up to 4 ft) need not be

terminated. When longer cable lengths are required for transfer of a linear signal, the cable should be terminated in a resistive load equal to the cable impedance to prevent reflections and oscillations in the cable. Oscillation suppression can be effected by either a series termination at the sending end of the cable or by a shunt termination at the receiving end. For convenience a BNC tee can usually accommodate both the cable and a mating terminator at the input of the receiving instrument. These units are available commercially, including BNC terminators with nominal values of 50, 100, and 1000Ω . ORTEC stocks a limited quantity of all but the 1000Ω terminators for your convenience, as listed below:

BNC Tee Connector	ORTEC C-29
50Ω Terminator	ORTEC C-28
100Ω Terminator	ORTEC C-27

When a shunt termination at the receiving end of the cable is impractical, consider series termination at the sending end. For a series termination the full signal amplitude span is available at the receiving end only if the input impedance is many times the characteristic impedance of the cable. For series termination install the correct resistance between the actual amplifier output, on the etched circuit board, and the output connector. Effectively, the terminating resistance is in series with the input impedance of the receiving instrument, and may result in some loss in signal amplitude. For example, if the series terminator is 93Ω and the driven load is 900Ω , the available signal span will be only about 90% of the maximum signal amplitude for each pulse. The termination of a 93Ω cable in a 93Ω load will cause a 50% loss for the signal.

3.5. LOGIC SIGNAL CONNECTIONS

The start and stop input circuits accept NIM-standard fast negative pulses. Each of these input circuits is designed with a 50Ω input impedance and is intended as the proper termination for the signals, furnished through 50Ω cables.

Impedance considerations for each of the remaining logic inputs and output for the 467 are noncritical and 93Ω cable is usually used. They can be terminated with 100Ω to prevent ringing if the signal is used to drive a high-impedance load.

4. OPERATING INSTRUCTIONS

4.1. TIME TO PULSE HEIGHT CONVERSION

There are seven front panel controls on the 467. Of these, four are directly associated with the conversion of a

start-to-stop interval into an analog equivalent TPHC output pulse. These controls are Range μ sec, Multiplier, TPHC Output Delay, and Anti Coinc/Coinc. If the SCA Inhibit switch is set at In, this also affects the generation of a TPHC output.

The Range μsec and Multiplier switches determine the full-scale limit for time conversion. Any of 15 combinations may be selected as follows:

Switch Settings		Full-Scale Time Limit
Range	Multiplier	
0.05	X1	50 ns
0.1	X1	100 ns
0.2	X1	200 ns
0.4	X1	400 ns
0.05	X10	500 ns
0.8	X1	800 ns
0.1	X10	1 μs
0.2	X10	2 μs
0.4	X10	4 μs
0.05	X100	5 μs
0.8	X10	8 μs
0.1	X100	10 μs
0.2	X100	20 μs
0.4	X100	40 μs
0.8	X100	80 μs

For example, with the Range switch set at 0.05 and the Multiplier switch at X100, the full-scale time range is 5 μs . Any stop input signal that occurs within 5 μs after a true-start signal will initiate the gating of an output pulse through both TPHC Output connectors. The output pulse will not be furnished through these connectors unless it is strobed. The strobe condition is selected by a rear panel switch and can be based on the time of the true-start signal, delayed by an amount of time greater than the selected full-scale time; or by the stop signal, delayed by an amount of time adjusted with the front panel TPHC Output Delay control, or by an external strobe input signal. When the output does occur, its peak amplitude will be proportional to the ratio of the measured start-to-stop interval to the selected full-scale time, in a 0- to 10-V range.

Internal logic eliminates any pulse ambiguity. No output pulse is furnished unless a stop signal is accepted within the selected full-range time. A stop signal is not effective unless it is preceded by a true-start signal. For further logical control either a coincidence or anticoincidence mode can be selected for gating control of the start input circuit. To eliminate gating for the start input, set the Gate switch at Anti Coinc and leave the gate input circuit without any connection. When the same switch setting is used and an input signal is furnished, start signals are not accepted when the gate signal is +2 V or more.

For coincidence gating of the start input circuit set the Gate switch at Coinc and furnish a signal of +2 V or more

through the Gate Logic Input connector when start signals are to be accepted.

If a signal is furnished through the Inhibit/Reset connector on the front panel, any time measurement that may be in process will be aborted and no new measurement can begin until the inhibit/reset signal is removed. To be effective, the inhibit/reset signal must precede an output strobe time.

The rear panel Strobe Sync switch selects the source for the strobe signal for the TPHC output. When the switch is set at Int Start, the strobe is generated by a delayed true-start signal and the delay is fixed at a time that is longer than the selected full-range time. When the switch is set at Int Stop, the strobe is generated by a delayed true-stop signal and the delay is adjusted by the TPHC Output Delay control on the front panel within the range of 1 to 10 μs . When the switch is set at Ext, an input pulse must be furnished through the adjacent BNC connector and the TPHC output signal is strobed promptly at the external signal time.

The timing of an external strobe input signal must be within the switch-selected interval, 5 or 120 μs , after the true-stop pulse for the measurement. If the strobe is furnished prior to stop, the signal is not accepted. In the case of a strobe pulse failing to arrive within the selected interval after stop, the 467 will have been automatically reset internally; so there is no available output and the strobe signal is ignored. If the 467 is to be used as a stretcher or buffer storage of the analog output for more than 120 μs , a simple modification can increase this time limit; see Section 6.4.

By the addition of four jumpers in the 467 circuit the X1 setting of the Multiplier switch can be replaced by a X1000 setting. If these jumpers are added, as described in Section 6.4, the minimum time range setting is 500 ns and the maximum range is 800 μs .

In any application of the 467 in which stop signals occur immediately following a true start but are to be ignored, in favor of time measurements, to stop signals that occur later, the rear panel Stop Inhibit circuit can be used. With the Mode switch set at In, the adjacent screwdriver control can be adjusted for a delay of 0.1 to 1.0 μs and all stop signals are ignored that occur within the adjusted delay time following a true-start signal. The adjusted time delay can be monitored through the rear panel Monitor connector to measure the duration of the delay signal that occurs at each true-start-input time.

4.2. SINGLE CHANNEL ANALYSIS

The single channel analyzer portion of the 467 measures the peak amplitude of each analog TPHC pulse as soon as it is formed. If the peak amplitude is within the lower and upper limits that are set with the LLD and ULD controls on the front panel, an SCA output signal is generated after a 400-ns propagation time. The signal can be used to control

the subsequent generation of a TPHC output if the front panel SCA Inhibit switch is set at In. Under this condition the SCA must generate an output in order to permit the generation of a TPHC output at its strobe time, and this can limit the range of time signals that are furnished to a multichannel analyzer to generate a spectrum. An independent SCA output signal is furnished through both the front and rear panel SCA Output BNC connectors for any external applications that may be desired.

A rear panel switch selects either Window or Normal mode for the SCA. In the Window mode the acceptance range is from the LLD setting to the sum of the LLD plus ULD settings. In the Normal mode the LLD control and the ULD control each operates independently and the acceptance range is from the LLD setting to the ULD setting; the ULD setting must always be greater than the LLD setting to generate an SCA output.

5. CIRCUIT DESCRIPTION

5.1. GENERAL

The circuits for the 467 are shown in schematics 467-0201-S1 and 467-0301-S1 and in block diagram 467-0101-B1. All these drawings are included at the back of the manual.

The components that are included in schematic 467-0201-S1 all have reference designation numbers that are less than 300, and those on the 467-0301-S1 drawing have reference designations in the 300 series. The division of circuits between the two boards on which the components are mounted is indicated in the block diagram.

The nomenclature used to identify the integrated circuit packages referred to in this manual is defined below for the example

IC2(10),

where

IC = integrated circuit,
2 = component number,
(10) = pin number.

Any portion of an IC package can be designated by its output pin number.

5.2. TPHC CIRCUIT

The start input circuit contains D1, Q1, and resistors R1 through R4, which form a voltage limiter to protect the base input circuit of Q2. A negative input signal of 250 mV or more, limited at 700 mV, is amplified by Q2 and Q3 and causes tunnel diode D3 to switch from its low state (−50 mV) to its high state (−450 mV). The tunnel diode remains in the high state until reset is furnished from Q51 to trigger D3 back to its low state.

While tunnel diode D3 is in its high state, the current that normally flows through Q5 is switched to Q4 to perform

two functions: It drives the true-start-output circuit (Q5, Q6, IC1, and Q56) for an external timing signal keyed to an accepted and valid start input, and it switches the current that normally flows through Q12 to Q11. While current flows through Q11, Q10 is held at cutoff and a constant current from Q46 charges the selected timing capacitor linearly; the timing capacitor (C6 and possibly C32 or C33) is selected by the Range Multiplier switch, S2. If the X1 selection is changed to a X1000 selection, C29 and C31 can also be selected as a part of the timing capacitor. The voltage to which the selected timing capacitor can be charged is limited to 3.6 V by Q7.

The voltage developed across the timing capacitor is applied to the input of a stretcher amplifier that includes Q41 through Q44. This amplifier has a gain of unity and its output voltage is obtained from the gate of Q44B.

If a stop signal is not furnished within the selected time range, Schmitt trigger Q53 and Q54 fires at a timing capacitor level of about 3 V from a 10-V signal on Q37E. This identifies an overrange condition. The output triggers the reset circuit, which includes Q48, Q49, Q51, and Q52. The reset circuit causes tunnel diode D3 to return to its low state without generating a TPHC output pulse.

If an external stop signal is received prior to the overrange identification, Q46 is switched off and the timing capacitor receives no further charge. The charge that accumulated on the timing capacitor between the start and stop input pulses determines the capacitor's voltage and therefore the output voltage.

In the stop input circuit, diode D9 and its associated resistors form an amplitude-limiting circuit similar to the start input circuit. A valid start pulse enables the stop circuit through Q17. The stop pulse is amplified by Q18 and Q19. If the stop pulse arrives while D11 is enabled, this diode is driven to its high state to switch the current from Q21 through Q20. When Q20 conducts, Q45 is driven into conduction and the constant current through Q46 is cut off. The selected timing capacity is not charged any further

and has no discharge path; so it holds the voltage to which it has been charged.

Switching pair Q21 and Q20 also performs two additional functions. If the internal stop strobe is used, a trigger is furnished to the read timer, Q24 and Q27 through Q29. This circuit generates a delay of 1 to 10 μs and then operates gate circuit Q35 and Q36. Switching pair Q21 and Q20 also furnishes a strobe to the SCA circuit through Q22 and Q23.

Read timer Q27 and Q28 performs two functions: It opens linear gate Q36 and triggers reset through Q52. Timing for Q27 and Q28 is adjusted by R86, and the gate width is normally set at about 2 μs . The linear gate is opened during this period and reset occurs at the end of the period. At reset tunnel diode D3 is switched to its low state and cannot be switched back to high again for about 5 μs ; this feature prevents pileup. When D3 is reset, it forces D11 to its low state through Q4, Q12, and Q17.

Linear gate Q36 conducts a current with an amplitude proportional to the charge stored in the timing capacity, and the charge is proportional to the time between start and stop input signals. The gating pulse from Q33 causes Q35 to conduct to, in turn, cut off Q36. The current that was flowing through Q36 is rerouted into OA-1 during the period of the gating pulse. OA-1 is a high-gain operational amplifier that has its gain regulated to -1 for positive input signals and to 0 for negative input signals. The output from OA-1 drives another operational amplifier, OA-2 on the Q301 board, that has a gain of -1 and generates the positive TPHC output signals.

The TPHC information may be strobed out in three different ways: The strobe pulse can be referenced internally to the stop signal, internally to the start signal, or externally. In each case a one-shot multivibrator is triggered to generate the gate pulse. In the stop-strobe mode R73 and R74 with C13 determine the time from the stop pulse until Q24 conducts and the one-shot circuit is triggered. The delay is adjusted from 1 to 10 μs by R73 on the front panel. In the start-strobe mode the true-start signal from IC1(12) triggers a one-shot multivibrator that includes IC3(6), C55, R189, and R191. The period of this one-shot circuit is variable internally and determines the delay between the start pulse and the strobe pulse. The start-strobe signal drives the gate one-shot that includes IC4, Q59, and Q26. In the external strobe mode a positive pulse through the Strobe Ext input connector drives the gate one-shot through Q26.

Logic signals corresponding to true start, true stop, and TPHC busy are generated by the circuits that include IC1, IC2, Q56, Q57, and Q58. If for any reason a strobe signal is not received, the TPHC circuits are reset after 5 or 120 μs , selected by S5, through Q33 and the overrange circuit, by R103, C19, and C22. For this condition there is no TPHC output signal.

5.3. SINGLE CHANNEL ANALYZER CIRCUIT

There are two discriminator circuits in the SCA. The lower-level discriminator uses IC304, IC305, and IC306. The upper-level discriminator uses IC301, IC302, and IC303. Both channels obtain their reference voltage from D301 and the maximum voltage at TP1 and TP2 is adjusted to -5 V with R301 and R316. The TPHC amplitude from Q37 is divided by R333 and R334, and 50% of the TPHC level is compared in IC303 and IC306 to their reference levels, determined by the settings of R302 and R317 on the front panel, and to the setting of rear panel SCA Mode switch S6.

A signal is obtained from the stop circuit through Q23 to trigger a one-shot that includes IC308, R336, and C352. The output of the one-shot is used to strobe the lower and upper comparators. If the TPHC signal exceeds the lower reference but does not exceed the upper reference, a positive logic output of 4 V is obtained at Q305 through IC307, IC308, and IC309. If the TPHC signal is less than the lower reference or greater than the upper reference, the gate circuits in IC309 are not activated and there is no SCA output.

When switch S6 is set at Window, the lower-level and upper-level reference voltages are summed at the input of IC302. For this condition the window is the difference between the lower-level adjustment and the sum of both the lower- and upper-level adjustments within the linear range limits of the SCA.

5.4. AUXILIARY LOGIC

The 467 includes an input gate circuit, a stop inhibit circuit, an inhibit-and-reset circuit, and an SCA inhibit circuit. The function of each of these logic circuits is defined in Sections 4.1 and 4.2.

The input gate circuit consists of D7, Q13, Q15, and Q16. When Gate switch S8 is set at Anti Coinc, Q13 is saturated and a negative start input pulse can trigger tunnel diode D3. If a positive gate input signal is furnished through CN2, Q15 conducts and clamps D3 to prevent it from responding. With the Gate switch set at Coinc Q13 clamps D3 and prevents it from responding except when a positive input is furnished through CN2.

Stop signals can be inhibited from triggering D11 through a controlled interval following each true start. This function uses IC3 and IC4. The start signal triggers a one-shot multivibrator that includes IC3, C56, R196, and R197. The output of IC4 is normally high and is driven low during the period of the one-shot. If Stop Inhibit switch S7 is set at In, the positive signal from IC4 clamps Q17 through Q16 to prevent response in D11. After IC4 returns to low, Q17 conducts and enables D11 to accept a stop input pulse. A positive monitor output is produced through Q60 during the inhibit interval.

A signal through the Inhibit/Reset connector on the front panel activates the overrange circuit, Q53 and Q54, and resets the TPHC circuit at any time during a cycle. A positive input through CN6 drives the base of Q53 negative through Q55. The reset circuit forces D3 to its low state and clamps it until the external signal drops below approximately 3.5 V. During this period a start signal will not be accepted.

If SCA Inhibit switch S3 is set at In, an SCA output signal is necessary in order to enable a strobed TPHC output. With the switch in this position Q30 is normally saturated and blocks the gating signal at Q31. A positive SCA output signal ("SCA OK") cuts off Q30 and allows the gating signal to propagate through Q31 to the gating circuit.

6. MAINTENANCE

6.1. TESTING PERFORMANCE

The following test procedures are furnished as a guide during installation and checkout of the 467 TPHC/SCA.

Test Equipment The following test equipment is recommended. Each test procedure refers to this list by the unit identification number for the required item(s) of test equipment. An equivalent unit may be substituted for any item in the list, providing that it furnishes the function required for each specific application.

1. Hewlett-Packard 222A Pulse Generator
2. ORTEC 436 100 MHz Discriminator
3. ORTEC 416A Gate and Delay Generator
4. ORTEC 425 Nanosecond Delay
5. Photomultiplier tube with scintillator and radiation source
6. ORTEC 403A Time Pickoff Control
7. ORTEC 449 Log/Lin Ratemeter
8. Tektronix Type 585 Oscilloscope
9. ORTEC 6240 Multichannel Analyzer
10. ORTEC 414A Fast Coincidence
11. ORTEC 444 Gated Biased Amplifier

Preliminary Procedures Take the following preliminary steps when the 467 is installed:

1. Check the module visually for possible damage.
2. With the power turned off, install the 467 into a NIM-standard Bin and Power Supply such as one of the ORTEC 401/402 Series.

3. Check the installation for proper mechanical alignment.
4. Switch on ac power and check the dc power voltage levels at test points on the 402 Power Supply control panel.

Basic Switch Settings Set the 467 controls as follows:

Range	0.05 μ s
Multiplier	1
ULD	10 (fully clockwise)
LLD	0 (fully counterclockwise)
SCA Inhibit	Out
Logic Input	Anti Coinc
Strobe Sync	Int Stop
SCA Mode	Normal
Strobe Reset	120 μ s
Stop Inhibit Mode	Out

Conversion Tests Use the typical test setup shown in Fig. 6.1 and supply a start and stop pair of input signals with known time difference into the 467. Observe the TPHC output. Then use the following procedures:

1. Adjust the delay for the stop input to 25 or 30 ns more than the basic 13 ns required for a minimum response.
2. Check to see that the full-scale time range is 0.05 μ s X 1, or 50 ns.

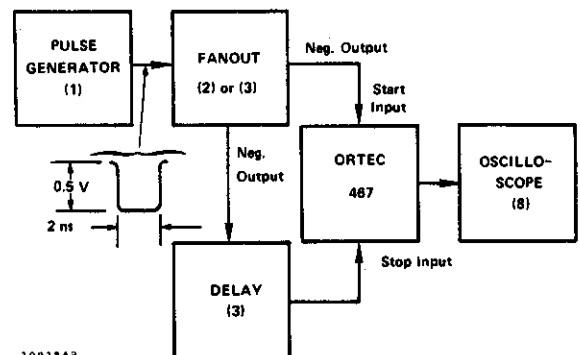


Fig. 6.1. Test System for Checking Conversion.

3. Measure the signal through the TPHC Output connector. It should be about 6 V for a 30-ns delay or 5 V for a 25-ns delay.

4. Turn the Range μsec switch through its .1, .2, .4, and .8 settings and observe the pulse amplitude at each setting; each successive switch position should decrease the pulse amplitude to about 1/2 of the amplitude for the previous setting.

5. Return the Range μsec switch to .05 and set the Multiplier switch at 10. The output amplitude should be reduced to about 1/10 of the reading for step 3.

Resolution Tests See Fig. 6.2 for the typical test setup used for resolution checks. The start and stop pulses used for this test must have fast rise time and be jitter-free. The minimum delay recommended for the stop pulses is 15 ns. The resolution of any scale can be measured with this setup, and the main consideration is that each stop signal delay be within the linear region of the selected time range. The testing procedure consists of the following:

1. Adjust the delay for the stop input to a basic setting of 30% to 80% of the selected time range.

2. Operate the system and obtain a timing spectrum. Normalize the output amplitude full range for the normally digitized full range of the ADC in the analyzer.

3. After you have accumulated an adequate spectrum to assure statistical accuracy of photopeak measurements (~ 1000 counts in the peak channel), identify the peak channel number and measure the FWHM channel number limits. Log for reference.

4. Increase the delay for the stop signal by a fixed and known amount. This may be done by switching in a fixed delay line cable (ORTEC 425) or by careful adjustment of the Delay unit controls. The total delay for the stop signal must still be less than 100% of the selected time full range.

5. Accumulate a spectrum for this measurement of increased time intervals.

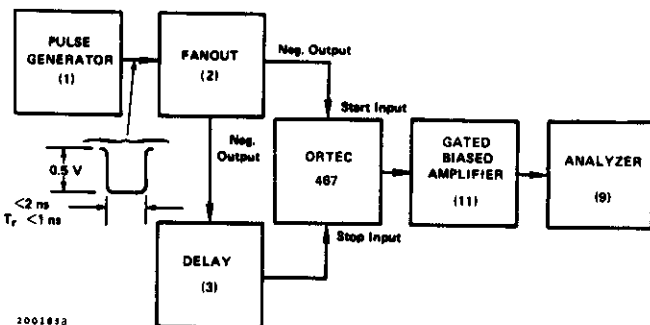


Fig. 6.2. Test System for Checking Converter Resolution.

6. Observe the relocated photopeak in the timing spectrum and record its peak channel number and its FWHM channel number limits.

7. Subtract the peak channel number in step 3 from the peak channel number in step 6. This is the number of channels that represents the time variation injected at step 4.

8. Using the formula listed below, calculate time resolution effective for the established system calibration:

$$\Delta t \text{ per channel} = \text{stop delay increase} \div \text{channel shift.}$$

9. With the equation listed below, calculate the converter resolution, using the FWHM channel width from either step 3 or step 7. These widths should be the same at either peak location.

$$\text{Time resolution (FWHM)} = \text{FWHM channel width} \times \Delta t \text{ per channel.}$$

This resolution is affected adversely by any jitter that may be present in the discriminator and by the resolution of the amplifier. Allowances should be made for these contributions.

Count Rate Tests In many applications it is important for a time to pulse height converter to handle high count rates, both external and internal. Since the start input is gated internally and the conversion circuits are all direct-coupled, the limit for its external count rate capability is determined solely by the input pulse width, and there are no pileup effects. The limit on the internal count rate is imposed by the conversion and reset process, where the start input is disabled through a converter busy interval following each accepted start signal. A converter busy interval is the measured time plus approximately $7 \mu\text{s}$ for start-stop intervals within the selected time range or is the selected time range plus $4 \mu\text{s}$ if no stop signal is furnished within the time range.

The following test, based on the system connection shown in Fig. 6.3, permits accumulation of a basic timing spectrum for the start-stop input pulses at 60 Hz. As the external count rate for start only is increased by regulating the random pulse generator, the internal pulse rate in the 467 is increased, and a ratemeter will monitor the resulting rate at which the internal capability is impaired.

1. The photomultiplier may be used as a random pulse generator, triggered by a radiation source. Use an initial sensitivity setting above the energy level for a zero output pulse rate.

2. Adjust the delay for the stop input to about $0.4 \mu\text{s}$.

3. Select the $0.5\text{-}\mu\text{s}$ time range with the 467.

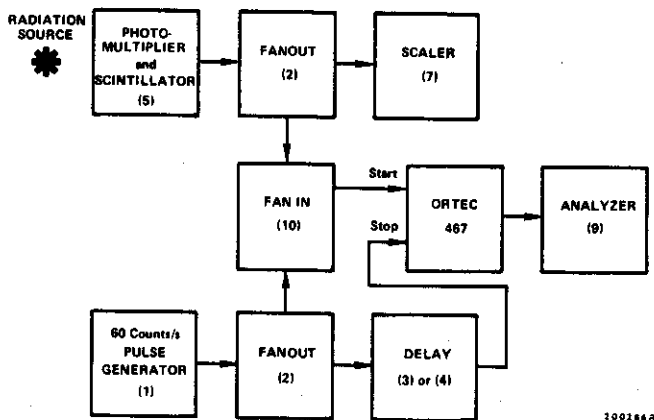


Fig. 6.3. Test System for Checking Count Rate.

4. Adjust the system for a timing spectrum, accumulated for the 60-Hz input pulses.
5. Decrease the threshold of the discriminator (2) to generate random start signals with no corresponding stop signals. Monitor the random rate with the ratemeter.
6. Observe the timing spectrum as the random input rate is gradually increased. Watch for interference in the accumulated spectrum.

Differential Linearity Measurements A system for testing differential linearity of the 467 is shown in the block diagram in Fig. 6.4. In this system the random pulse generator is used as the source for start signals, and a pulse generator with a fixed rate is used for stop signals. The measurable time interval between a start and stop is a random value, with equal probability that it will be any time difference up to the periods between the regular stop signals. For an infinite number of TPHC outputs the count levels for each channel of the analyzer should be equal. After the test has been run long enough to assure statistical accuracy (e.g., >25,000 counts/channel), the spectrum should be similar to those illustrated in Fig. 6.5. Any deviation from a straight line represents a differential

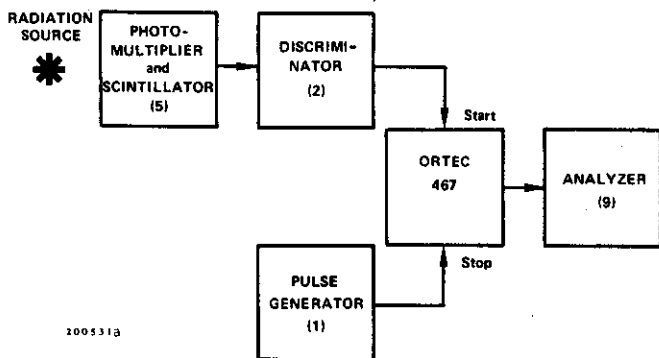
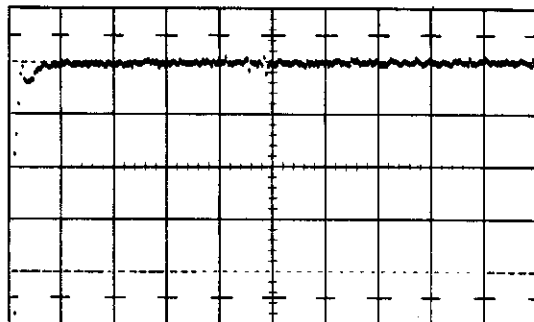


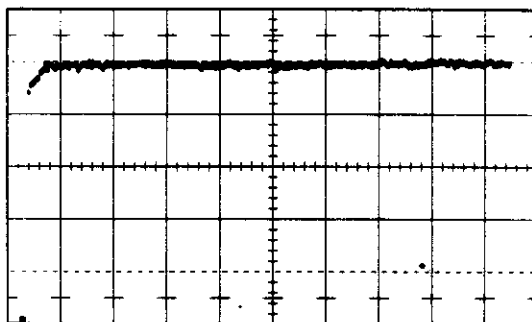
Fig. 6.4. Test System for Checking Differential Linearity.

nonlinearity, and the percent of deviation is the difference between this count level and the average divided by the average count level.

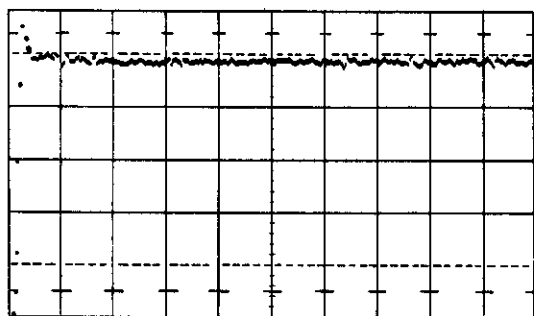
1. Select the 467 time range to be tested.
2. Calculate the maximum stop pulse repetition rate for the selected time range. This should be slightly lower than the reciprocal of the time range. For example, for the 1- μ s time range the reciprocal is 1×10^6 , and a pulse generator



Range = .1 } 100 ns
Multiplier = X1
(Vert): Full Scale 5×10^4 counts
(Horiz): Full Scale = 105% range



Range = .1 } 1 μ s
Multiplier = X10
(Vert): Full Scale 5×10^4 counts
(Horiz): Full Scale = 105% range



Range = .1 } 10 μ s
Multiplier = X100
(Vert): Full Scale 5×10^4 counts
(Horiz): Full Scale = 105% range

Fig. 6.5. Differential Linearity for the Indicated Ranges.

rate of 4 to 5 times 10^5 should be satisfactory. A lower rate increases the time required to run the test, while a faster rate will reduce the upper channel response because of analyzer dead time.

3. Operate the system and monitor the dead-time meter on the analyzer. Regulate the random start rate to cause the analyzer dead time to be approximately 10%.

4. Clear the analyzer to zero and operate the system until the average count level stored in each channel is sufficient to ensure statistical accuracy.

5. Compare any nonlinearity indications to the specifications listed in Section 2. Some nonlinearity can be expected in channels in the lower 5% of the analyzer range as shown in Fig. 6.5 because of the stop pulse width and the TPHC gating time.

Checking External Strobing Mode The system for checking the external strobing mode is shown in Fig. 6.6. This system can be used to verify the principles of operation of the 467.

1. Set the delay for the stop signal at about $0.4 \mu\text{s}$.
2. Set the 467 time range for $0.5 \mu\text{s}$.
3. Use the internal strobe mode for the 467. Adjust the oscilloscope sweep as required to identify the TPHC output pulses.
4. Adjust the delay for the strobe signal greater than $0.5 \mu\text{s}$ to ensure that it will occur later than the full time range.
5. Switch the 467 to its external strobe mode and observe the TPHC output pulse. It should be identical to the pulse observed in step 3 except for the time at which it occurs.
6. Vary the stop delay setting and observe the effect on the TPHC output pulse. It should occur at a constant time but vary in amplitude. If the stop delay is increased beyond $0.5 \mu\text{s}$, there will be no output pulse.

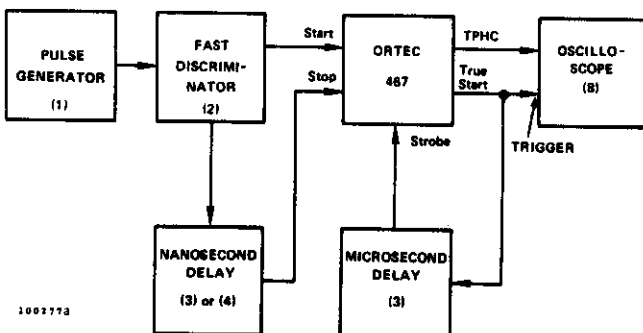


Fig. 6.6. Test System for Checking External Strobing Mode.

7. Vary the strobe delay and observe that there is no change in the TPHC output amplitude but that the output delay follows the strobe delay. Normally when the 467 is in external strobe mode, it is internally reset at either 5 or $120 \mu\text{s}$, selected with the rear panel Strobe Sync switch.

Testing the Single Channel Analyzer The single channel analyzer can be tested by the following procedure:

1. Set the ULD control fully clockwise at 10.00 dial divisions and the LLD control fully counterclockwise at 0.
2. Set the SCA Mode switch at Normal.
3. Use the circuit shown in Fig. 6.1. Select a convenient time range and adjust the stop delay to obtain an output of about 5 V through the TPHC Output connector. Note that an SCA output is present.
4. Increase the LLD control setting and note that the SCA output disappears as the LLD dial moves through about 5.00 dial divisions (considering the accuracy of the TPHC output amplitude adjustment). Decrease the LLD setting to about 4.00 so that the SCA output reappears.
5. Decrease the ULD setting and note that the SCA output pulse disappears as the dial moves down through about 5.00.
6. Move the SCA Inhibit switch setting to In and note that the TPHC output pulse is present only when the SCA output pulse is also present. Return the SCA Inhibit switch to Out.
7. Change the SCA Mode switch from Normal to Window. Set the LLD dial at 4.0 and the ULD dial at 2.0. Change the stop delay to change the TPHC output pulse amplitude from 3 V to 7 V. Note that the SCA output pulse is present only when the TPHC output amplitude is within the range of 4 to 6 V.

6.2. CORRECTIVE MAINTENANCE

Clean the surfaces of the printed circuits, the connectors, and all chassis parts periodically to prevent accumulated dust from forming leakage paths between the circuit components. The 467 should require maintenance only rarely, as indicated by a malfunctioning in its performance under known conditions.

If the instrument is suspected of malfunctioning, use the performance tests of Section 6.1 above to aid verification. When incorrect operation is identified, disconnect the 467 from its position in the system and perform routine diagnostic tests with a pulse generator and oscilloscope. Use the timing diagrams in Figs. 6.7–6.10 to isolate the problem, and use schematic diagrams 467-0201-S1 and 467-0301-S1 at the end of this manual to localize the malfunctioning.

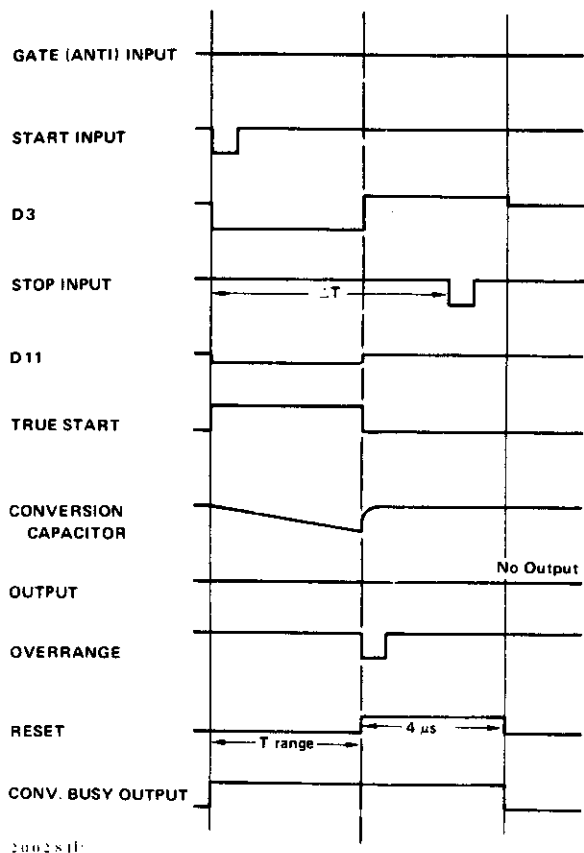


Fig. 6.7. Using Internal Strobe with Stop After End of Conversion.

Calibration Three critical calibrations that may need to be made are described below:

Discriminator Sensitivity The discriminators for the start input and stop input are calibrated to trigger at a level of approximately -250 mV. Control R148 is adjusted for the start input, and control R49 is for the stop input. A response cannot be triggered for the stop discriminator unless the start discriminator has been triggered at least 12 ns, but less than the selected time range, before the stop signal.

1. Set up the pulse generator (1) for negative 250 mV, approximately 100 ns wide. Connect this output to the start input.
2. Monitor the true-start output and adjust the start sensitivity trim potentiometer R148 until a true start is barely triggered.
3. Set fanout 2 or 3 (Fig. 6.1) to trigger start; delay the 250-mV signal pulse and insert it into the stop input of the 467.
4. Monitor TP3 (0200 printed circuit board) with the oscilloscope and adjust the stop sensitivity R49 so that the output barely triggers.

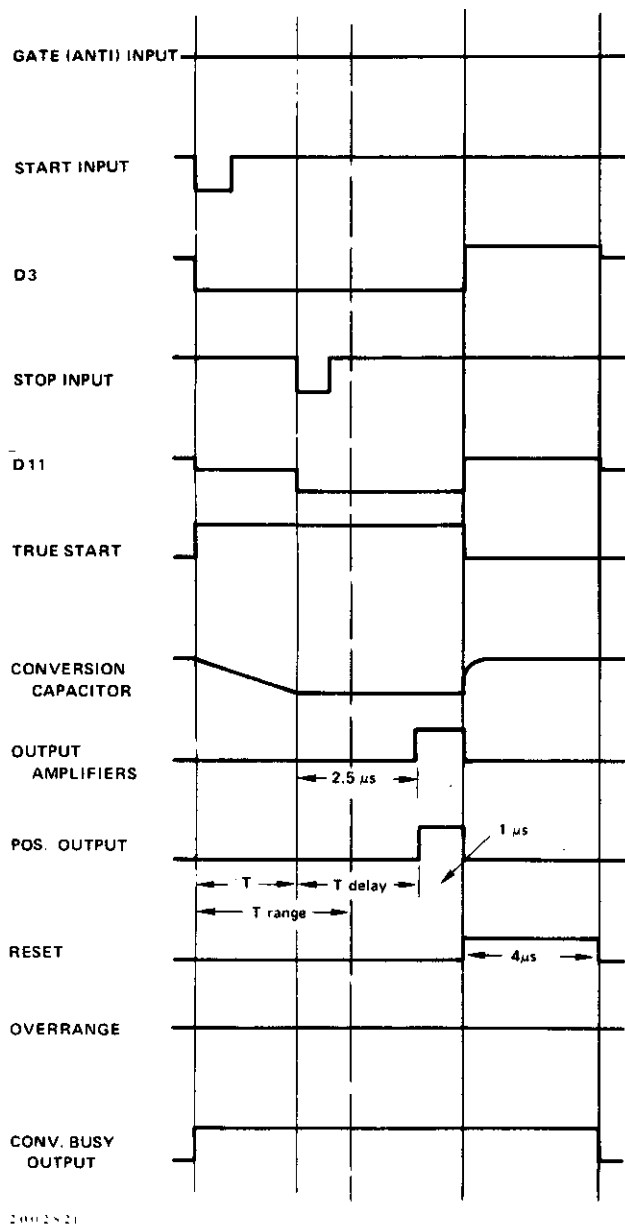


Fig. 6.8. Using Internal Strobe with Stop Timed Normally.

DC Level and Overage To calibrate the dc level and overrange, set up the circuit as shown in Fig. 6.1.

1. Put the front panel gate Anti Coinc/Coinc switch to Coinc so that the 467 will not accept pulses.
2. Monitor TP3 with a sensitive VTVM and adjust dc zero trim potentiometer R133 so that the dc voltage at TP3 is zero.
3. Return the Gate switch to Anti Coinc. Monitor TP3 with a calibrated oscilloscope and adjust stop delay to obtain a 10.1-V pulse at TP3.

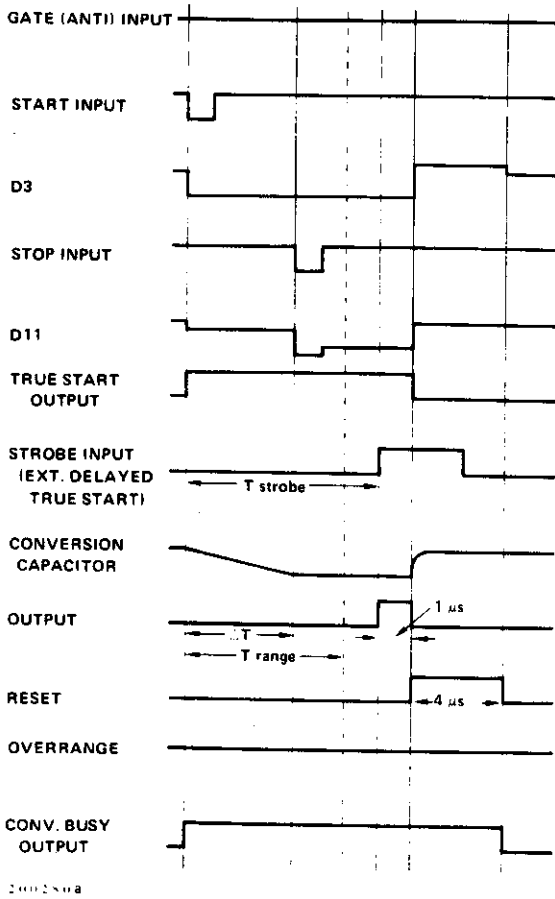


Fig. 6.9. Using External Strobe with Output Timed Normally.

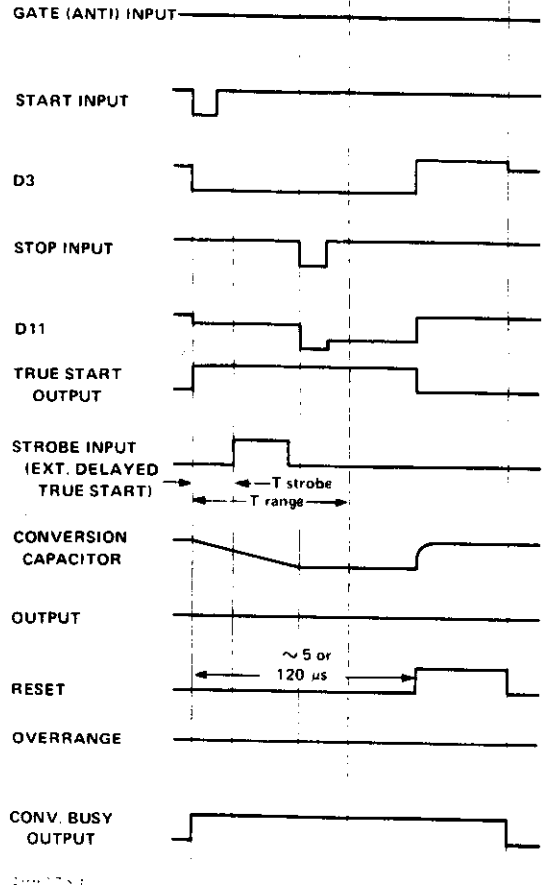


Fig. 6.10. Using External Strobe with Strobe Signal Arriving Before Conversion Is Complete.

4. Adjust the overrange trim potentiometer (R99) so that a signal is barely triggered. This sets the overrange threshold to 10.1 V.

Pulse Width Adjustment Use the same signal and circuit as in above.

1. Monitor the 467 output and adjust the stop signal delay to obtain an output pulse amplitude of 5 to 8 V.

2. Adjust the pulse gate width trim potentiometer R86 to obtain the desired pulse width. This is factory-set at approximately 2 μs.

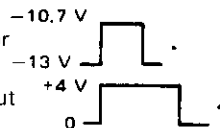
6.3. TROUBLESHOOTING

Use the tests in Section 6.1 and the circuit analysis in Section 5, and refer to schematics 467-0201-S1 and 467-0301-S1 and functional block diagram 467-0101-B1 to locate the faulty part or parts. A table of typical voltages is furnished at the end of this section for further identification of faulty circuit components.

Dynamic Signal To check signals under dynamic condition, set up as for "Resolution Tests" using Fig. 6.1. There are several tests for quickly finding trouble locations with an oscilloscope.

1. Observe input start signal to be > -0.3 V on 50Ω .

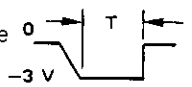
2. Check collector Q4 for



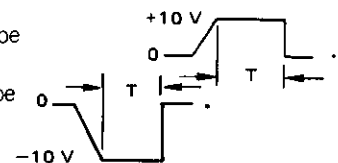
3. Check true-start output

4. Check that the input stop pulse is > -0.3 V on 50Ω and follows the start pulse within the time range selected.

5. Check signal at TP1 (O200 board) to be 0 $T > 1 \mu s < 6 \mu s$.



6. Check signal at TP2 to be



7. Check pulse at TP3 to be

6.4. TYPICAL DC VOLTAGES

Table 6.1 gives the typical dc voltages that were measured using the following control settings: Range, 0.2; Multiplier, 10; SCA Inhibit, Out; Logic Input switch, Anti Coinc; Strobe Sync, Int Stop; Stop Inhibit Mode, Out.

6.5. MODIFICATIONS

The 467 time range can be extended from its standard limit of 80 μ s so that it will measure time with a maximum range of 800 μ s full scale. The 467-0200 printed circuit board includes all the required components, and they can be used by installing jumpers at the appropriate points in the printed circuit board.

The jumpers that can be added are indicated in schematic 467-0201-S1 with the flagged reference to note 6. A total of four jumpers are involved, and the resulting Range Multiplier switch selections will be X10, X100, and X1000;

the X1000 selection uses the switch setting that is originally assigned to the X1 setting.

A slight loss of signal amplitude may be observed due to stretcher droop.

6.6. FACTORY REPAIR

This instrument can be returned to the ORTEC factory for service and repair at a nominal cost. Our standard procedure for repair ensures the same quality control and checkout that are used for a new instrument. Always contact the Customer Service Department at ORTEC, (615) 482-4411, before sending in an instrument for repair to obtain shipping instructions and so that the required Return Authorization Number can be assigned to the unit. Write this number on the address label and on the package to ensure prompt attention when it reaches the ORTEC factory.

Table 6.1. Typical dc Voltages.

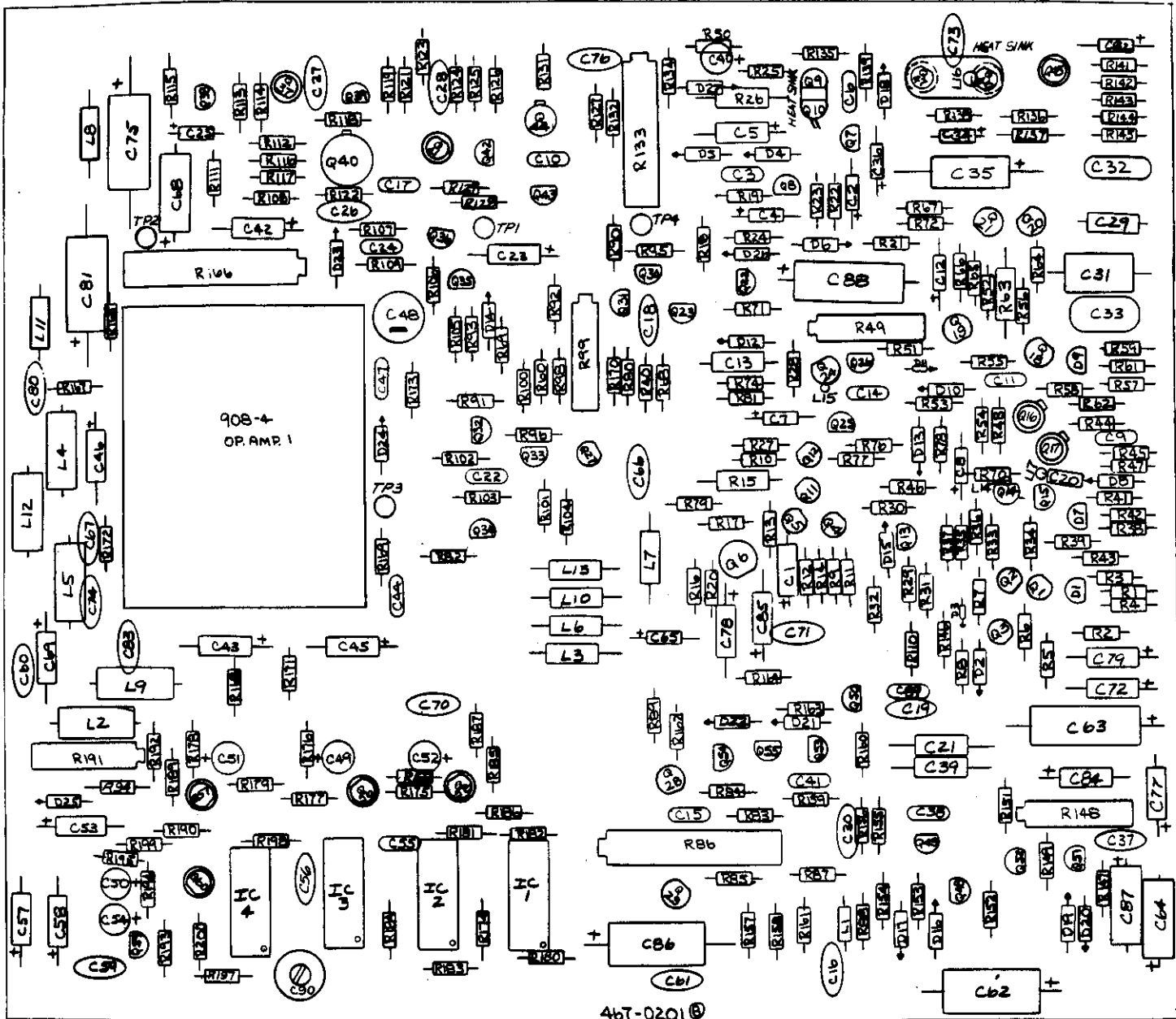
Checkpoint	Voltage (V) (or IC State)	Checkpoint	VOLTAGE (V) (or IC STATE)	Checkpoint	Voltage (V) (or IC State)	Checkpoint	Voltage (V) (or IC State)
Q2E	-0.75	Q23B	+0.73	Q45E	-12	IC1(12)	L
B	-0.011	C	+0.015	C	0	IC1(13)	H
Q3E	-0.68	Q24E	-11.32	Q46B	-11.37	IC2(1)	L
C	+1.1	C	0	Q47B	-11.38	IC2(8)	L
Q4E	+0.5	Q25B	-0.68	Q48E	+12.00	IC2(13)	H
B	-0.05	C	-0.02	B	+11.36	IC3(1)	+1.56
C	-13.12	Q26C	0	C	-11.38	IC3(2)	+1.70
Q5B	-0.23	Q27B	0	Q49B	+12.5	IC3(3)	H
C	-0.61	C	-5.73	C	0	IC3(5)	H
Q6C	+3.67	Q28B	-0.17	Q50B	0	IC3(6)	L
Q7E	+0.73	Q29B	-0.9	C	+5.23	IC3(9)	H
B	-2.75	C	-0.17	Q51E	-12.04	IC3(10)	L
Q8E	-7.3	Q31B	+0.67	B	-11.4	IC3(14)	+1.36
B	-6.62	C	-12.6	C	-1.97	IC3(15)	+1.57
C	+0.69	Q32B	+0.01	Q52B	-11.92	IC4(7)	H
Q10E	+0.02	C	0	C	0	IC4(14)	H
B	+0.72	Q33E	0	Q53E	+2.58	IC7(1)	L
C	+1.36	C	+12	B	+3.24	IC7(2)	L
Q11E	-12.7	Q34B	+0.74	Q54B	0	IC7(3)	H
C	-7.32	C	0	C	+8.00	IC7(5)	H
Q12C	-0.23	Q35E	-12.64	Q55B	0	IC7(7)	Ground
Q13B	+0.72	B	-12.6	Q56E	0	IC7(8)	H
C	+0.14	Q36B	-12	B	+0.23	IC7(10)	L
Q14E	+1.15	C	-3.31	C	+12	IC7(13)	H
B	+1.85	Q37E	0	Q57E	0	IC7(14)	V _{cc}
C	+4.3	B	+0.60	B	+0.16	IC8(1)	Open
Q15B	+0.097	Q38E	-6.8	C	+12	IC8(2)	H
C	+7.5	B	-6.1	Q58E	0	IC8(3)	L
Q16B	0	Q39E	+19.8	B	+0.19	IC8(4)	Ground
C	+0.32	Q40E	-0.7	C	+12	IC8(5)	L
Q17C	+2.2	B	-0.08	Q59E	-0.40	IC8(6)	L
Q18E	-0.73	C	+5.14	B	+0.21	IC8(7)	H
B	0	Q40B	-0.08	Q60E	0	IC8(8)	Ground
Q19E	-0.68	C	+19.2	B	+0.15	IC8(9)	H (Open)
C	+1.14	Q41E	+11.9	C	+12	IC8(11)	V _{cc}
Q20E	+0.47	B	+11.2	D18 Anode	-21.2	IC8(12)	L
B	+0.02	Q42E	+7.04	D25 Cathode	+5.63	IC8(14)	+1.5
C	+1.14	Q44A-S	+0.56	IC1(5)	H	IC8(15)	+1.5
Q21B	-0.233	D	+0.015	IC1(6)	L	IC8(16)	V _{cc}
C	-5.31	G	+6.42	IC1(8)	L	IC9(1)	H
Q22E	-4.93	Q44B-S	+0.541	IC1(9)	H	IC9(6)	L
B	-5.31	G	+0.02	IC1(10)	L	IC9(7)	Ground
C	-24	D	+6.41	IC1(11)	H	IC9(12)	L
						IC9(14)	V _{cc}

**BIN/MODULE CONNECTOR PIN ASSIGNMENTS
FOR AEC STANDARD NUCLEAR INSTRUMENT MODULES
PER TID-20893**

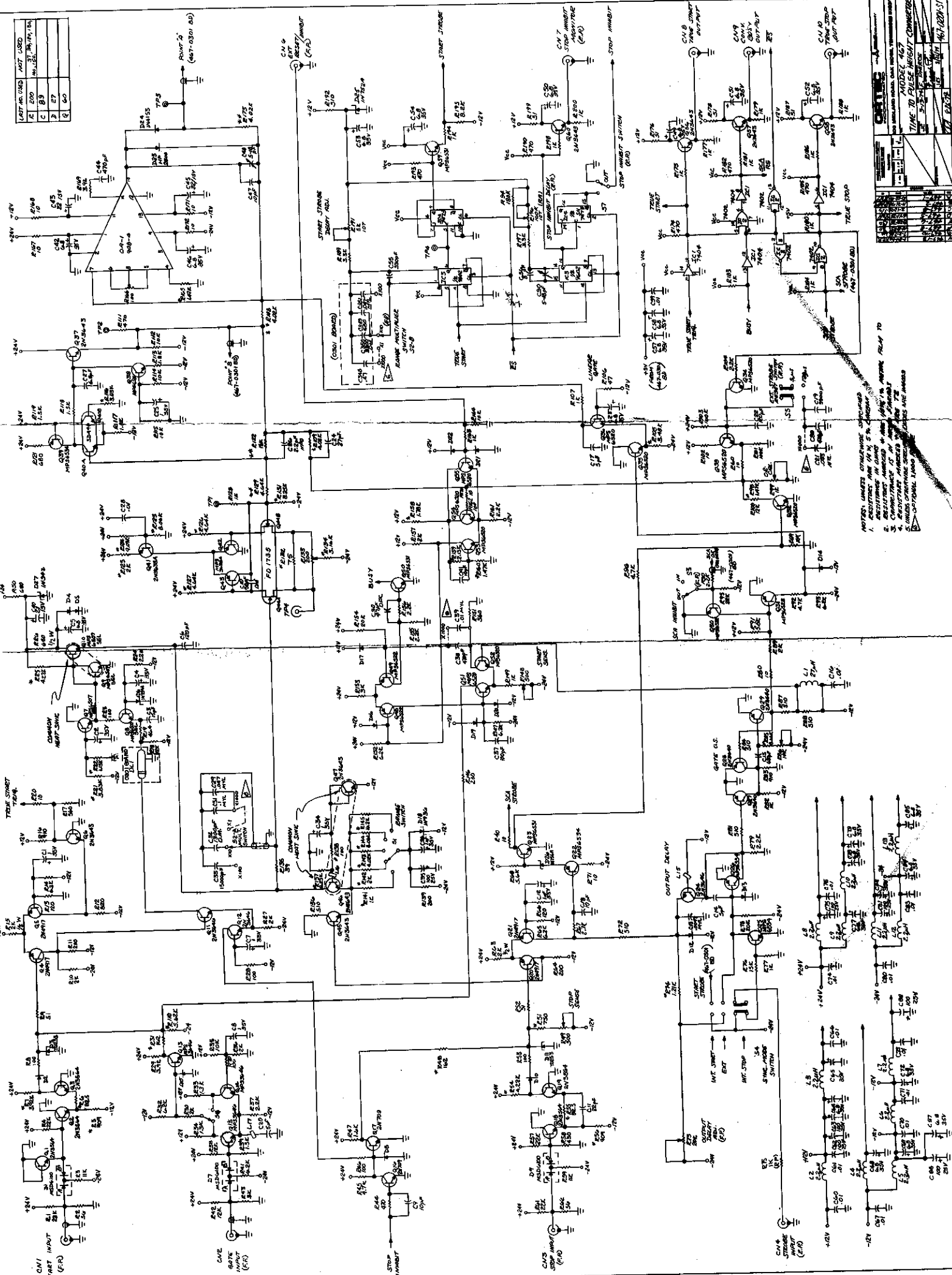
Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	-3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	-24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	-6 volts	*33	115 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	**35	Reset (Scaler)
14	Spare	**36	Gate
15	Reserved	**37	Reset (Auxiliary)
*16	+12 volts	38	Coaxial
*17	-12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	115 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

Pins marked (*) are installed and wired in ORTEC 401A and 401B Modular System Bins.

Pins marked (*) and (**) are installed and wired in EG&G/ORTEC-HEP M250/N and M350/N NIMBINS.



REF. NO.	USED	NOT USED
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- NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED
 2. CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED
 3. COMPONENTS AT AN ANGLE TO THE MAIN SCHEMATIC ARE SHOWN IN THE MARGIN
 4. DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
 5. UNLESS OTHERWISE SPECIFIED THE TOLERANCE IS ±1%

UNIT

MODEL 407

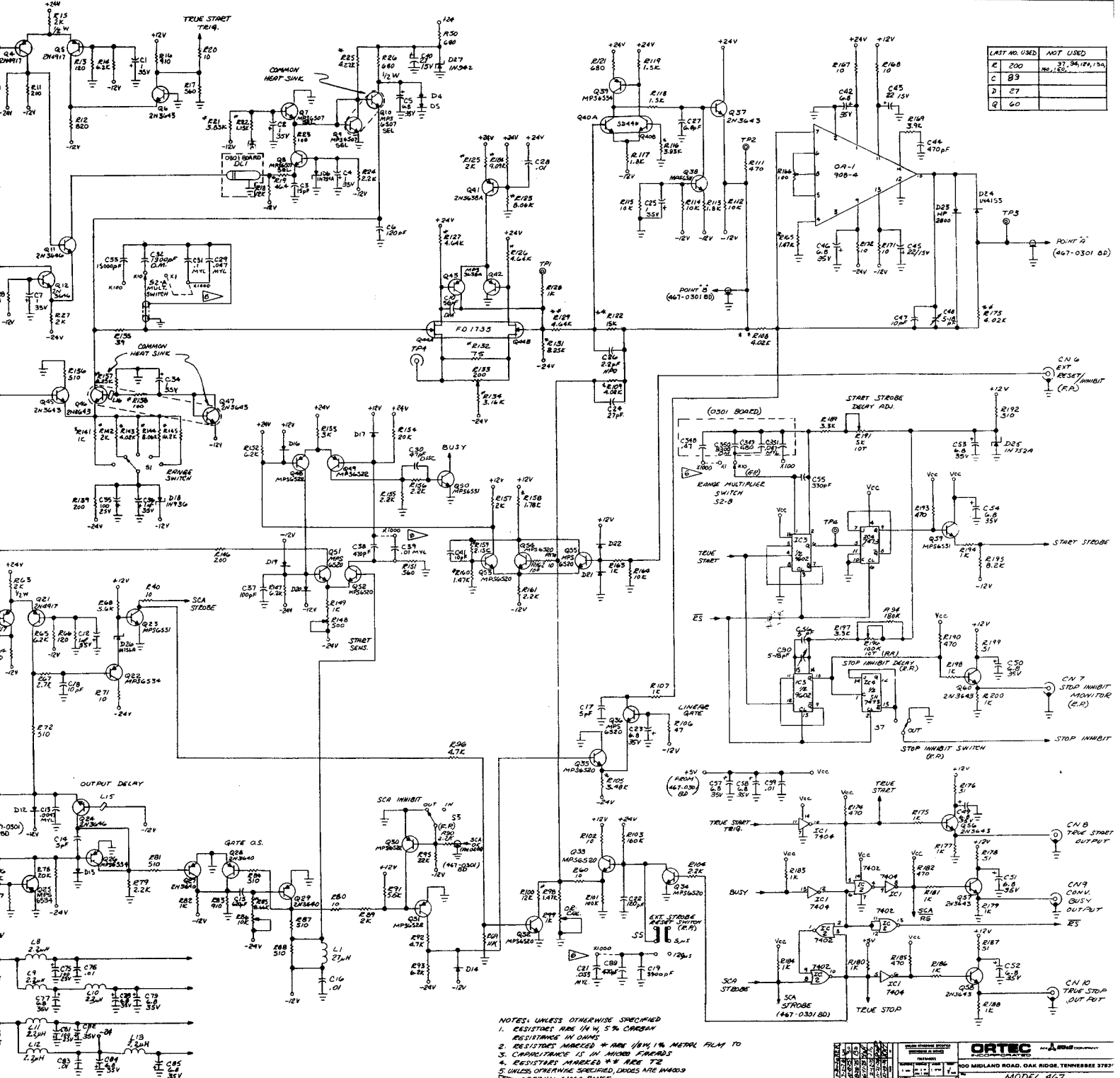
TIME TO PULSE HEIGHT CONVERTER

DATE: 11/15/54

REV: 1

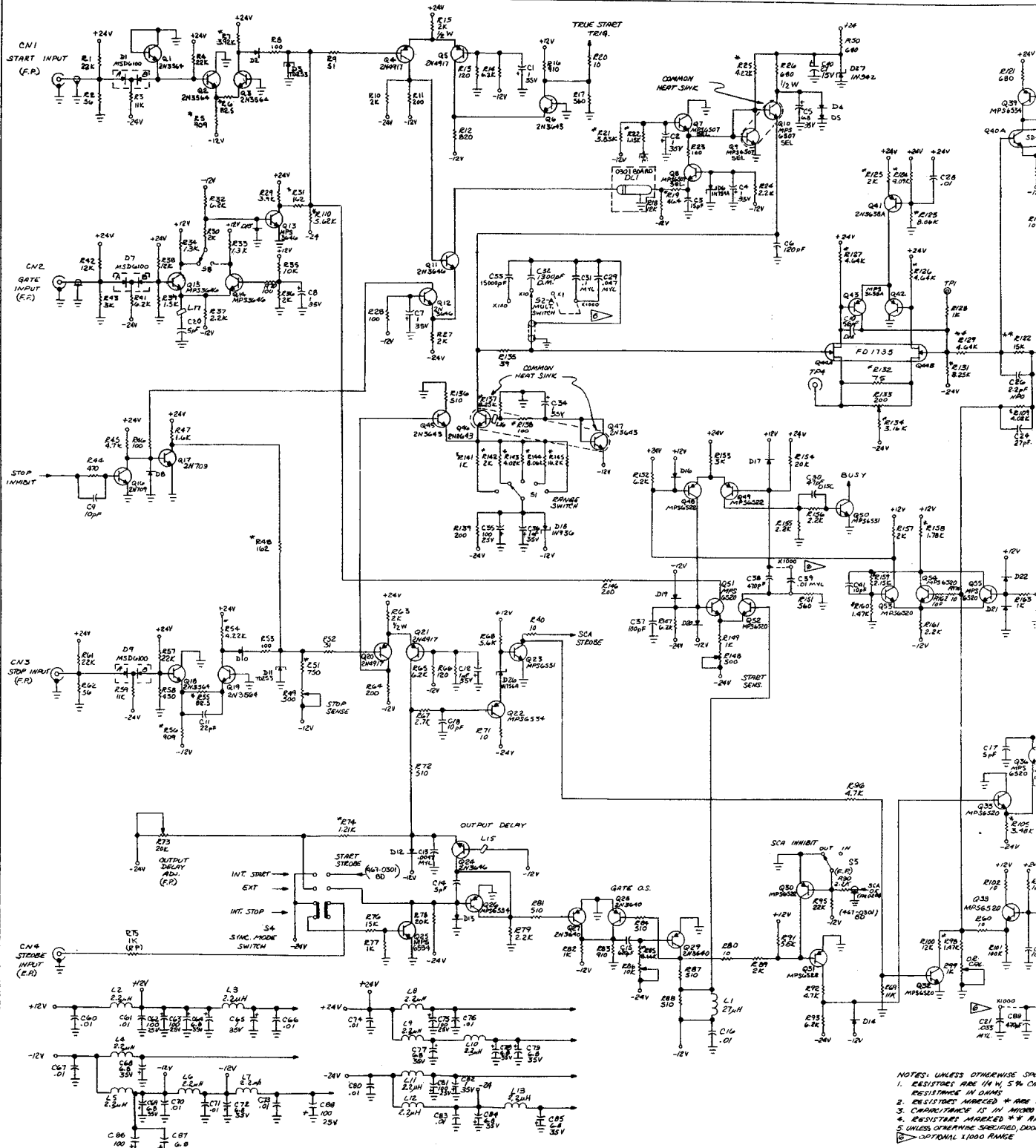
467-0201-51

LAST NO. USED	NOT USED
R 200	37, 34, 174, 154
C 3	3
D 27	
Q 60	



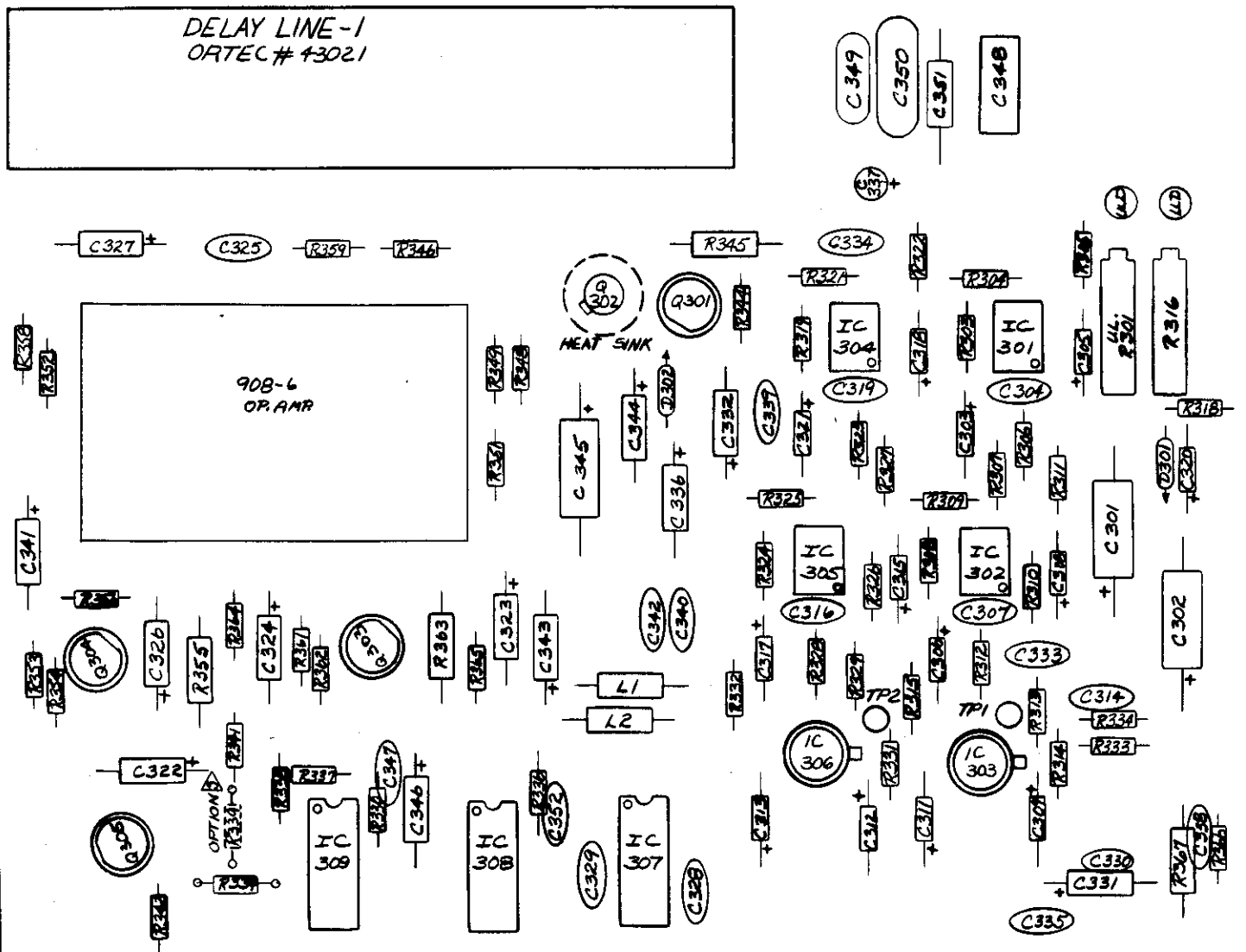
NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTORS ARE 1/4 W, 5% CERRAM
 RESISTANCE IN OHMS
 2. RESISTORS MARKED * ARE 1/4 W, 1% METAL FILM TO
 3. CAPACITANCE IS IN MICRO FARADS
 4. RESISTORS MARKED ** ARE T2
 5. UNLESS OTHERWISE SPECIFIED, DIODES ARE 1N4005
 6. OPTIONAL 1000 RANCE

100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37837	
MODEL 467 TIME TO PULSE HEIGHT CONVERTER	
3-74 100-1000 100-1000 100-1000	467-0201-S1

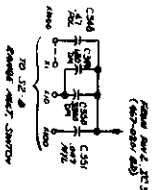
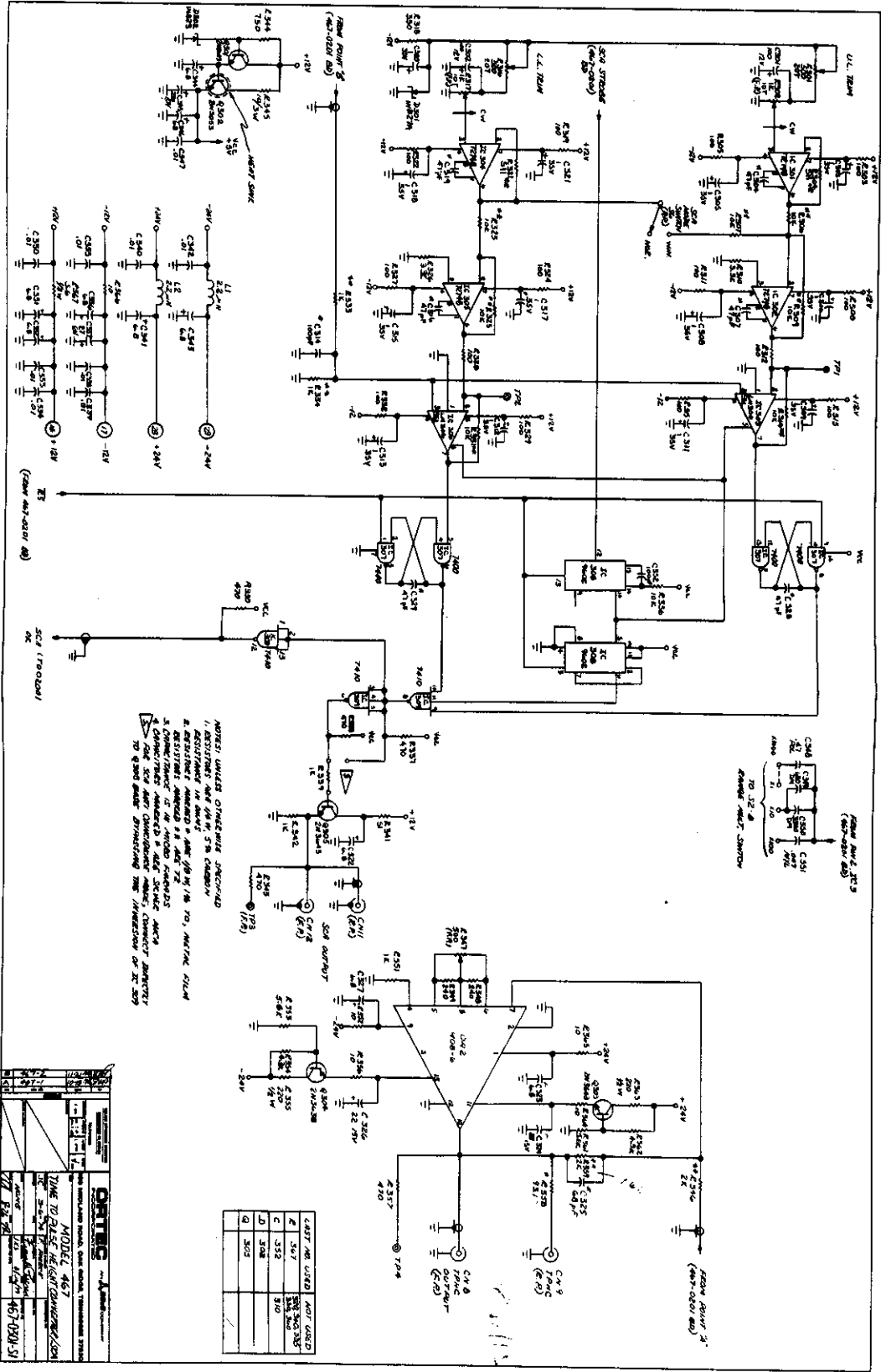


- NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 1/4 W, 5% CN
 2. RESISTORS MARKED * ARE IN OHMS
 3. CAPACITANCE IS IN MICRO
 4. RESISTORS MARKED ** ARE 1% UNLESS OTHERWISE SPECIFIED, DOD
 5. OPTIONAL 1000 RANGE

DELAY LINE-1
ORTEC # 43021



467-0301(B)



NOTES: 1. CHECK THE CONNECTIONS OF THE 6X4 AND 6X5 TUBES. 2. RESISTOR VALUES IN PARENTHESIS ARE FOR THE 6X4 AND 6X5 TUBES. 3. CONNECT THE 6X4 AND 6X5 TUBES TO THE FILAMENT WINDING OF THE 6X4 AND 6X5 TUBES. 4. CHECK THE CONNECTIONS OF THE 6X4 AND 6X5 TUBES TO THE FILAMENT WINDING OF THE 6X4 AND 6X5 TUBES.

LIST AND USED	NOT USED
A 5A7	6X4
B 5B7	6X5
C 5C7	6X6
D 5D7	6X7
E 5E7	6X8
F 5F7	6X9
G 5G7	6X10
H 5H7	6X11
I 5I7	6X12
J 5J7	6X13
K 5K7	6X14
L 5L7	6X15
M 5M7	6X16
N 5N7	6X17
O 5O7	6X18
P 5P7	6X19
Q 5Q7	6X20
R 5R7	6X21
S 5S7	6X22
T 5T7	6X23
U 5U7	6X24
V 5V7	6X25
W 5W7	6X26
X 5X7	6X27
Y 5Y7	6X28
Z 5Z7	6X29

OPTICS

THE FOLLOWING INFORMATION IS FOR YOUR INFORMATION ONLY. IT IS NOT TO BE USED AS A BASIS FOR ANY CLAIMS OR DAMAGES.

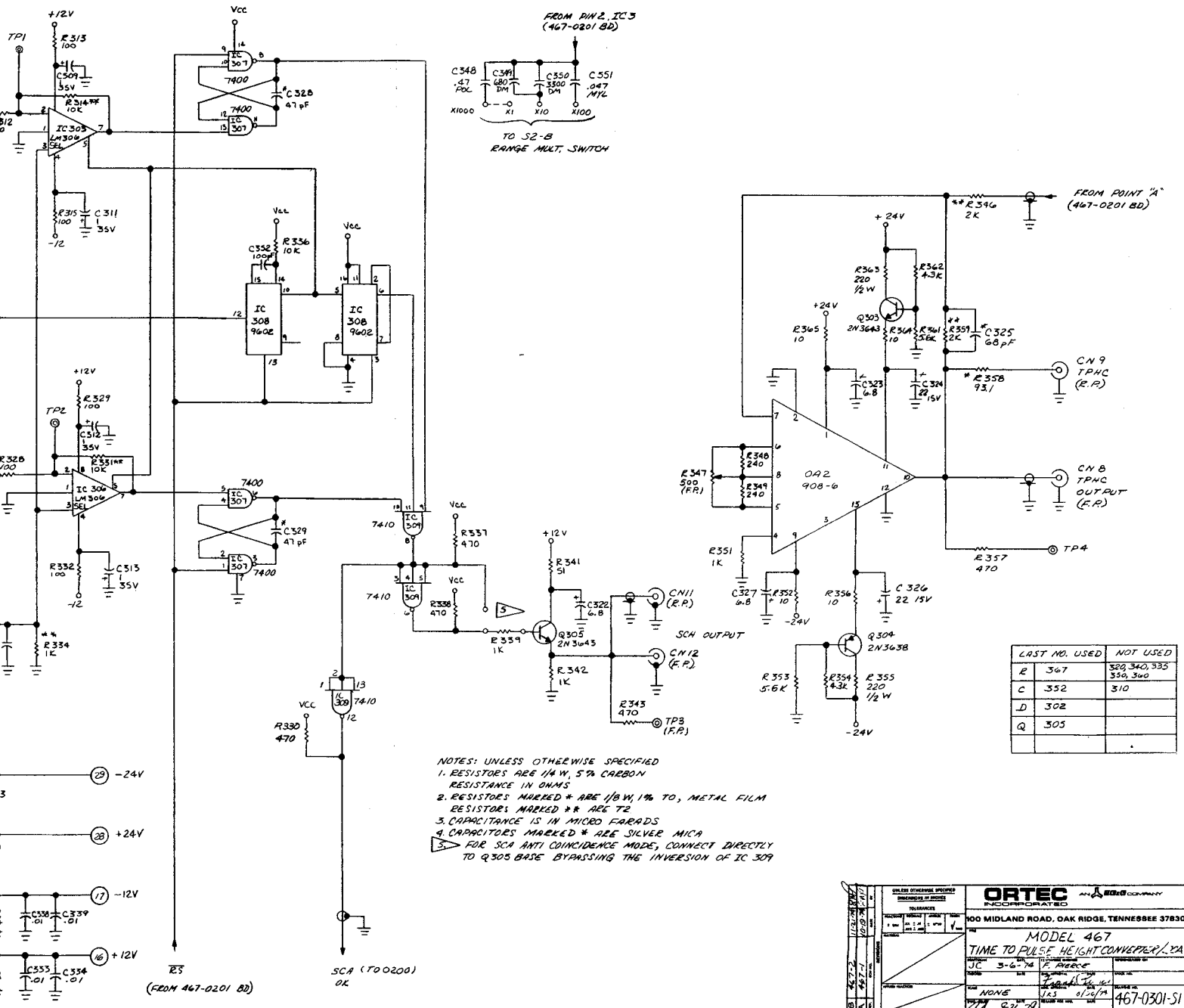
MODEL 467

TYPE TO BE USED IN CONNECTION WITH THIS MODEL

DATE: 1/15/50

REV: 1/15/50

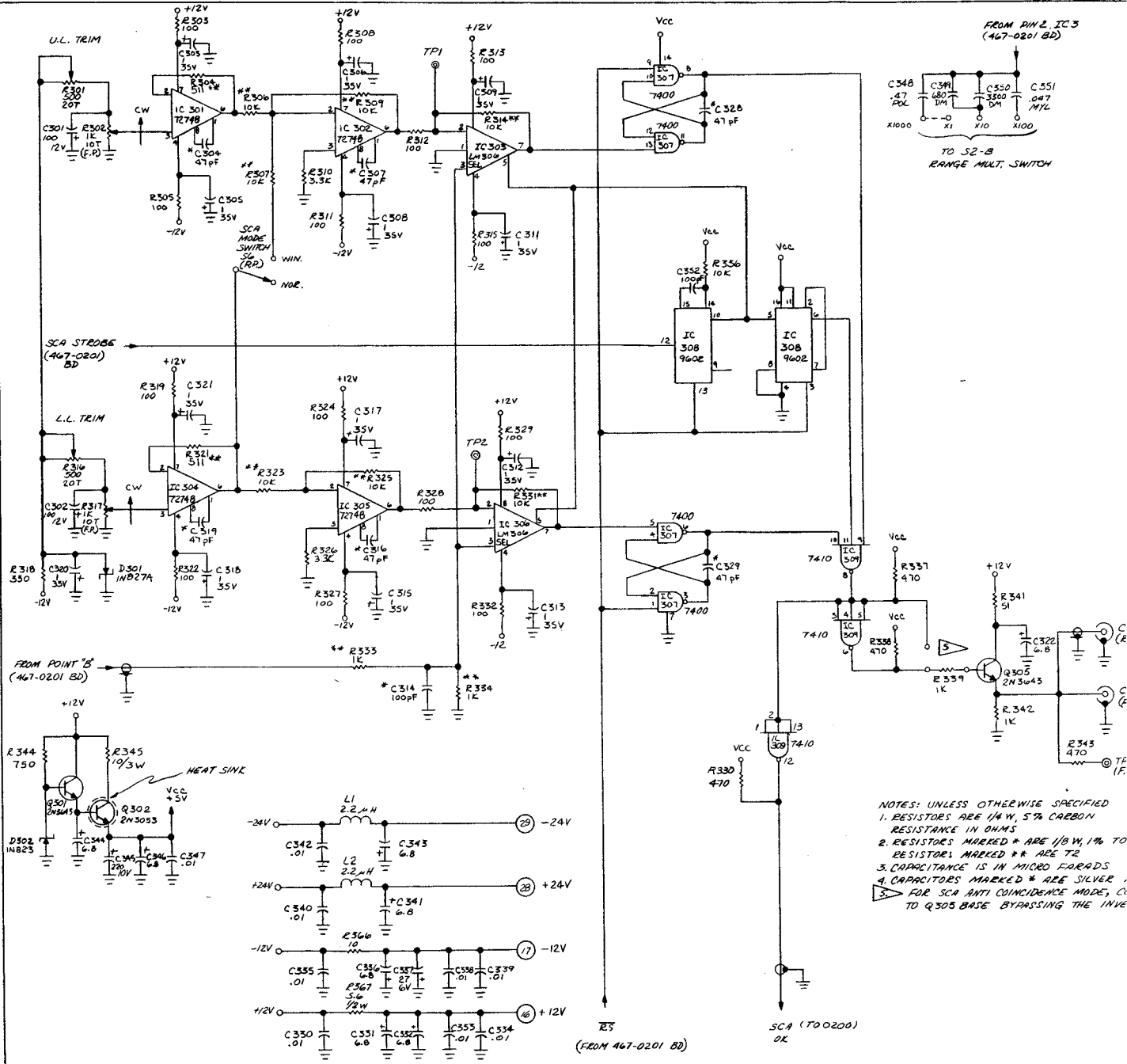
467-000-51



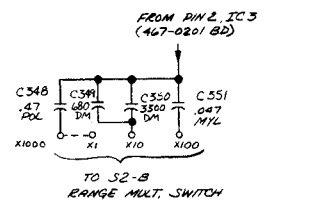
NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTORS ARE 1/4 W, 5% CARBON RESISTANCE IN OHMS
 2. RESISTORS MARKED * ARE 1/8 W, 1% TO, METAL FILM RESISTORS MARKED ** ARE TE
 3. CAPACITANCE IS IN MICRO FARADS
 4. CAPACITORS MARKED * ARE SILVER MICA
 5. FOR SCA ANTI COINCIDENCE MODE, CONNECT DIRECTLY TO Q305 BASE BYPASSING THE INVERSION OF IC 309

LAST NO. USED	NOT USED
R 367	329, 340, 333 33a, 34a
C 352	310
D 302	
Q 305	

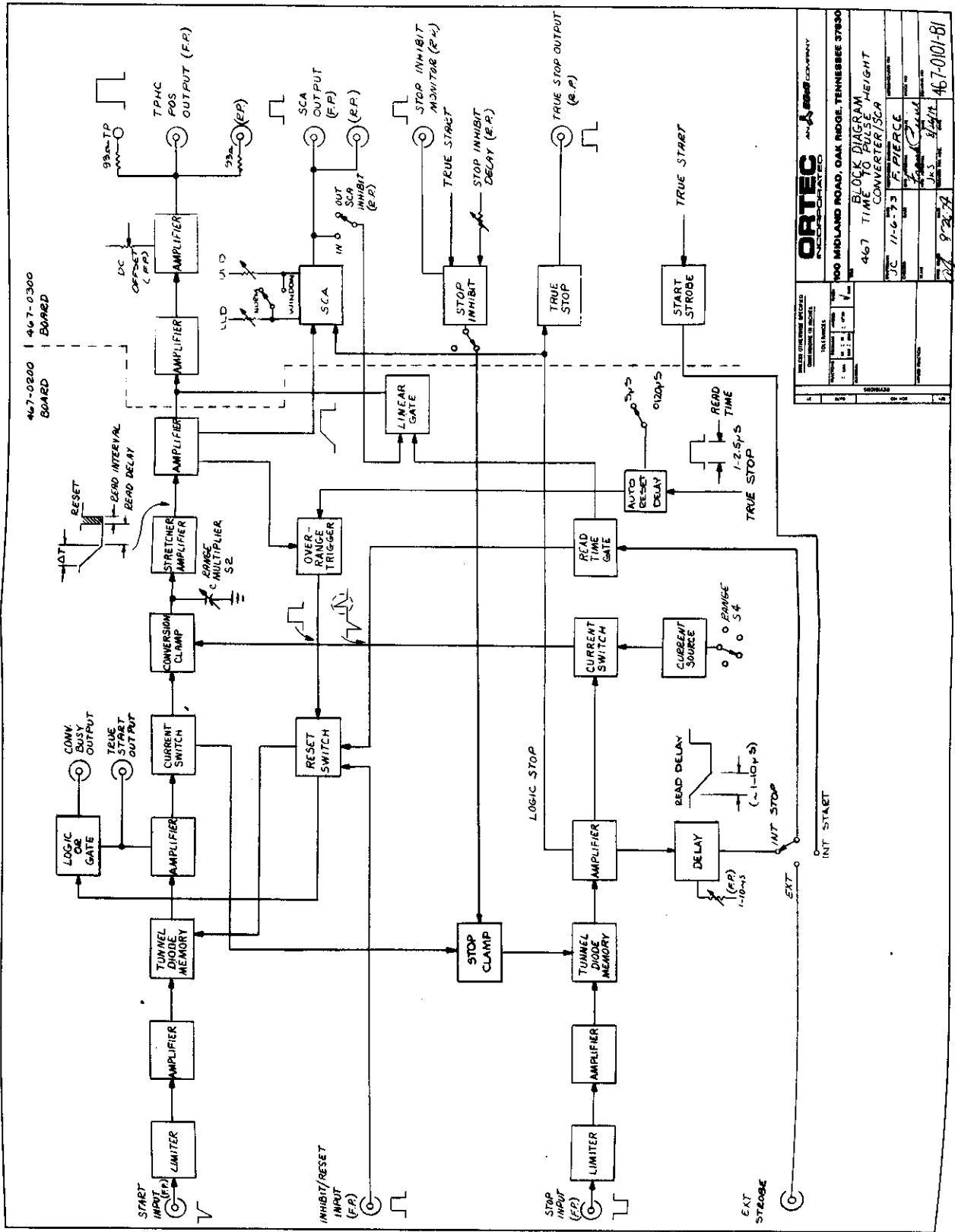
ORTEC ELECTRONICS SPECIFICATIONS		ORTEC INCORPORATED	
MODEL 467		AN IBM COMPANY	
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830			
TIME TO PULSE HEIGHT CONVERTER, 2A			
DATE	3-6-74	DESIGNED BY	F. ARBEE
REV	1	CHECKED BY	
APPROVED BY		DATE	
NAME	NONE	REVISION	113
DATE	8/24/74	BY	
REV	1	DATE	467-0301-S1



- NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTORS ARE 1/4W, 5% CARBON RESISTANCE IN OHMS
 2. RESISTORS MARKED * ARE 1/8W, 1% TO RESISTORS MARKED ** ARE T2
 3. CAPACITANCE IS IN MICRO FARADS
 4. CAPACITORS MARKED * ARE SILVER
 5. FOR SCA ANTI COINCIDENCE MODE, C₃ TO Q305 BASE BYPASSING THE INVE



E3 (FROM 467-0201 BD)
 SCA (TO 0200) OK



ORTEC PRECISION ELECTRONICS	
100 MIDLAND ROAD, OAK RIDGE, TENNESSEE 37830	
BLOCK DIAGRAM WEIGHT 467 TIME CONVERTER/SCA	
DATE: JE 11-6-73	DRAWN BY: F. PIERCE
CHECKED BY: [Signature]	DATE: 9/24/74
PROJECT NO.: 467-0101-B1	SHEET NO.: 9-25A