SPECIFICATIONS FOR THE

MODEL 7186/7186H

16-CHANNEL CAMAC TDC

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MODEL 7186/7186H
16 CHANNEL CAMAC TDC

FEATURES:

* Model 7186 features NIM Inputs with LEMO Connectors
* Model 7186H features Differential ECL Inputs
* 7.8 μsec conversion and processing time
* 12-Bit Dynamic Range, resolution down to 25 psec/count
* Programmable Pedestal Correction
* Sparse Data Scan with Lower and Upper Time Cuts
* Fast Clear and Inhibit
* COMMON START or COMMON STOP
* Built-in Test Features check TAC and digitization

Description:

The Model 7186/H TDC implements 16 channels of Time to Amplitude Conversion (TAC) followed by a digital processing section and CAMAC interface in a single width CAMAC module. To minimize data readout time, the module performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following the COMMON input. It may be delayed by a user-programmable amount to allow time for derivation of FAST CLEAR signals.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel FAST CLEAR or CAMAC commands.

Several user selectable time ranges are provided:

Range	Resolution		Range	Resolution
100 nSec	25 psec		1 μSec	.25 nSec
200 nSec	50 psec	OR	2 μSec	.50 nSec
400 nSec	100 pSec		4 μSec	1.0 nSec
800 nSec	200 pSec		8 μSec	2.0 nSec

Note: All channels need not have the same scale factors. Custom ranges are available when ordering.

Individual START or STOP inputs:

7186 : Fast negative NIM, direct coupled bridging input (1KΩ impedance); user must terminate end of daisy chain with 50Ω; minimum pulse width 10 nSec.

7186H : 100Ω, differential ECL, 100mv threshold. Minimum input pulse width 10 nSec.

Common Control Signals (COMMON, CLEAR, INHIBIT, TEST):

7186 : Two bridged LEMO inputs to facilitate daisy chaining (1 KΩ impedence).

7186H : Two pairs of differential ECL inputs to facilitate daisy chaining (1 KΩ impedence).

Digitization Time : 7.8 μsec minimum, includes 1 μsec for settling and for accepting Fast Clear signals prior to digitization. Timing is measured from the leading edge of the COMMON signal. Digitization may be delayed by 0 to 16 μSec in 62.5 nsec increments with external jumpers. An increased delay is mandatory in COMMON START mode and may be used in either mode to allow a greater acceptance window for Fast Clear signals. For ranges ≤ 800 nsec full scale, increasing the delay by more than 4 μsec after the first STOP may result in a degradation in module performance.

Fast Clear : Clear resets the Hit Register and the front ends as follows:

100, 200, 400, 800 nsec full scale:

t < (COMMON - 850 nsec): resets any channels that have received START signals; no effect on digitization.

(COMMON - 700 nsec) < t < DIGITIZATION: resets front ends and aborts digitization cycle.

t > DIGITIZATION: resets front ends; no effect on digitization.

1, 2, 4, 8 μsec full scale:

t < (COMMON - 2.2 μsec): resets any channels that have received START signals; no effect on digitization.

(COMMON - 1.9 μsec) < t < DIGITIZATION: resets front ends and aborts digitization cycle.

t > DIGITIZATION: resets front ends; no effect on digitization.

BUSY is asserted following clear to allow time for the front ends to fully reset.

Inhibit Input : Inhibits TAC and digitization. Must be removed at least 10 nsec before START or COMMON signals for those signals to be recognized.

Front end inhibit: must be applied no later than the START signal.

Digitization inhibit: must be present 10 nsec before the COMMON input to inhibit digitization.

Test Function : Common to all channels. Used in conjunction with the COMMON START/STOP input to test operation of the TDC anywhere within the range.

Test Function : Common to all channels. Used in conjunction with the COMMON START/STOP input to test operation of the TDC anywhere within the range.

Busy Output 7186 : LEMO output. NIM current switching bridged output (32 ma);

7186H : ECL output. Two differential pairs.
Active as follows:
From receipt of COMMON until the event has been aborted by a Fast Clear or has been fully digitized and read out through the sparse data port. BUSY follows the Hit Register and thus may also be released by clearing the Hit Register.
For 800 nsec following FAST CLEAR (2.4 μsec for ranges ≥ 1 μsec)
During any CAMAC addressing of the module.

FRONT END PERFORMANCE:

START/STOP pedestal : 20 nsec. Front ends are offset this amount to allow use of full dynamic range

Linearity : Integral - < 3 counts over 10% to 90% of range
Differential - <.025% of full scale

Noise & Jitter : typically < 20 psec RMS

Crosstalk : < 3 LSB maximum between adjacent channels

Stability : Gain: 100 ppm/°C typ
Offset: .15 counts/°C typ

POWER REQUIREMENTS: +6v - 2.7 amps typ; -6v - 2.2 amps typ
+24v - 180 ma typ
Forced cooling is recommended.

ADDITIONAL TEST FEATURES

Calibration Check : Simulates a Start/Stop sequence under CAMAC control to verify operation of the module. CAMAC selectable nominal 1/3 or 2/3 full scale calibration for each full scale range. Not intended for use in calibrating the module.

CAMAC check : Loads a predetermined pattern to simulate the outputs of the A/D converters. Useful for verifying the operation of the digital processing sections of the module.

CAMAC DATAWAY OPERATIONS

F(0)·A(X) : Read event data memory for Channel (X+1). Data word contains the data and the channel number.

F(1)·A(X) : Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).

F(4)·A(0) : Read Sparse Data. Only those channels with data that falls between the upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false.

F(6)·A(0) : Read the TDC control register. This tells which of the Pedestal, Upper Threshold or Lower Threshold are enabled, as well as the programming of the Processing Start Delay.

F(6)·A(1) : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.

F(8) : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(9) : Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(10) : Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

F(11)·A(0): Reset the Control Register. Occurs on S2 strobe.

F(11)·A(1): Reset the hit register. No effect on data memory. Occurs on S2 strobe.

F(11)·A(2): Reset the test register. Occurs on S2 strobe.

F(11)·A(3): Reset the hit register and data memory. Occurs on S2 strobe.

F(16)·A(X): Write to data memory for channel (X+1).

F(17)·A(0): Select the Pedestal Memory for the next F1 or F20 operation.

F(17)·A(1): Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)·A(2): Select the Upper Threshold Memory for the next F1 or F20 operation.

F(17)·A(4): Select the Test Register for the next F20 operation.

F(19)·A(0): Selectively enable the Pedestal, Upper and Lower Thresholds.

F(20)·A(X): Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation.
Program the test register if it was selected by the most recent F17 operation. (X) is used to select one of the following simulated data patterns to be used for the test: 001001001001, 010010010010, 100100100100, 111111111111.

F(23)·A(0): Selectively disable the Pedestal, Upper and Lower Thresholds.

F(24) : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(25)·A0 : Digital test. Initiates a data acquisition cycle using the value stored in the test register by the most recent F20 command.

F(25)·A1 : Test. Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)·A2 : Test. Runs a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

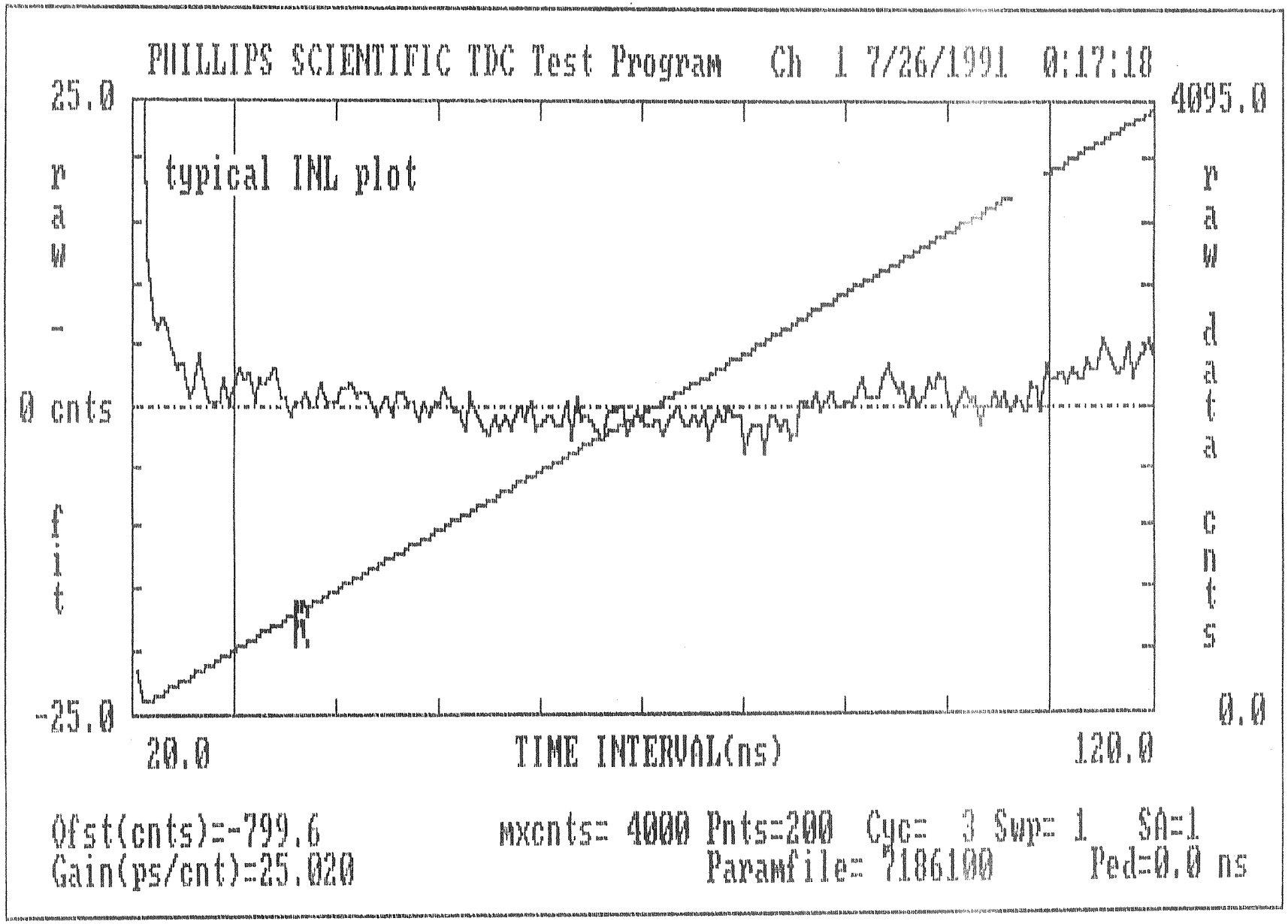
F(26) : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

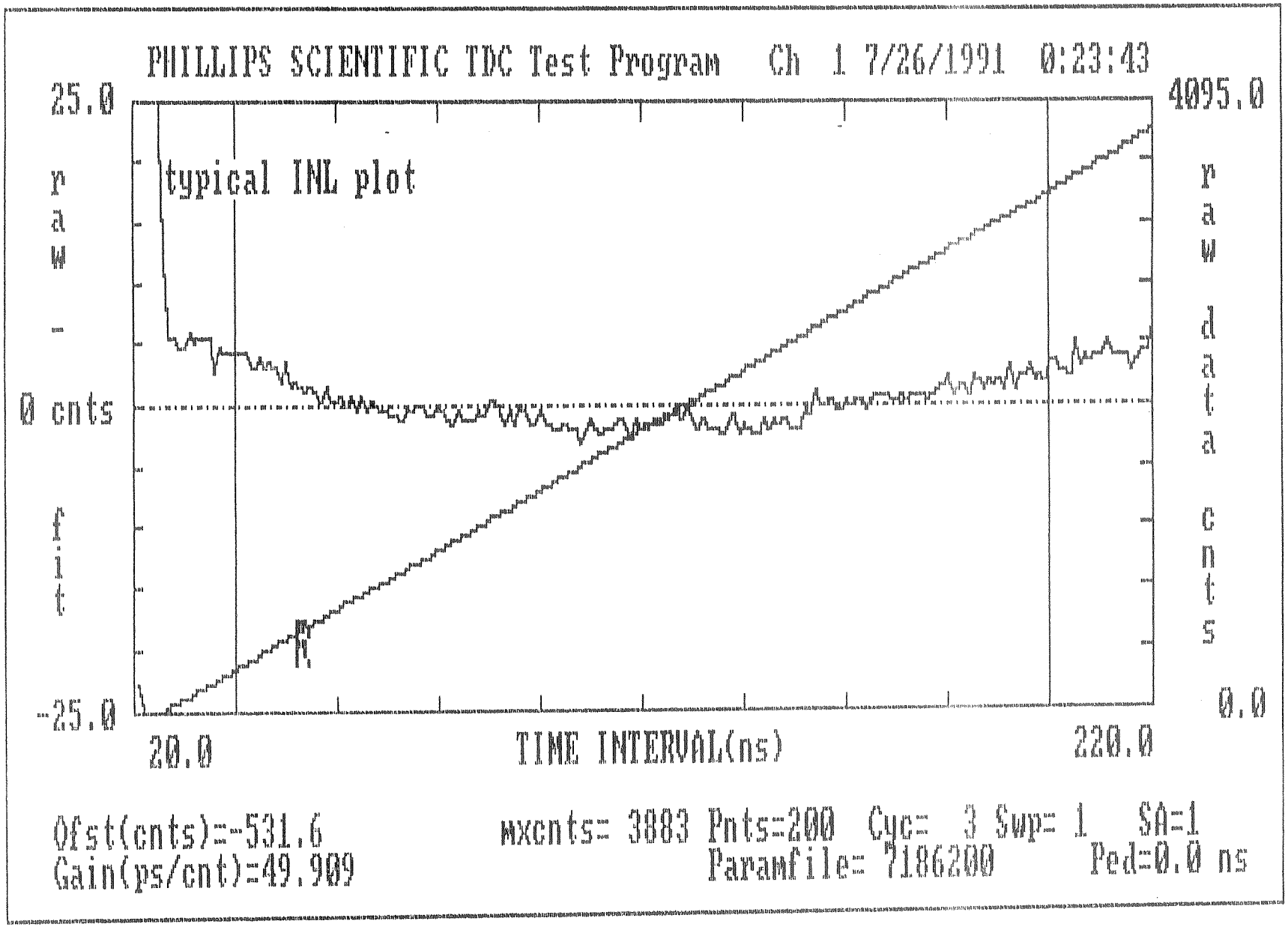
CAMAC NON-DATAWAY COMMANDS

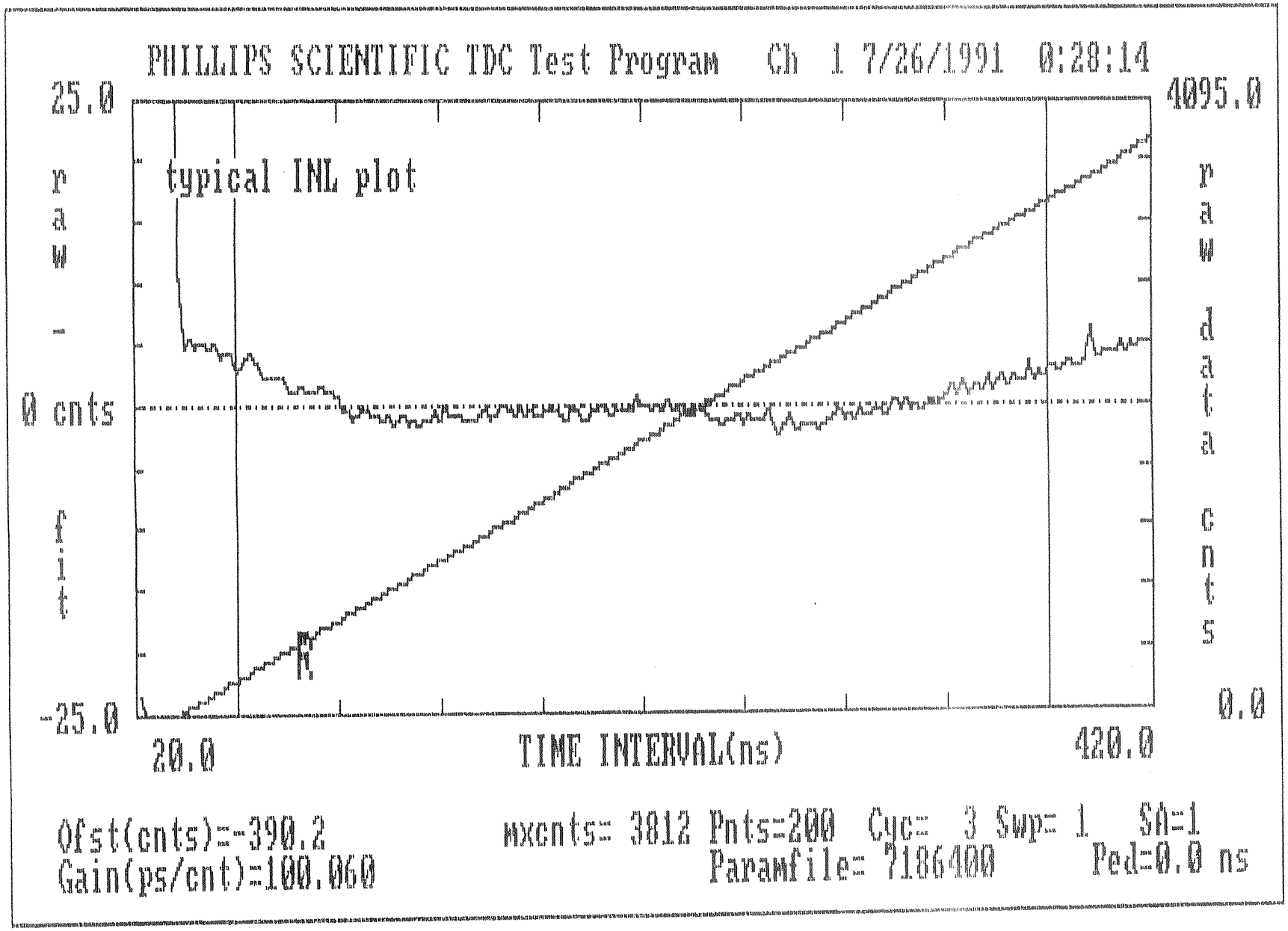
C, Z : Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the hit register. Occurs on the S2 strobe.

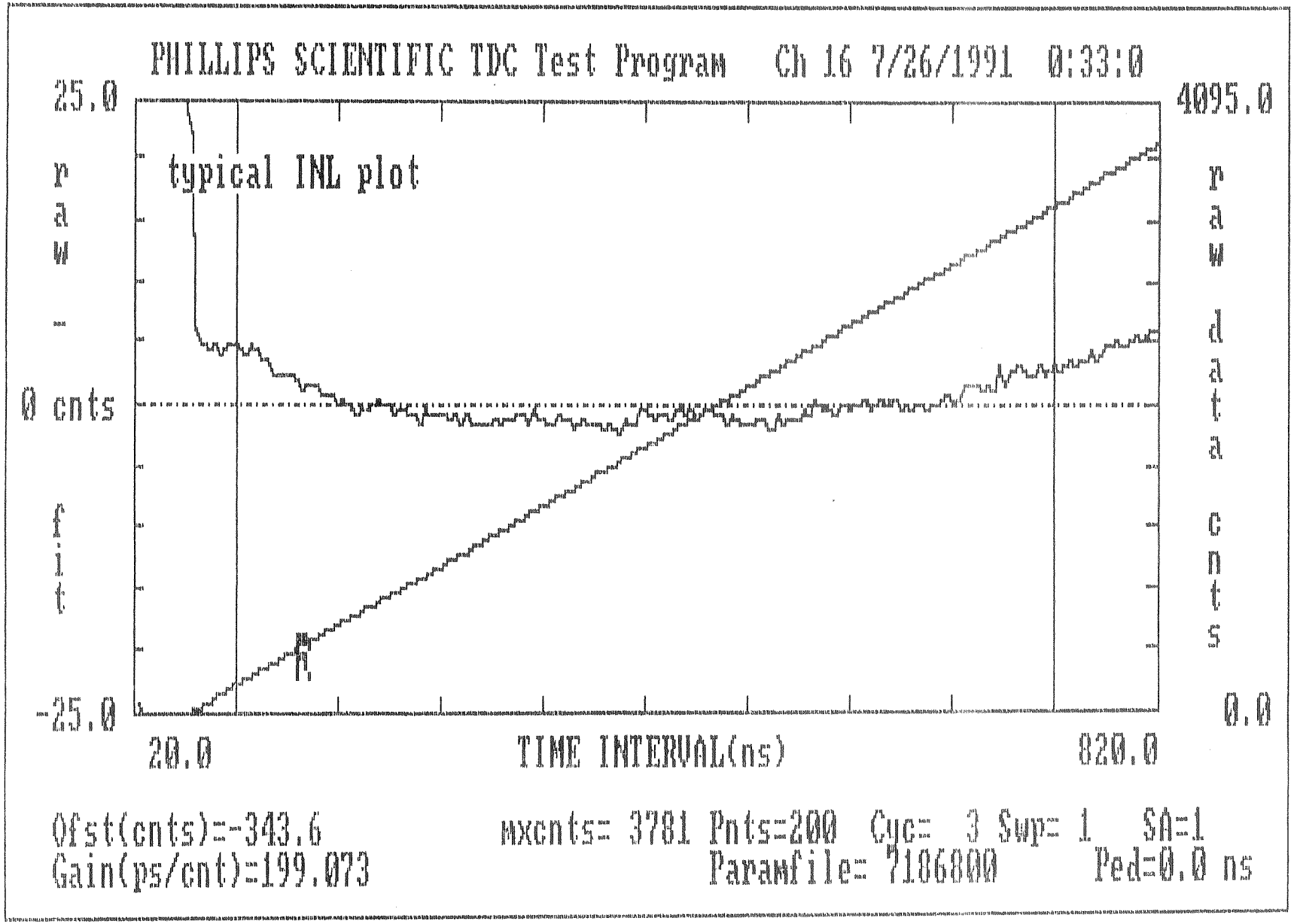
I : Inhibit all Camac Functions.

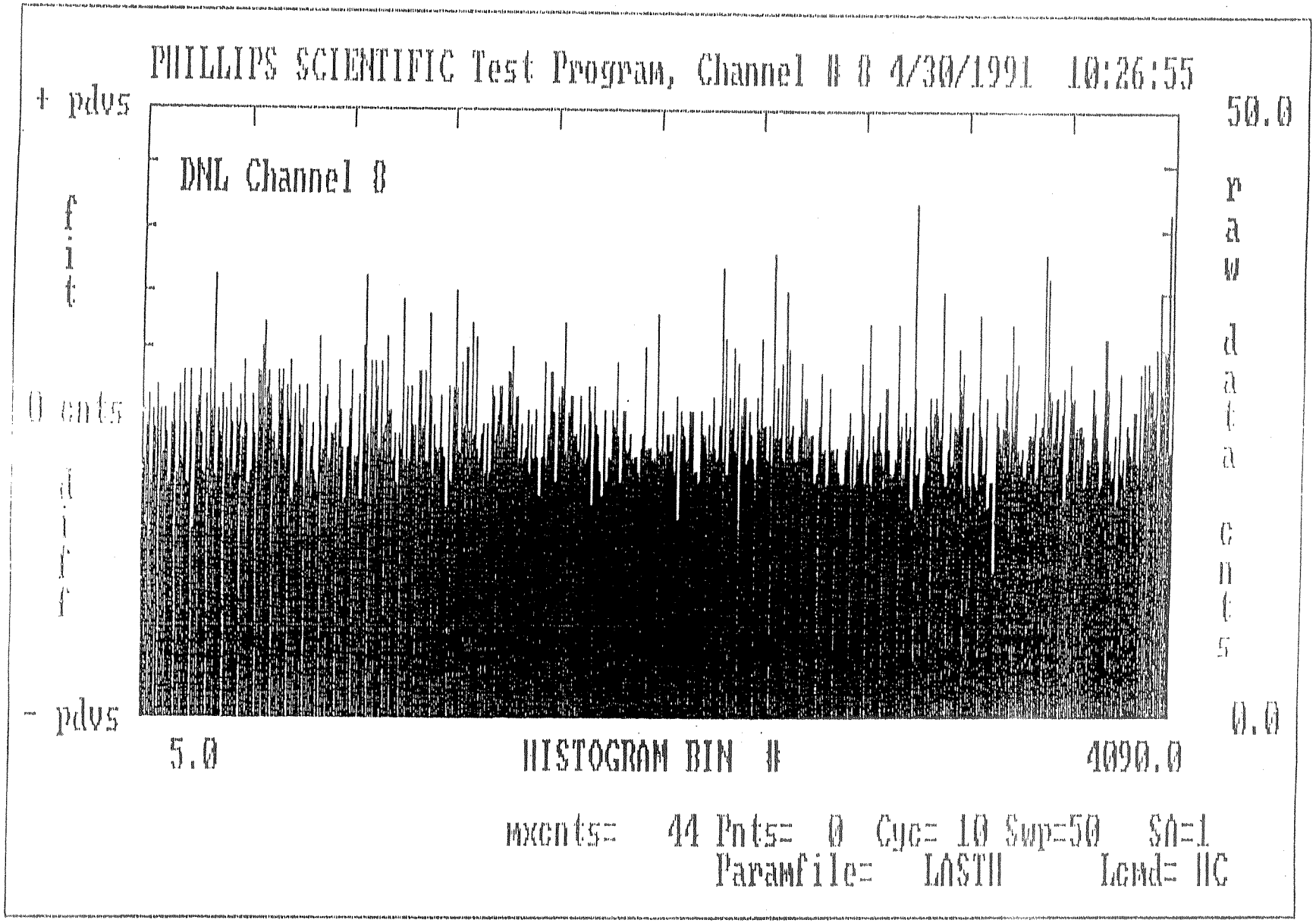
version: 12 September 1991: Clarify 7186 vs 7186H connections, CLEAR operation

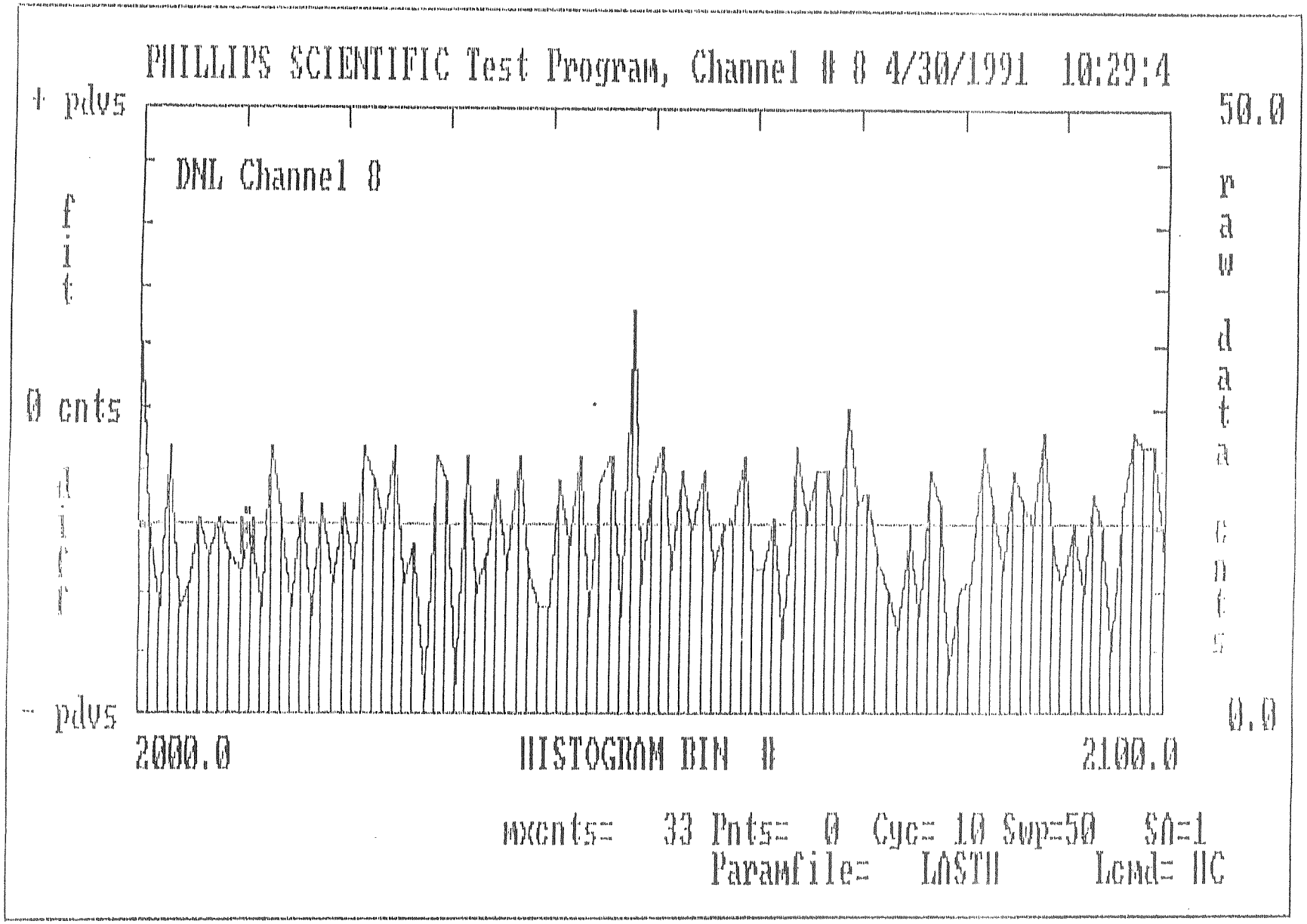

PHILLIPS SCIENTIFIC TDC Test Program Ch 1 7/26/1991 0:17:18
typical INL plot
25.0
raw - fit
0 cnts
-25.0
4095.0
raw data cnts
0.0
20.0
TIME INTERVAL(ns)
120.0
Ofst(cnts)=-799.6
Gain(ps/cnt)=25.020
mxcnts= 4000 Pnts=200 Cyc= 3 Swp= 1 SA=1
Paramfile= 7186100 Ped=0.0 ns

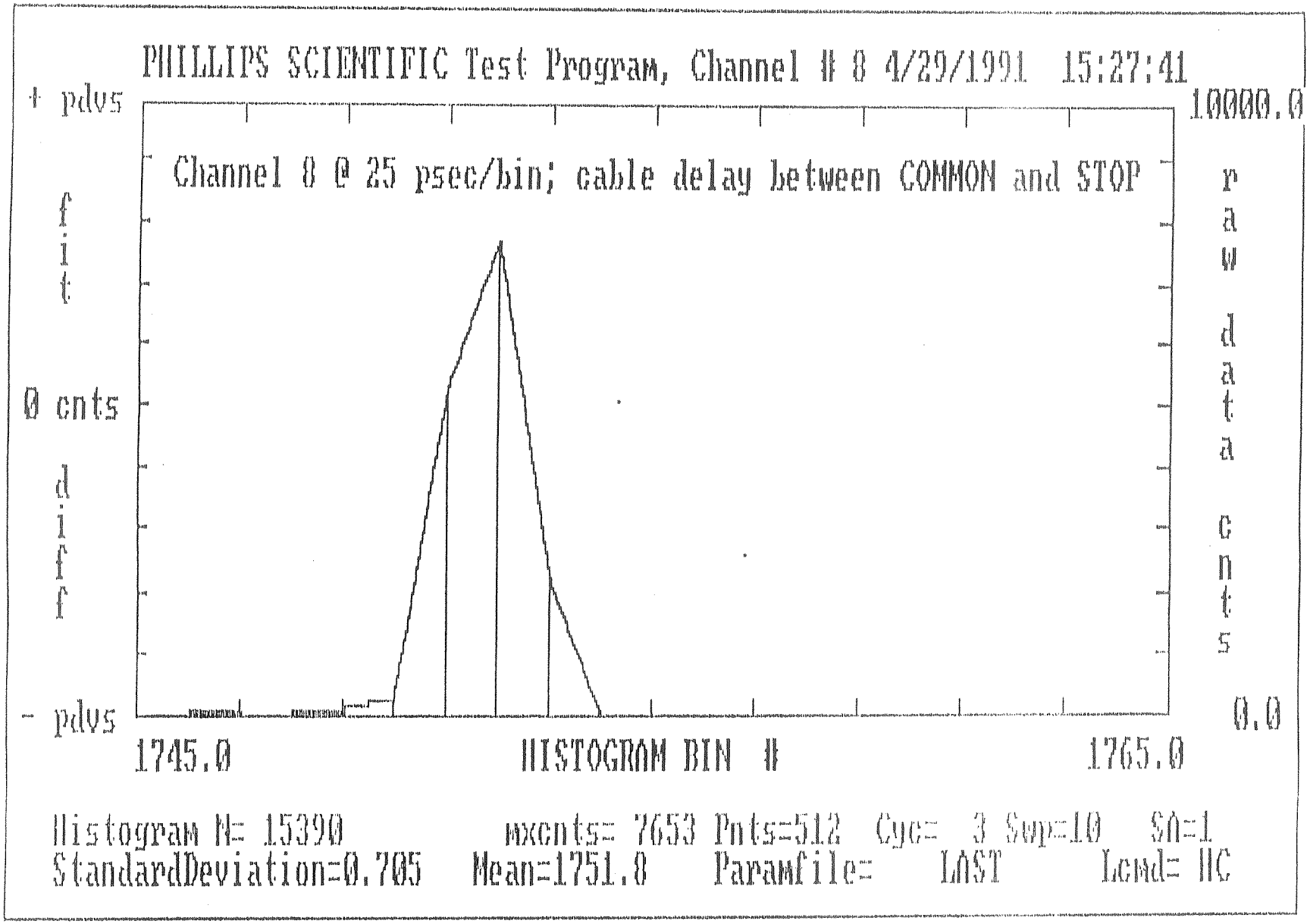

PHILLIPS SCIENTIFIC TDC Test Program Ch 1 7/26/1991 0:23:43
25.0
4095.0
typical INL plot
raw - fit
0 cnts
raw data cnts
0.0
-25.0
20.0
TIME INTERVAL(ns)
220.0
Ofst(cnts)=-531.6
Gain(ps/cnt)=49.909
mxcnts= 3883 Pnts=200 Cyc= 3 Swp= 1 SA=1
Paramfile= 7186200 Ped=0.0 ns


PHILLIPS SCIENTIFIC TDC Test Program Ch 1 7/26/1991 0:28:14
typical INL plot
25.0
raw - fit
0 cnts
-25.0
4095.0
raw data cnts
0.0
20.0
TIME INTERVAL(ns)
420.0
Ofst(cnts)= 390.2
Gain(ps/cnt)=100.060
mxcnts= 3812 Pnts=200 Cyc= 3 Swp= 1 SA=1
Paramfile= 7186400
Ped=0.0 ns


PHILLIPS SCIENTIFIC TDC Test Program Ch 16 7/26/1991 0:33:0
typical INL plot
25.0
4095.0
raw - fit
0 cnts
raw data cnts
-25.0
0.0
20.0
TIME INTERVAL(ns)
820.0
Ofst(cnts)=-343.6
Gain(ps/cnt)=199.073
mxcnts= 3781 Pnts=200 Cyc= 3 Swp= 1 SA=1
Paramfile= 7186800
Ped=0.0 ns


PHILLIPS SCIENTIFIC Test Program, Channel # 8 4/30/1991 10:26:55
+ pdvs
fit
0 cnts
diff
- pdvs
DNL Channel 8
50.0
raw data cnts
0.0
5.0
HISTOGRAM BIN #
4090.0
mxcnts= 44 Pnts= 0 Cyc= 10 Swp=50 SA=1
Paramfile= LASTH Lcmd= HC


PHILLIPS SCIENTIFIC Test Program, Channel # 8 4/30/1991 10:29:4
+ pdvs
fit
0 cnts
noise
- pdvs
50.0
raw data cnts
0.0
DNL Channel 8
2000.0
HISTOGRAM BIN #
2100.0
mxcnts= 33 Pnts= 0 Cyc= 10 Swp=50 SA=1
Paramfile= LASTU Lcmd= HC


PHILLIPS SCIENTIFIC Test Program, Channel # 8 4/29/1991 15:27:41
+ pdvs
fit
0 cnts
diff
- pdvs
10000.0
raw data cnts
0.0
Channel 8 @ 25 psec/bin; cable delay between COMMON and STOP
1745.0
HISTOGRAM BIN #
1765.0
Histogram N= 15390
mxcnts= 7653 Pnts=512 Cyc= 3 Sup=10 SN=1
StandardDeviation=0.705
Mean=1751.8
Paramfile= LAST
Lend= HC

MODEL 7186/7186H
16 CHANNEL CAMAC TDC
PROGRAMMING MANUAL

1 CAMAC DATAWAY OPERATIONS

1.1 Writing Data

F(16)·A(X): Write to data memory for channel (X+1).

1.2 Reading Data

F(0)·A(X): Read event data memory for Channel (X+1). Data word contains the data and the channel number.

F(4)·A(0): Read Sparse Data. Only those channels with data that falls between the upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false, X true.

1.3 Set the Control Register

F(19)·A(0)·D(X): Selectively enable the Pedestal, Upper and Lower Thresholds.

D1=1 Enable the Pedestals
D2=1 Enable the Lower Thresholds
D3=1 Enable the Upper Thresholds
D4 to D15 = 1 No Action

1.4 Reset the Control Register

F(23)·A(0)·D(X): Selectively disable the Pedestal, Upper and Lower Thresholds.

D1=1 Disable the Pedestals
D2=1 Disable the Lower Thresholds
D3=1 Disable the Upper Thresholds
D4 to D15 = 1 No Action

1.5 Read the Control Register

F(6)·A(0): Read the TDC control register. This tells which of the Pedestal, Upper Threshold or Lower Threshold are enabled, as well as the programming of the Processing Start Delay.

D16 D9	D8 D4	D3	D2	D1
MSB Delay Time LSB	00000	UT Enabled	LT Enabled	PED Enabled

Control Register Data Format

1.6 Read the Hit Register

F(6)·A(1): Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds. A 1 in any position indicates the channel has passed sparsification. For example, 0100001000001001 data on channels 1, 4, 10 and 15 have passed sparsification. These channels may be read using the sparse data read function (F4).

D16	D1
Channel 16	Channel1

Hit Register Data Format

1.7 Write the Parameter Memory

1.7.1 Select The Parameter

F(17)·A(0): Select the Pedestal Memory for the next F1 or F20 operation.

F(17)·A(1): Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)·A(2): Select the Upper Threshold Memory for the next F1 or F20 operation.

1.7.2 Write The Data

F(20)·A(X): Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation.

1.8 Read the Parameter Memory

1.8.1 Select The Parameter

F(17)·A(0): Select the Pedestal Memory for the next F1 or F20 operation.

F(17)·A(1): Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)·A(2): Select the Upper Threshold Memory for the next F1 or F20 operation.

1.8.2 Read The Data

F(1)·A(X): Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).

1.9 Test Functions

1.9.1 Run A Test From The Test Registers

1.9.1.1 Select a Pattern

1.9.1.1.1 Select The Test Registers

F(17)·A(4): Select the Test Register for the next F20 operation.

1.9.1.1.2 Select A Pattern

F(20)·A(X): Program the test register if it was selected by the most recent F17 operation.

X	Pattern
0	001001001001
1	010010010010
2	100100100100
3	111111111111

1.9.1.2 Run A Test

F(25)·A0: Digital test. Initiates a data acquisition cycle using the value stored in the test register by the most recent F20 command.

1.9.2 Run A 1/3 Or 2/3 Full Scale Test

F(25)·A1: Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)·A2: Initiates a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

1.10 LAM

F(24): Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(26): Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

F(8): Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(10): Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

1.11 Resets

F(9): Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(11)·A(0): Reset the Control Register. Occurs on S2 strobe.

F(11)·A(1): Reset the hit register. No effect on data memory. Occurs on S2 strobe.

F(11).A(2): Reset the test register. Occurs on S2 strobe.

F(11)·A(3): Reset the hit register and data memory. Occurs on S2 strobe.

2 CAMAC NON-DATAWAY COMMANDS

C, Z: Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the hit register. Occurs on the S2 strobe.

I: Inhibit all Camac Functions.

INDEX

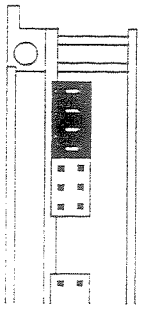
F(0)·A(X): Read event data memory., 1
F(10): Clear LAM., 4
F(11)·A(0): Reset the Control Register., 4
F(11)·A(1): Reset the hit register., 4
F(11)·A(2): Reset the test register., 4
F(11)·A(3): Reset hit register and data memory, 4
F(16)·A(X): Write to data memory., 1
F(17)·A(0): Select the Pedestal Memory., 2
F(17)·A(1): Select the Lower Threshold Memory., 2
F(17)·A(2): Select the Upper Threshold Memory., 2
F(17)·A(4): Select Test Register., 3
F(19)·A(0)·D(X): Selectively enable Parameters, 1
F(1)·A(X): Read parameter memory., 2
F(20)·A(X): Program the test register., 3
F(20)·A(X): Write the parameter memory., 2
F(23)·A(0)·D(X): Selectively disable Parameter, 1
F(24): Disable LAM., 3
F(25)·A0: Initiate digitization with test regist, 3
F(25)·A1: Initiate 1/3 full scale test., 3
F(25)·A2: Initiate 2/3 full scale test., 3
F(26): Enable LAM., 3
F(4)·A(0): Read Sparse Data., 1
F(6)·A(0): Read the TDC control register., 1
F(6)·A(1): Read the Hit Register., 2
F(8): Test LAM., 3
F(9): Clear the Module., 4

Version E: 12 September 1991: Added F11·A3 /hp

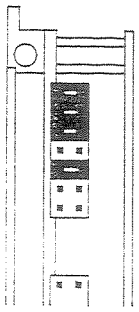
7186 JUMPER PROGRAMMING

ALL VIEWS ARE FROM TOP REAR OF MODULE.

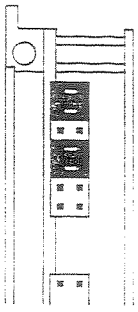
RANGE



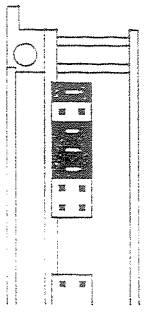
100 nsec



200 nsec

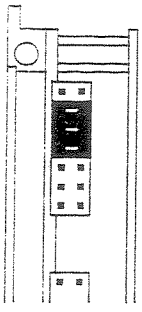


400 nsec

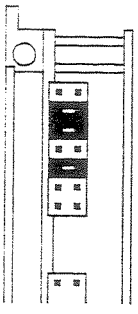


800 nsec

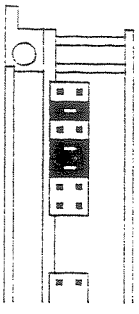
EXTENDED RANGE OPTION*



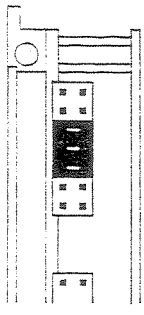
1 µsec



2 µsec



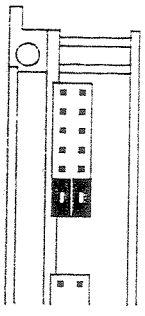
4 µsec



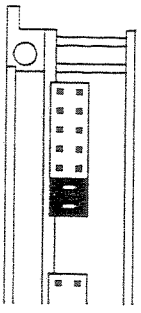
8 µsec

* THIS OPTION REQUIRES AN INTERNAL CAPACITOR VALUE CHANGE. CONSULT FACTORY FOR DETAILS.

COMMON START/STOP



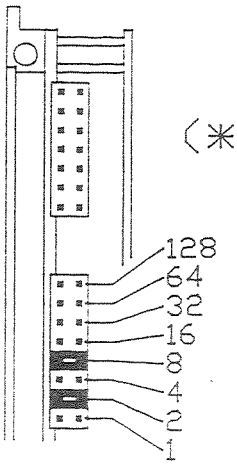
COMMON START



COMMON STOP

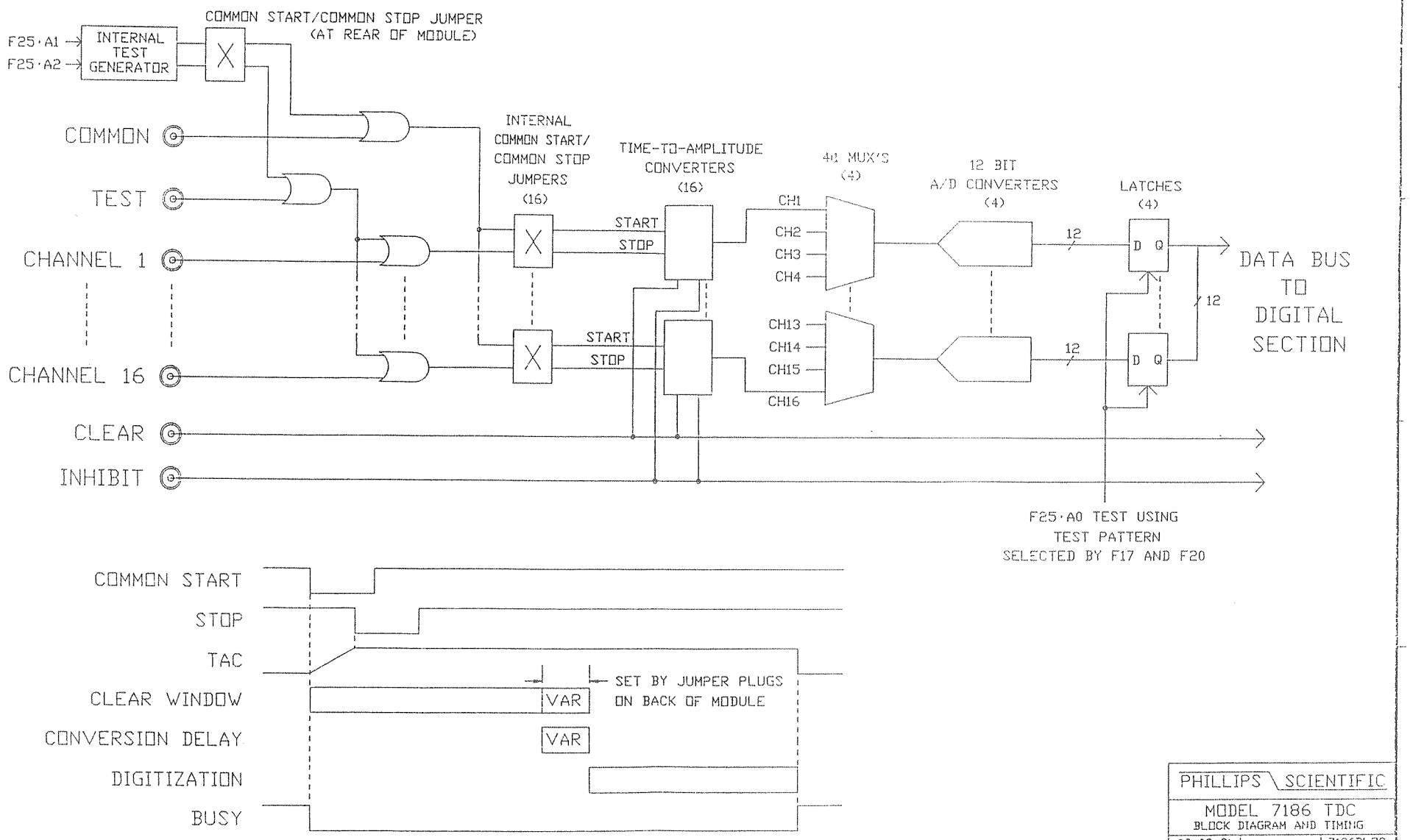
CHANNEL JUMPERS
J4 → J34
(EVEN #'S)

DELAY TIME MULTIPLIER



(*62.5 nsec)

625 nsec SHOWN



PHILLIPS SCIENTIFIC

MODEL 7186 TDC
BLOCK DIAGRAM AND TIMING

08-02-91		7186BLOC