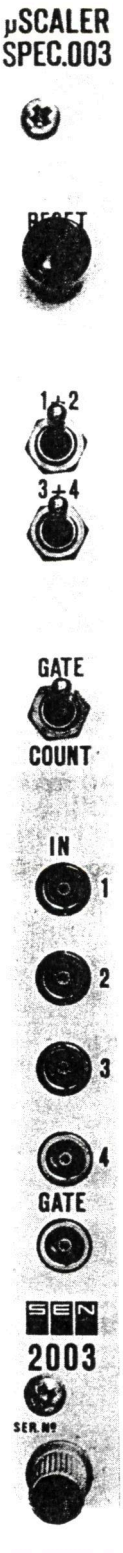
SEN
ELECTRONIQUE

CAMAC



4S 2003 FOUR-FOLD SCALER (CERN Spec's 003)

50 MHz and 100 MHz VERSIONS

The module contains four 16 bit scalers, each having an overflow flag to be tested by dataway commands. An L-request is produced whenever an overflow flag is on.

The two upper and the two lower scalers can be cascade connected in order to get two 32 bit scalers. Cascade connection is effected by front panel switches, which also disable the overflow flag of the first scaler in the cascade.

The four scalers share a common gate input, which can be made inoperative by a front panel switch. Reset is done either by a common push-button or by dataway commands. Dataway Clear is controlled by a switch on the back panel.

INPUT SPECIFICATIONS

Input (Scalers 1 to 4)

Scaling Speed :	50, 100 MHz minimum at 50% duty ratio
Reflexions :	⩽15% with a 1 ns, 18 mA pulse edge
Impedance :	50 ohms
Input Thresholds :	"0" : – 4 to + 20 mA "1" : – 12 to – 36 mA
Minimum Pulse Width :	3 ns at – 12 mA, nearly square pulse of – 13 mA peak amplitude.
Slowest Rise Time :	No limit, DC coupling

Gate

Whenever applicable, specifications as for **Input**, except pulse width : 5 ns at – 12 mA, nearly square pulse of – 13 mA peak amplitude.

Maximum Delay : ⩽3 ns

This Four-Fold Scaler has been designed to insure compatibility with other products built in accordance to the "Microscaler Type 003, CERN–NP CAMAC Note 16–00, Feb. 1970"

1211 GENÈVE 13 - SUISSE/SWITZERLAND - 31, Av. Ernest-Pictet - Tél. (022) 44 29 40 - Télex 23359 - Câbles SENELECTRON

100 MHz Scalers

Differences of characteristics to the 50 MHz Scaler are as follows :

Scaling Speed :	100 MHz minimum	
Power Requirements :	+ 6 V ≃ 900 mA	−6 V ≃ 570 mA

The circuit diagram is identical to the 50 MHz Scaler. Scaling Speed is improved by replacing MC 1013P IC's no. 11, 12, 13 and 14 by Type MC1027, whereas SN 7474 N no. 19, 20, 21 and 22 are replaced by SN 74H74 N IC's.

DATAWAY COMMANDS TO THE 4 S 2003

(FCT ff, SAD a = Function ff, Sub-address a)

The scalers of the 4 S 2003 are labelled according to the above mentioned CERN note. Scaler 1 is addressed by SAD 0, scaler 2 by SAD 1 etc.

FCT 0, SAD 0 to 3 :	Read the addressed scaler on R1 to R16
FCT 2, SAD 0 to 3 :	Read and Clear the addressed scaler
T 6, SAD 0 :	Read the Module Identification Code (this function puts a "1" on R3, R7 and R8
FCT 8, SAD 0 to 3 :	Test the addressed overflow flag
FCT 9, SAD 0 to 3 :	Clear the addressed scaler
FCT 10, SAD 0 to 3 :	Test and Clear the addressed overflow flag, see note 1 below.
FCT 25, SAD 0 :	Increment the 4 scalers

Non-addressed Commands :

Inhibit (I) :	Inhibit scaling action, do not block FCT 25
Clear (C) :	Reset the 4 scalers and the 4 overflow flags if rear panel switch is on YES.
Initialize (Z) :	Reset the 4 scalers and the 4 overflow flags

NOTES :
1. The test action in FCT 10 is not allowed by the CERN specifications, contrary to the CAMAC report EUR 4100 e, page 15. Thus, Q can be disconnected by removing a jumper.
2. All functions except 8 and 10, always produce a Q-response. Functions 8 and 10, of course, produce a Q only if the overflow flag is on.

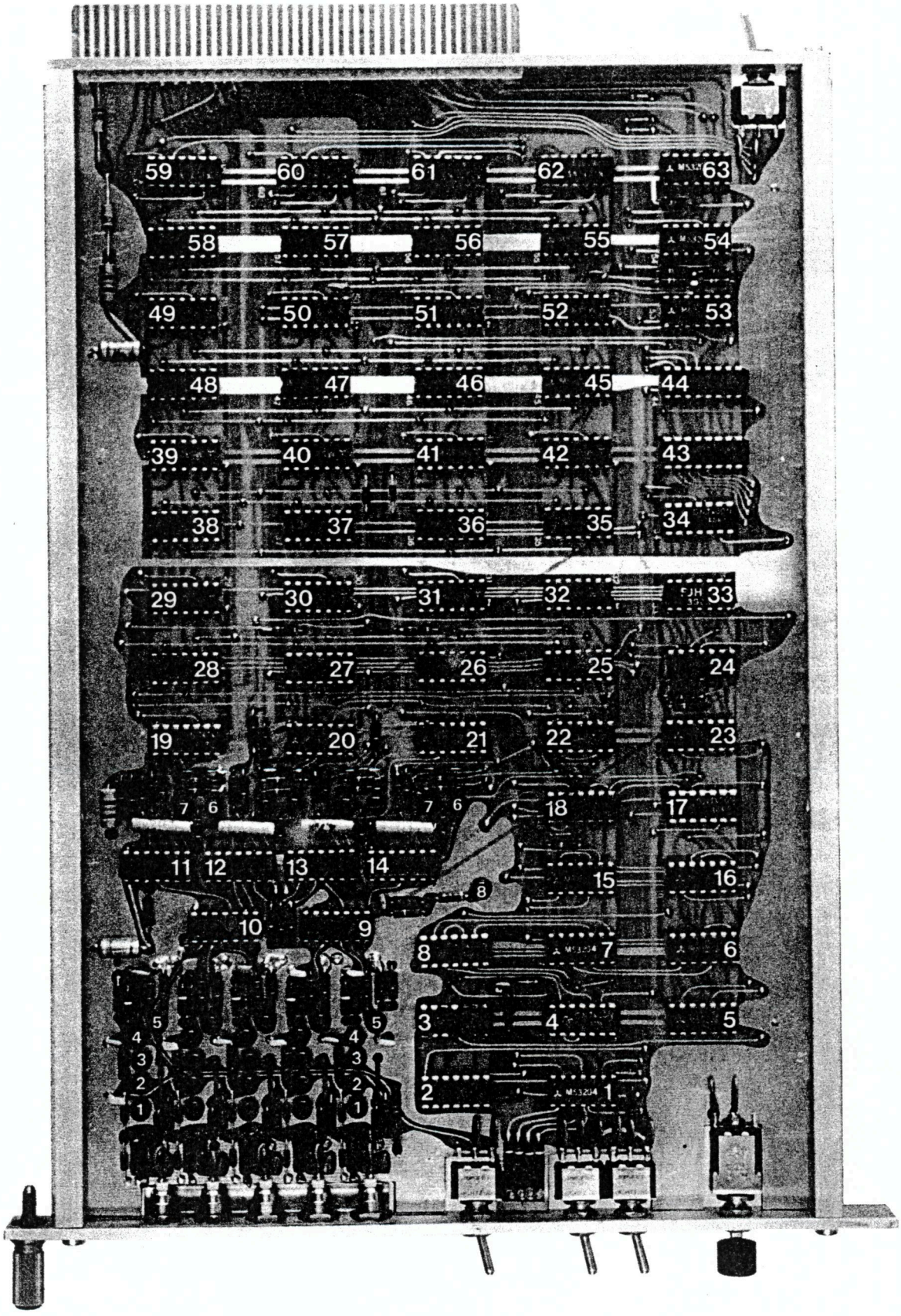
PHYSICAL

Single width CAMAC module with shielding covers on both sides. Fiber-glass circuit board with plated-through holes.

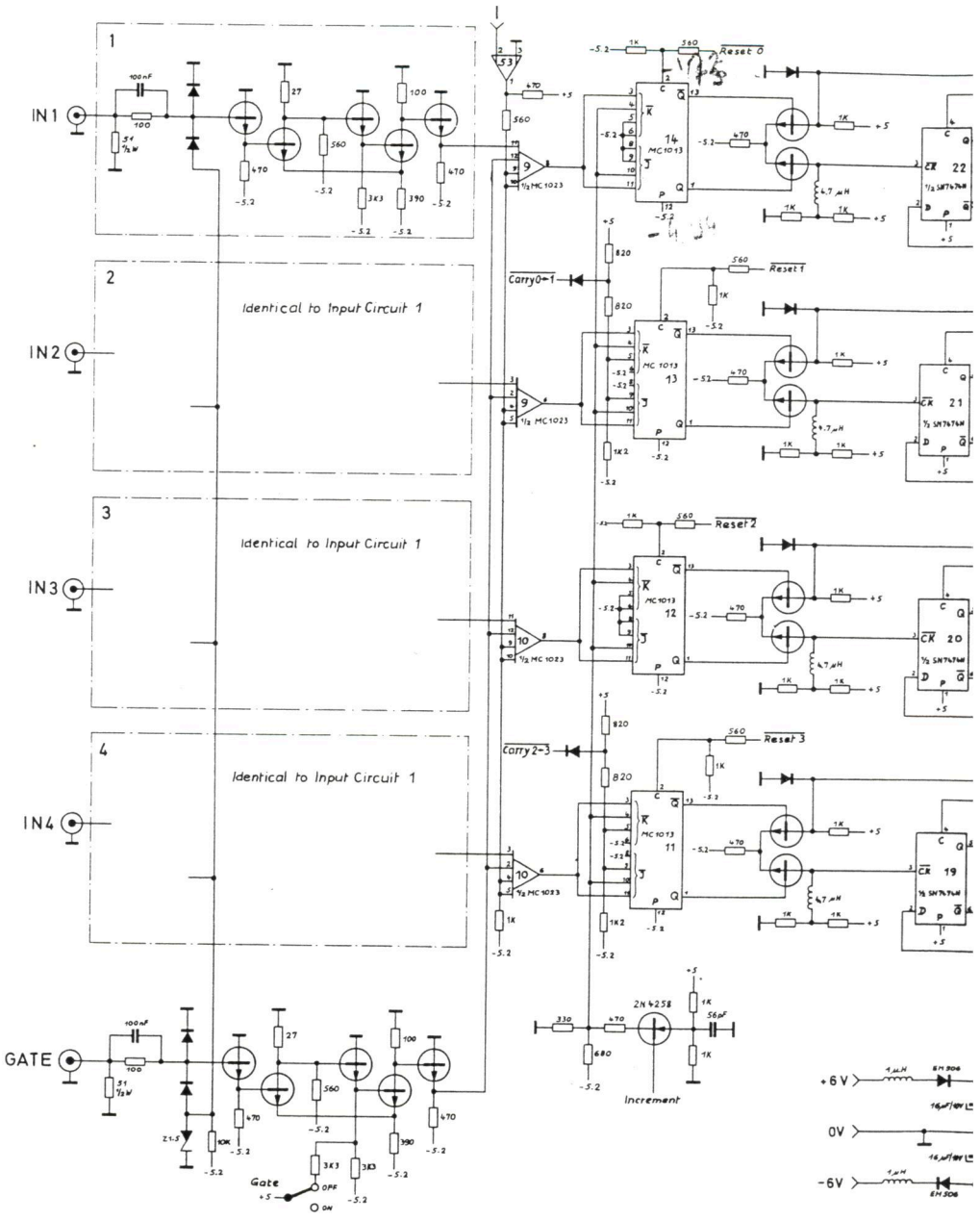
MECL and TTL integrated circuits for speed and dependability.
Meets all electrical and mechanical specifications of EUR 4100 e report.

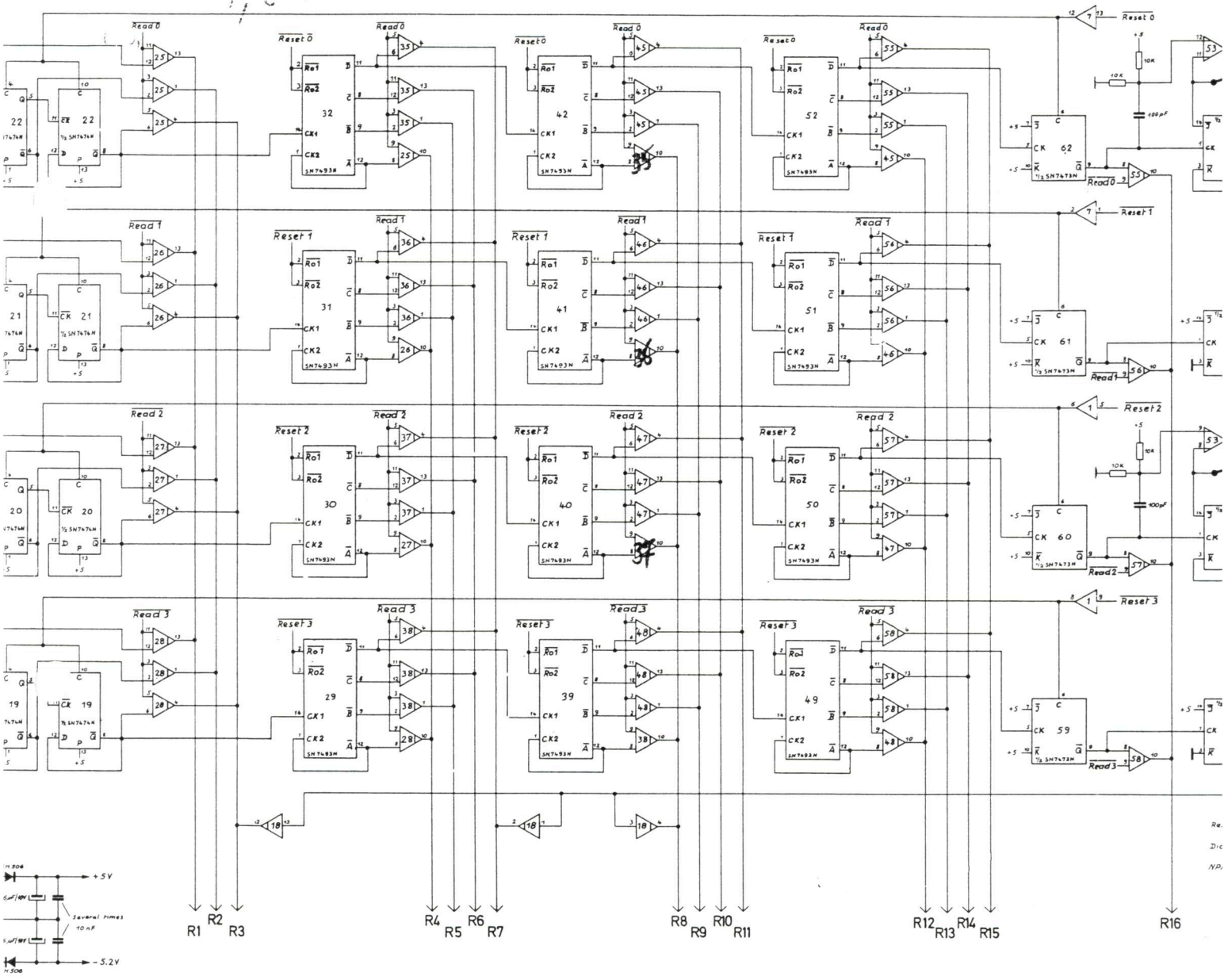
POWER REQUIREMENTS

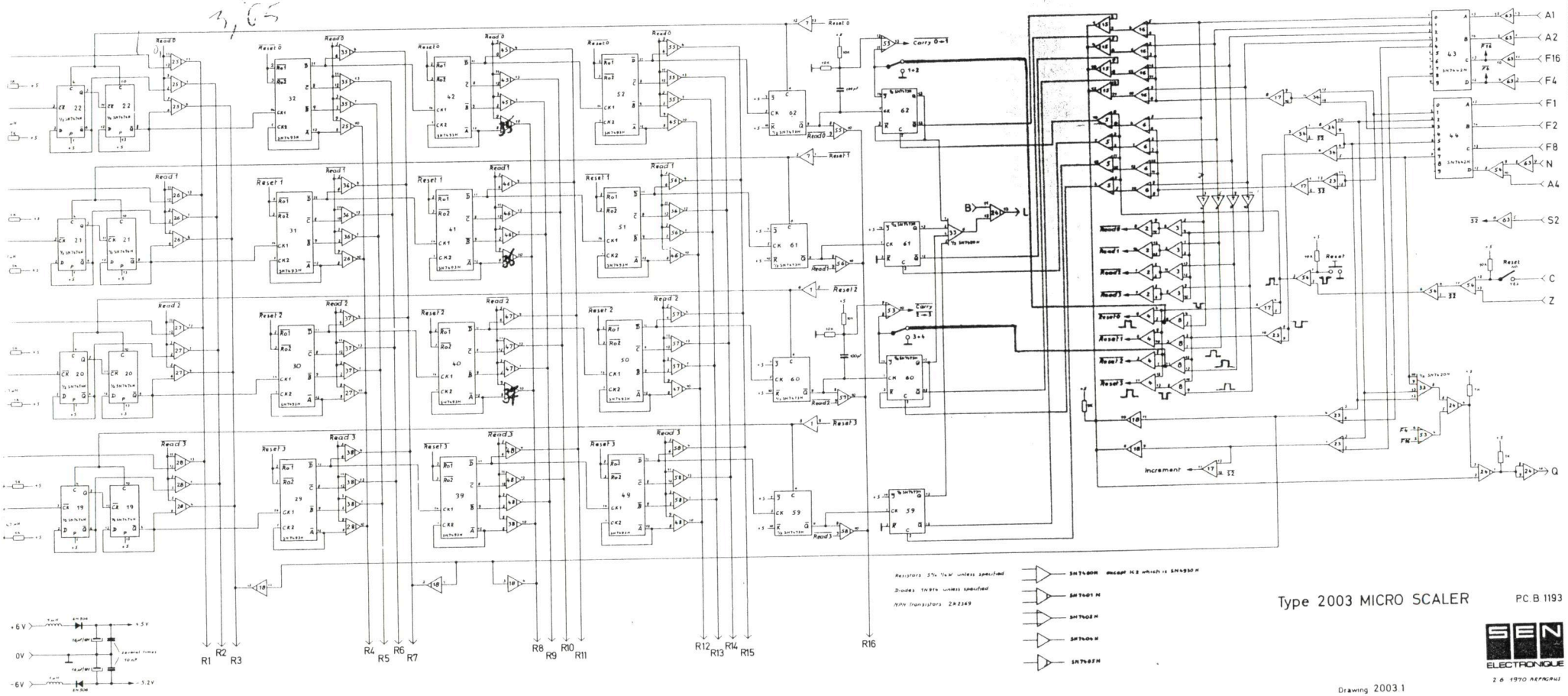
+ 6 V	~ 850 mA
– 6 V	~ 450 mA



TYPE 2003 Component Location


IN1
IN2
IN3
IN4
GATE
1
2
3
4
Identical to Input Circuit 1
Identical to Input Circuit 1
Identical to Input Circuit 1
Carry0→1
Carry 2→3
Reset 0
Reset 1
Reset 2
Reset 3
MC 1013
MC 1023
SN7474N
2N4258
Increment
Gate
OFF
ON
+6V
0V
-6V
EM 206


Read 0
Reset 0
Read 1
Reset 1
Read 2
Reset 2
Read 3
Reset 3
SN7493N
SN7473N
SN7474N
+5
10K
100pF
Several times
10 nF
+5.5V
-5.2V
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16



Resistors 5% ¼W unless specified

Diodes 1N914 unless specified

NPN transistors 2N3569

SN74S00N except IC3 which is SN74S30N

SN74S01N

SN74S02N

SN74S04N

SN74S74N

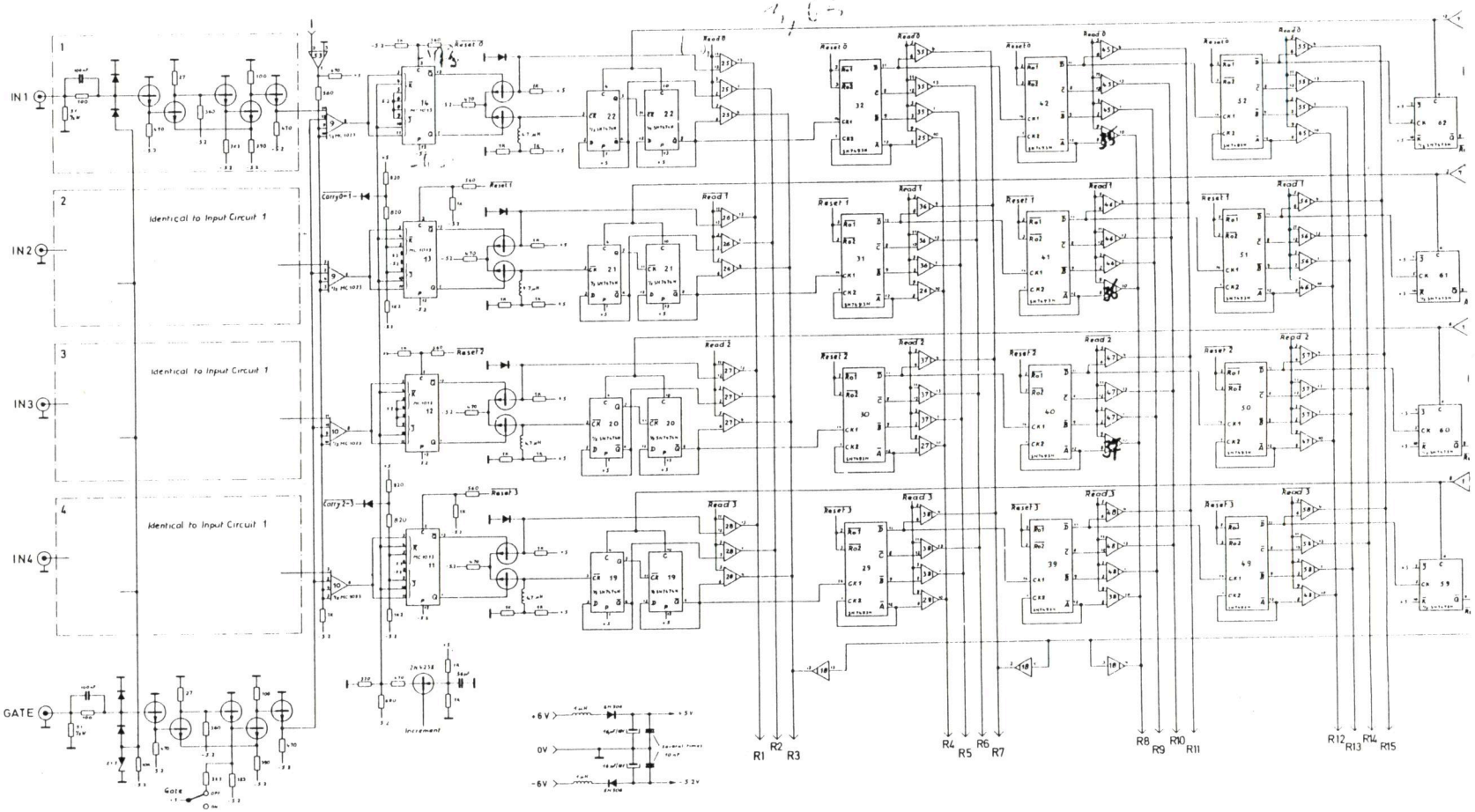
Type 2003 MICRO SCALER

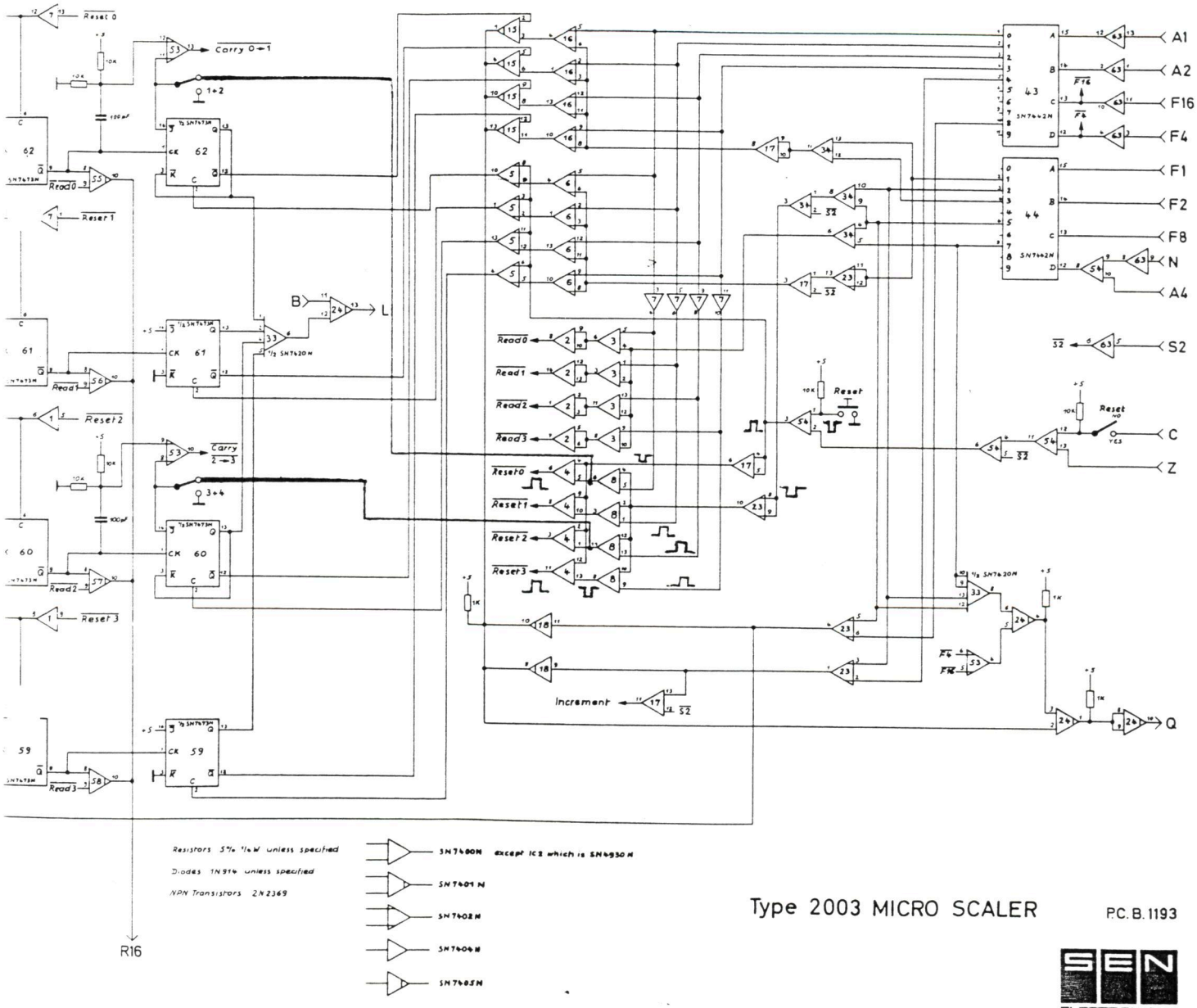
PC.B 1193

SEN ELECTRONIQUE

26 1970 AEPIGNUS

Drawing 2003.1


IN1
IN2
IN3
IN4
GATE
Identical to Input Circuit 1
Identical to Input Circuit 1
Identical to Input Circuit 1
Carry0→1
Carry1→2
Carry2→3
Reset 0
Reset 1
Reset 2
Reset 3
Read 0
Read 1
Read 2
Read 3
Increment
+6 V
0V
-6V
+5V
-5.2V
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15



Type 2003 MICRO SCALER

P.C.B. 1193

SEN ELECTRONIQUE

26 1970 ARPAJON

Drawing 2003.1

CERN-NP CAMAC Note 16 - 0(
Feb. 197(

MICROSCALER

TYPE 003

ELECTRONICS II

F. Iselin, A. Lang, B.A. Löfstedt, A. Maurer, O.P. Nicolaysen, A. Orêve, Ph. Ponting, R. Rivollet, J.P. Vanuxem

SIS/R/16596

MICROSCALER - TYPE 003

1. INTRODUCTION

1.1 General

The CAMAC system proposed (Rome 1968) by quite a large number of laboratories and institutes (including CERN) is a system well adapted to electronics for data handling. It will be used in CERN-NP in the field of "electronics" or "counter" experiments.

The basic documents to work with on CAMAC are the

- CAMAC ESONE report
- Euratom EUR report No. 4100.

All units to be described, as well as the logic systems, must follow the CAMAC compatibility rules as noted in these two fully-equivalent documents (EUR 4100 being a final document appearing after the ESONE report), and also the CERN-NP CAMAC options (Leaflet 1-00).

1.2 CERN-NP CAMAC Notes

The CERN-NP CAMAC notes are intended to give an up-to-date picture of what is currently being done, and what is preferred or requested by CERN-NP in this field. This information is tentative and is meant to improve contracts with laboratories, industry, and colleagues in an informal and simplified way, since experience has shown that it is extremely difficult to provide complete detailed information with the necessary time limits. Most of the CAMAC "leaflets" (or "notes") will be devoted to particular plug-in units, and very often this will be the basis for tenders. The descriptions will therefore contain sufficient indications to allow for the correct design of the unit. The information will also be such that interchangeability of plug-in units, made according to the specifications, is guaranteed. This interchangeability is a very important feature for useful contacts with other laboratories.

All CAMAC rules must, of course, be followed, as well as CERN options; therefore only information pertinent to the described module shall be given.

2. DESCRIPTION OF THE UNIT

This "Microscaler" type 003 is one unit wide and contains four 16-bit 25 MHz scalers without any display. It has a common input gate, a possibility to have two sequential words [A(0) with A(1), A(2) with A(3)], and various CAMAC features, such as overflow alarms (LAM) and increment.

The 003-type is intended for use when high degree of compactness is required.

3. FRONT PANEL

3.1 Reset button

It resets the four scalers and their overflows.

3.2 Serializing switches (1,2 and 3,4)

These make it possible to put in series scaler 1 with scaler 2, and scaler 3 with scaler 4, in order to obtain two 32-bit scalers. These switches also suppress the overflow action (L) of the first scaler when two scalers are in series.

3.3 Count/Gate switch

It sets the gate on "always open" (COUNT) or on its normal position (GATE), and this simultaneously for the four scalers.

3.4 Input (1, 2, 3, 4)

One input per scaler.

Speed of counting:	≥25 MHz with worst case signals, temperature and elements.
Input impedance:	50 Ω.
Reflexion:	<|±15%| on a 1 nsec (10% - 90%) rise- or fall-time of a -18 mA pulse.
Slowest rise-fall times:	∞ (direct coupling) recommended.

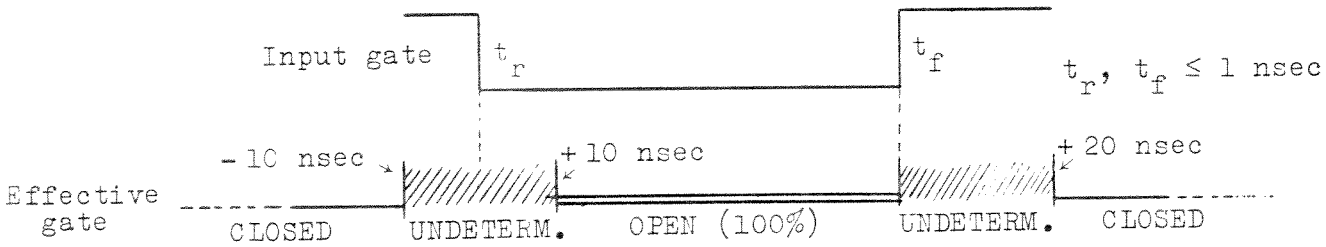
Duty ratio:	Max 50% in worst case conditions at 25 MHz.
Sensitivity:	ESONE - CAMAC "0" (-4 to +20 mA) "1" (-12 to -36 mA).
Minimum pulse:	4 nsec at -4 mA and 3 nsec at -12 mA (max peak -13 mA) in worst case conditions at max speed.

3.5 Gate

One input for the four scalers

ESONE - CAMAC current level specifications as for Inputs.

Cate delay:



OPENING:	Delay measured between the leading edges at - 12 mA gate level and input level.
CLOSING:	Delay measured between the trailing edges at -4 mA gate level and input level.

Within this specification the effective gate must not be longer than the input gate +25 nsec (+15 nsec recommended).

Minimum pulse:	11 nsec at -4 mA and 10 nsec at -12 mA (max peak -13 mA) in worst case conditions at max speed.

The recovery time must not be longer than 40 nsec after the input gate closing.

4. CAMAC FUNCTIONS

4.1 Functions used in this unit

Read Group 1 Registers	F(0)
Read and Clear Group 1 Registers	F(2)
Read module characteristic	F(6)
Test Look at me	F(8)
Clear Group 1 Registers	F(9)
Clear Look at me	F(10)
Increment Preselected Registers	F(25)

Functions are coded (0 to 31) on the five function lines.

N is the module address (direct on-line selection).

A is the word sub-address from the four A lines:

A(0)	for scaler	1
A(1)	"	" 2
A(2)	"	" 3
A(3)	"	" 4

4.2 Various "Reset"

Clear. S2 conditioned by the Rear Reset Switch (YES/NO)	→	General non-addressable Reset in the whole module.
Manual Reset	→	General Reset in the module.
$[F(2) + F(9)] \cdot N \cdot S2 \cdot A$	→	Reset Group 1 Registers (and not overflows) in function of A.
$F(10) \cdot N \cdot S2 \cdot A$	→	Reset overflows only in function of A.

4.3 Response

All the functions foreseen in this unit give always Q = "1" (with N and A) except F(10), but $F(8) \cdot N \cdot A(x) \cdot OVF_x \rightarrow Q$ = "1". F(10) is not used to test the LAM before S2 in this particular case because a LAM could appear between S1 and S2 and would be lost. Therefore F(10) does not generate Q = "1" and is only used to clear the LAM source in S2.

The action of the first scaler overflow must be suppressed when two are in series.

4.4 Read module characteristic

F(6)·N·A(0) → 003/04 ("1" on Read lines R3, R5, R6).

The presentation of the characteristic has to remain in accordance with the provisory specification.

4.5 Increment preselected registers

F(25)·N·A(0)·S2 → Add ONE in the four scalers simultaneously.
Max. freq. : 2 MHz.

5. REMARKS

5.1 Busy

$\overline{\text{Busy}}$·LAM source → "1" on L line (LAM).

5.2 Inhibit

$\overline{\text{Inhibit}}$·Input 1,2,3,4 → COUNTING

Inhibit must not block Increment action [F(25)].

5.3 A(0)

In 4.4 and 4.5, A(0) is not mandatory because these two functions do not use different sub-addresses.

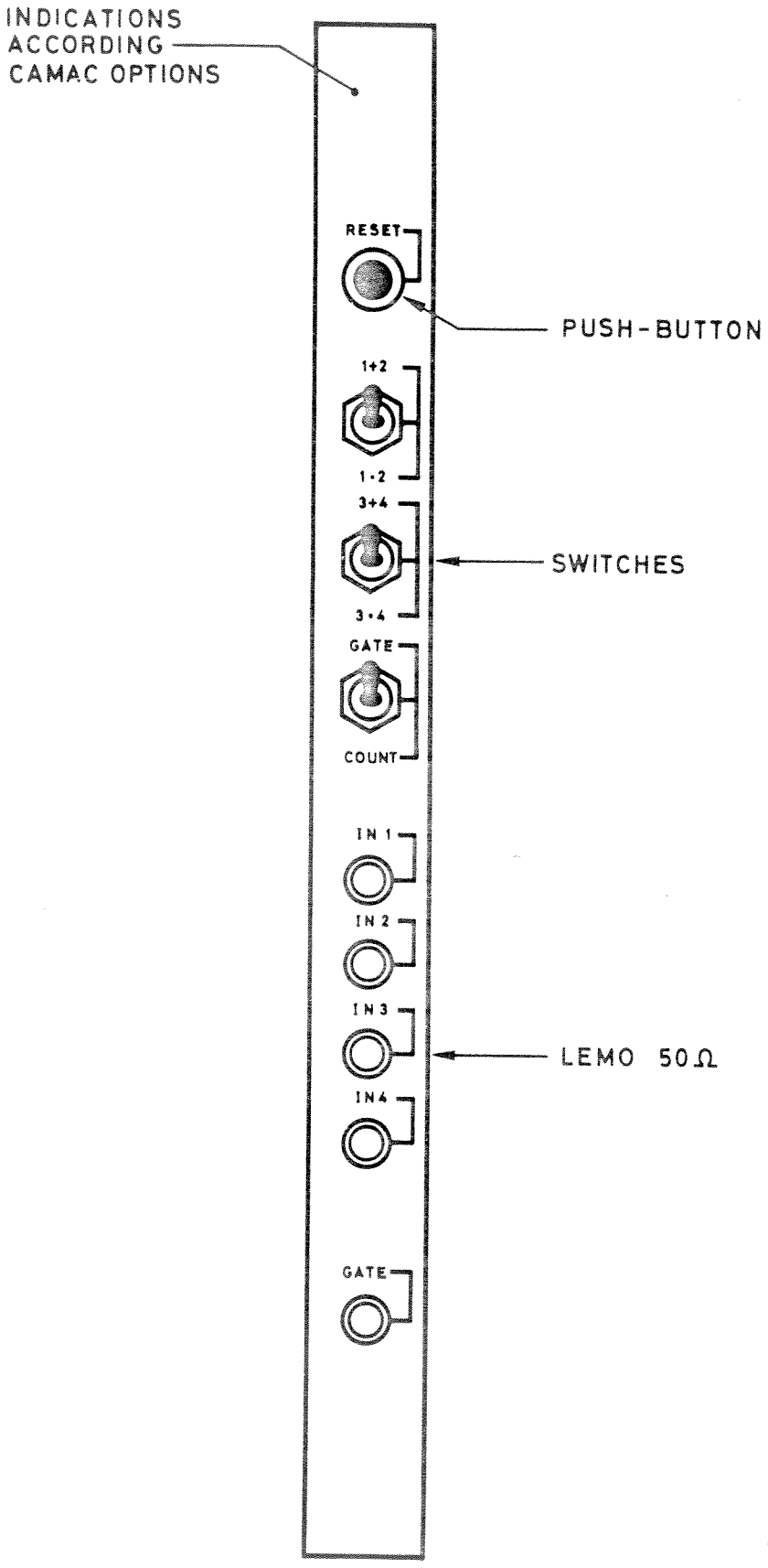
5.4 Read-out delay

The delay between

Beginning Read - Data ON
and also End Read - Data OFF

must not be longer than 250 nsec in the worst case conditions (loading equivalent to 23 identical units).

See Figs. 9 and 7.1.1, 7.1.2 on EUR 4100e report.



Scale 1/1

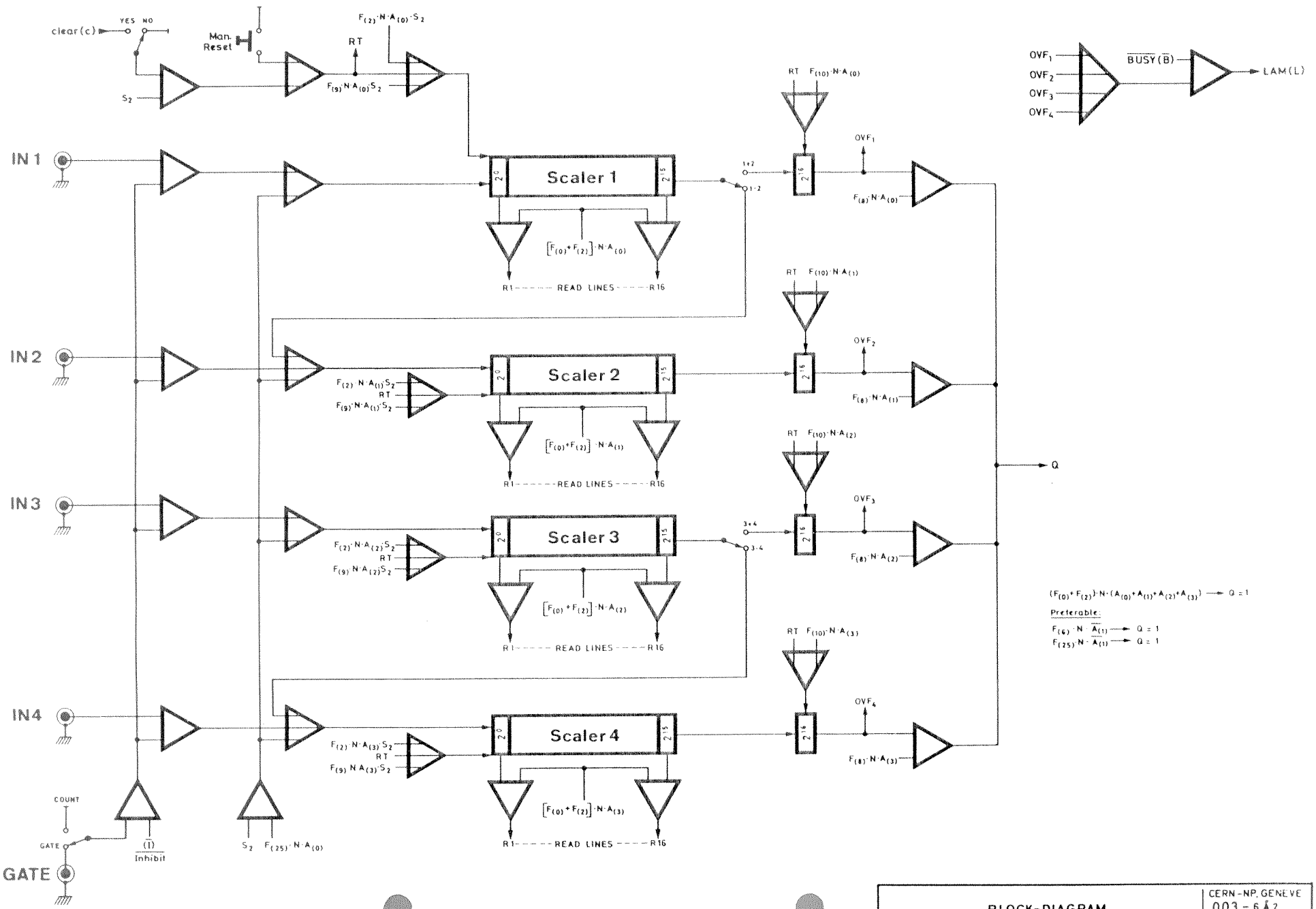
FRONT PANEL (typical)

MICROSCALER-TYPE: 003

CERN - NP, GENEVE

003 - 3A 4

17. 2. 70 Schmall



BLOCK-DIAGRAM
MICROSCALER-TYPE:003

CERN-NP, GENEVE
003 – 6 Å 2
21.1.70 Schwarz

A D D E N D A

1. Initialize (Z) must be introduced in this module.
   In accordance with par. 5.5.1 on EUR 4100e report, $(Z.S_2)$ resets all data registers and LAM sources.
   In this case it is identical to $(C.S_2)$

2. In 4.2

   The clear action must be conditioned by the Rear Reset Switch.

3. In 4.4

   In accordance with para. 5.7 of the CAMAC OPTIONS Note 1-00, December 1968.

   Read module characteristic → 003/04 ("1" on Read lines R3, R7, R8)

4. In Block diagram

   F(10) . N . S2 . A(o) clears the LAM source of scaler 1
   F(10) . N . S2 . A(1) " " " " " scaler 2
   F(10) . N . S2 . A(2) " " " " " scaler 3
   F(10) . N . S2 . A(3) " " " " " scaler 4