TDC

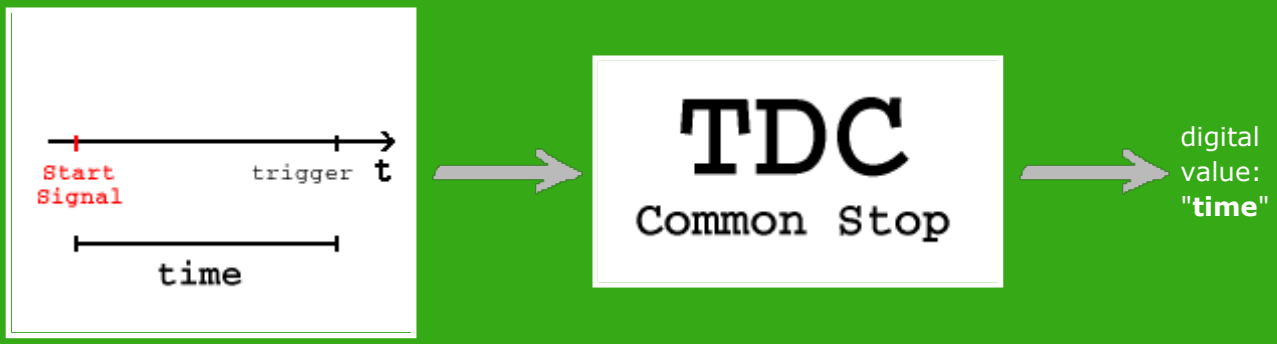
Time Digital Converter

Model: **Silena 9418/6-T32** (standard V430)

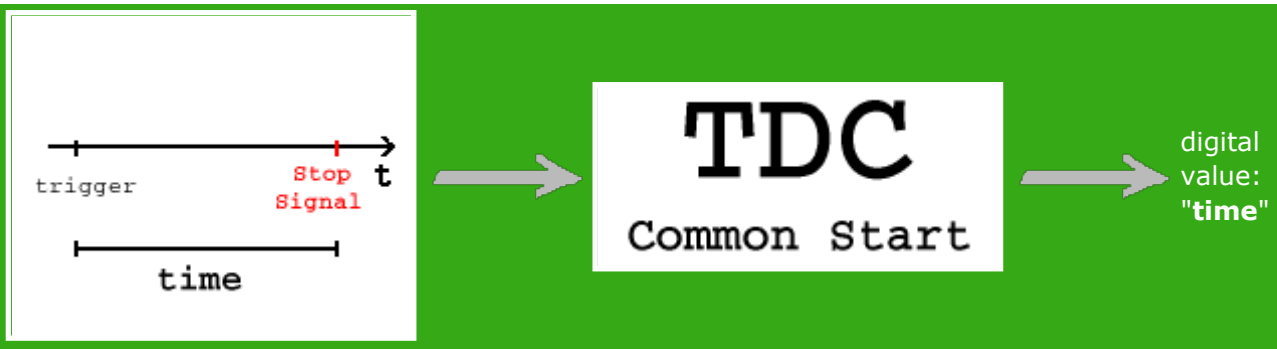
Resolution	12 bit (< 50 pico-sec)
Number of channel	32 input channels on a single-width VME module
Conversion Time	15 micro-sec for all 32 channels
Time Resolution	< 50 pico-sec
Differential Non-Linearity	< 2% on 95% of the dynamic range
Integral Non-Linearity	< 0.1%
Spectroscopy Grade Performance	< 2% DNL
Low Level Threshold	from 0 to 50% of the full scale (8 bit) individual for each channel
other	Common Start and Common Stop operation
	Programmable full scale (2 bit): 200, 400, 800, 1000 nano-sec
	Input 32 channels ECL standard on two 34 pin header connectors
	1 Common Start/Stop differential ECL input
	1 ECL gate differential input
	One unit 6U VME V430 CERN backplane compatible
	Zero Suppression and skip of channels with value < LLD (sparse mode)
	Multiplicity output one, on front panel LEMO connector

This module is fully compatible with the **FAIR bus** and **VME bus**.

How the TDC works in **Common Start** Mode:



How the TDC works in **Common Stop** Mode:



Functional Description

Programmable features
All main function of this module are software programmable, such a Full Scale Time and Low Level Threshold.
A full functionality test of the board can be executed by the self-test mode. The module can work either in common start or common stop mode.

Readout
This module (and all the 9418/6 series) can be read through two different bus systems, VME or FAIR, selected through a jumper on the module board.

FAIR Readout
The 9418/6 Series Modules can be read through a serial dedicated readout bus, the FAIR, using the 64 pins User defined on the VME P2 connector, and operated via a dedicated crate controller, loading the ADC and TDC data in a local memory.

VME Readout
The 9418/6 Series Modules can be read (optionally) through a VME standard bus, using a VME V430 CERN standard back plane, and either a CPU located in the Master Crate and reading all front-end modules, or multiple CPUs located in each Slave Crate and reading all modules.

Output Data Format (FAIR mode)

The output is a longword (32 bit) for each channel (whose value is over the custom threshold) with the following format:

Data word

bit	31	30	29...26	25...20	19...13	12.....0
meaning	0	PAR	X	DWN	X	Data

When the module has written all data word it write also a footer word:

Footer word

bit	31	30	29...26	25...22	21...16	15.....0
meaning	1	PAR	EC	X	VDW	VSN

PAR Parity bit a bit for the parity control 1bit

DWN	Data Word Number (or sub address)	is the VSN's channel that was touched	5bit
Data	Data	the data	12bit
EC	Event Counter	used only for debugging purpose	4bit
X	Don't Care	not used	4bit
VDW	Valid Data Word	how many valid data words preceed the footer word	6bit
VSN	Virtual Station Number	a given number that identify the module	16bit

Model 9418/6-T 32 Channels Spectroscopy TDC (stand. V430)

The model 9418/6-T is a single-width VME module with a high-resolution analog-to-digital converter, excellent integral non-differential linearity performance, fast conversion time and unique full programmable features.

The 9418/6-T is a multi-time to voltage converter (TAC) circuit connected to a high speed conversion module, allowing storage of up to 32 simultaneous pulses that are converted in a fast sequence. The TACs are mounted on a separate PCB on the VME motherboard.

The TDC has 12-bit resolution with a conversion time of 10 µs for all channels. This is obtained using a fast 12-bit ADC, coupled to a 32 channel multiplexer. The data are then sent to a FIFO memory after the zero suppression stage. A sliding scale compensation technique has been implemented on the 9418/6-T to improve the differential linearity.

- Fast Conversion: 10 µs for all 32 Channels
- 12 – Bit Resolution
- 32 Input channels on a Single – Width VME Module
- Spectroscopy Grade Performance: <2% DNL
- One unit 6U VME V430 CERN Backplane compatible, zero Suppression and Skip of Channels with Value <LLD (sparse mode).
- Common Start/Stop Operation
- Inputs 32 channels ECL standard on two 34 pin header connectors; 1 Common Start/Stop differential ECL input; 1 ECL gate differential input ECL
- Resolution 12 bit
- Differential Non-Linearity < 2% on 95% of the dynamic range
- Integral Non-Linearity < 0,1%
- Conversion Time 10 ms for all 32 channels
- Low Level Threshold from 0 to 50% of the full scale (8 bit) individual for each channel
- Programmable Full Scale (2 bit): 200, 400, 800 and 1000 ns
- Time Resolution < 50 ps for the minimum full scale
- Multiplicity output one, on front panel LEMO connector.

Output Data Format

- Header Word indicates the module address within the VME crate (Virtual Station Number), the data number and the event counter
- The data conversion number and the input channel number
- The event end marker

FUNCTIONAL DESCRIPTION

Programmable features
All main functions of the 9418/6-T, such a Full Scale Time and Low Level Threshold, are software programmable with a resolution of 2 and 8 bits respectively. A full functionality test of the board can be executed by the self-test mode. The module can work either in common start or common stop mode.

Readout
The 9418/6 Series Modules can be read through two different bus systems, either VME or FAIR*, selected through a jumper on the module board.

VME Readout
The 9418/6 Series Modules can be read through a VME standard bus, using a VME V430 CERN standard backplane, and either a CPU located in the Master Crate and reading all front-end modules, or multiple CPUs located in each Slave Crate and reading all modules.

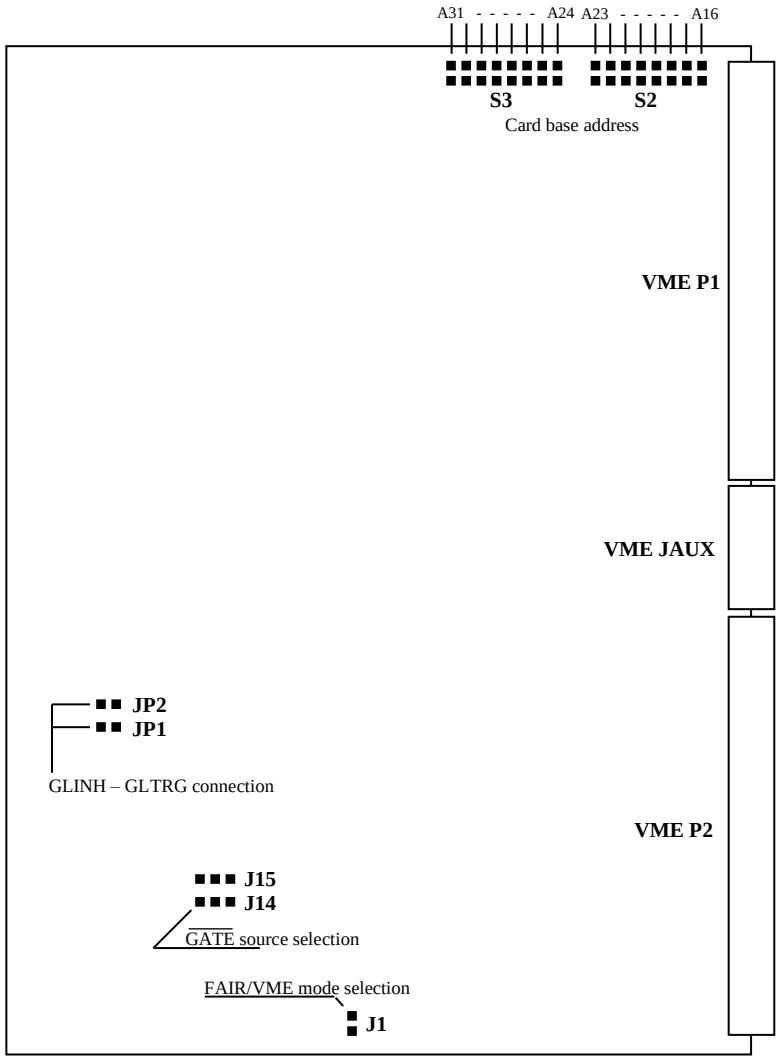
FAIR Interface

The 9418/6 Series Modules can be read (optionally) through a serial dedicated readout bus, the FAIR, using the 64 pins User Defined on the VME P2 connector, and operated via a dedicated crate controller, loading the ADC and TDC data in a local memory.

*FAIR is a Fast Inter-crate Readout designed by the Naples Section of the Italian National Institute of Nuclear Physics.

Silena 9418 headers description

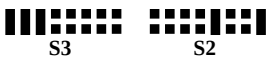
Headers position
(component side view)



Base address configuration (S2, S3)

S2 selects the module base address in VME Standard space
S2-S3 select the module base address in VME Extended space.
A jumped (close) header means "0" and an open header is "1".

Example:



	ADDR	*jumper*	*BIN*	*HEX*		*ADDR*	*jumper*	*BIN*	*HEX*
S3	A31	close	0	1	**S2**	A23	open	1	F
	A30	close	0			A22	open	1	
	A29	close	0			A21	open	1	
	A28	open	1			A20	open	1	
	A27	open	1	F		A19	close	0	6
	A26	open	1			A18	open	1	
	A25	open	1			A17	open	1	
	A24	open	1			A16	close	0	

Base address in VME Standard space is F60000, in VME Extended space is 1FF60000.

FAIR/VME operating mode selection (J1)

	jumper	*mode*
J1	open	VME
	close	FAIR

/GATE source selection (J14)

The behaviour of the /GATE signal is like that an INHIBIT signal. The triggers (COM input) are not accepted when the /GATE signal is present. The J14 header allow the select between 2 different sources for this signal: from a line of the FAIR Bus (on the P2 connector) or from the front panel input (/GATE input). In VME operating mode should be selected the source from the front panel.

	header jumped	*/GATE source*
J14	1-2	from /GATE input on the front panel
	2-3	from a FAIR Bus trigger line

Header J14

The header J14 is for internal purpose. It has always to be configured with 2-3 pins jumped.

GLINH-GLTRG (JP1-JP2)

The signals GLINH (Global Inhibit) and GLTRG (Global Trigger) belong to the FAIR Bus transfer protocol. In the FAIR Bus protocol, when a front end module (ADC, TDC, etc.) acknowledges a valid trigger, it generates the signal GLINH. The signal GLINH arrives to the FAIR BUS System Controller that generates the signal GLTRG. The GLTRG is an input signal for all modules in the front end. By means of this signal the System Controller informs all modules in the front end that a valid trigger is occurred and validates it. Alternatively the System Controller can generate the RJTRG (Reject Trigger) signal to reject the event and to clear any operation (i.e. digitalization) in the front end about that event. In any case each module in the front end waits for GLTRG (to validate) or RJTRG (to reject) the event. These are necessary in order to synchronize all modules in the front end when the modules are working in multievent mode.
In VME operating mode, in order to simplify the cabling, when only one module (i.e. only one ADC) is present in the front end it is possible to enable the front end module to generate by itself the GLTRG signal at the GLINH occurrence.
To do that both the JP1 and JP2 headers must be jumped. When more than one front end module is present in the system and the acquisition is performed in multievent mode, this "auto-GLTRG" option may cause a loss of event syncrhonization among the modules. In this case the JP1 and JP2 headers has to be left opened (not jumped). The management of all the signals (MDTRG, GLINH, GLTRG, RJTRG) has to be performed by external electronics. A special VME acquisition control card has been developed for this purpose.

Configuration for VME operating mode (multievent case)